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A Wide Dynamic Range Radar Digitizer

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With the advent of high-speed, high-resolution analog to digital converters (ADCs) and associated digital to analog converters (DACs), there is a growing push to move more functionality into the digital signal processing arena. Receiver processing that has been performed in the analog and radio frequency (RF) domains is performed digitally now, with improved performance (near ideal filters and associated signal processing functions) as well as the flexibility to dynamically configure the channel characteristics (i.e., modulation and matched filter response).

However, converting from the analog to digital domain introduces errors which limit overall system performance. One of the most important limitations is dynamic range, which is the range of signal amplitudes that can be captured by an ADC. This defines the minimum detectable signal in the presence of a larger, interfering signal. This is set both by the number of bits and the Signal to Noise Ratio (SNR).

This article describes the use of a high speed, 16-bit ADC for weather radar signal capture. A simplified block diagram for this system is shown in Figure 1.

A 16-bit ADC is used to capture the (C Band) transmit pulse after down conversion to IF. This adequately records the start pulse for synchronization and associated signal phase for demodulation.

However, the input RF return signal has a dynamic range of 105 dB, which is greater than the (ideal theoretical) dynamic range for any commercial, high-speed ADC (limited to 16 bits). This dynamic range requires a 20-bit ADC as shown. To provide this capability, the normal input signal range is extended using instantaneous automatic gain control (AGC) as part of the digital signal processing (DSP) function.

ADC Dynamic Range

An ideal ADC has an SNR equal to $6.02 \times N + 1.76$ dB, where N is equal to the number of bits. For a 16-bit converter, this translates to 98 dB, which is the maximum (ideal theoretical) limit for input signal dynamic range. However, for high speed converters this ideal SNR is never achieved due to other issues which conspire to limit the SNR to a much lower value. These issues include ADC nonlinearity, front end amplifier noise and sample clock jitter. A typical SNR value for a high-speed (120 MHz sample rate) ADC is about 76 dB, which is well below the theoretical limit.

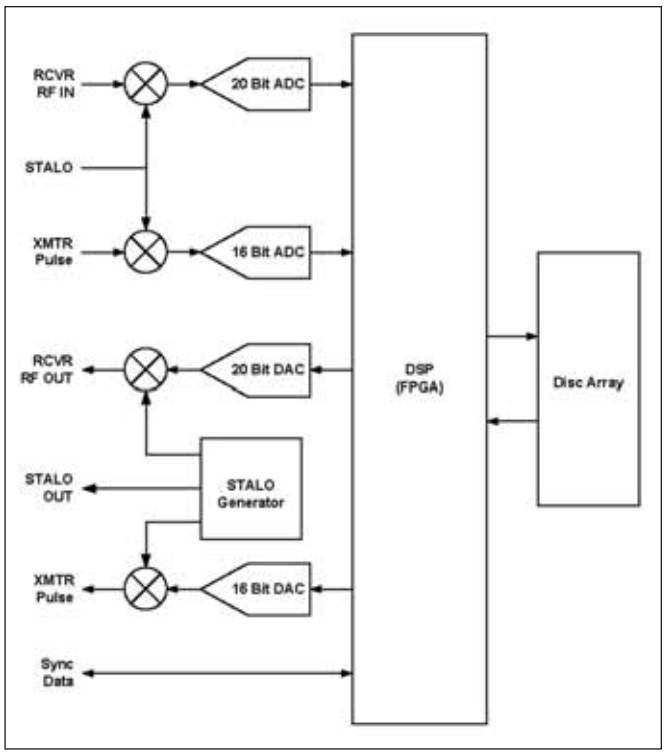

Figure 1 · Weather radar capture block diagram.

The ideal (98 dB) SNR is a comparison of the input noise level to a full scale input signal. In reality, the input signal level is constantly changing and is usually not known precisely. As a result, the maximum ADC input level is normally adjusted to at least one to three dB higher than the expected maximum input signal level. This, in turn, reduces the SNR for a (typical) full-scale signal input by the same amount.

Processing Gain

Although the dynamic range for an ADC is limited by its SNR, this range can be extended through processing gain if the full Nyquist bandwidth is not required. ADC noise is dominated by quantization noise, which can be considered random in nature. This noise is uniformly distributed across the Nyquist bandwidth, which is equal to one-half of the sampling rate as shown in Figure 2.

If digital filtering is used (after the ADC) to remove noise components outside the signal bandwidth, then the

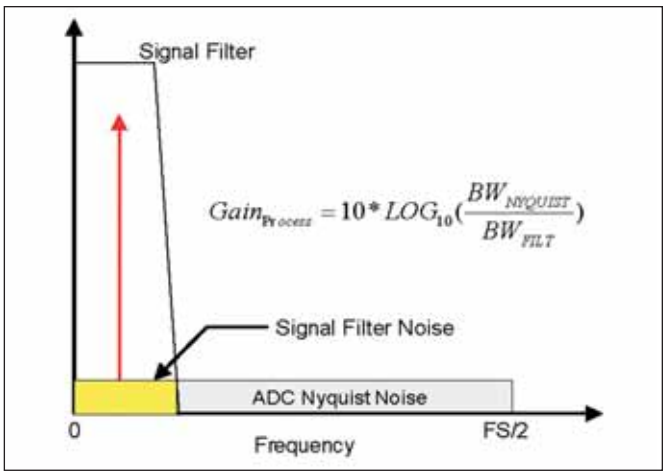

Figure 2 · ADC with processing gain.

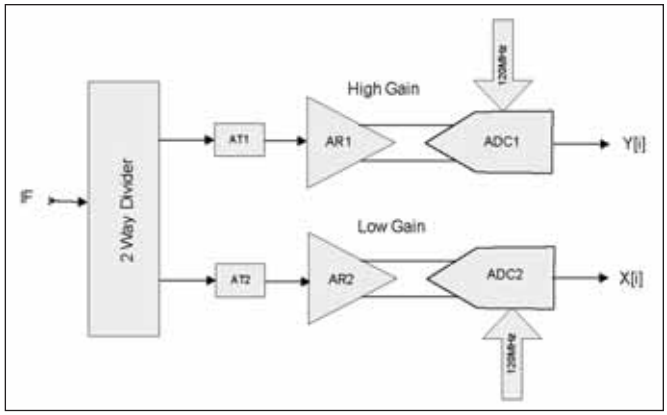

Figure 3 · Two channel extended range ADC.

RMS noise will be reduced with a corresponding improvement in SNR. This improvement is referred to as processing gain. By oversampling the input signal and then passing the signal through a low pass filter, we improve the SNR by:

$$SNR_{new} = SNR_{Nyquist} + 10 * \log_{10}\left(\frac{F_{NYQUIST}}{F_{FILT}}\right)$$

For example, consider an ADC with the following specifications:

Sample rate:	120 MHz
SNR @ 120 MHz:	76 dB
LPF bandwidth:	2 MHz

The SNR after processing gain is improved to approximately 90 dB:

$$SNR_{new} = 76dB + 10 * \log_{10}\left(\frac{60\ MHz}{2\ MHz}\right)$$

Hence, by utilizing a high sampling rate relative to the signal bandwidth, we can operate over a dynamic range greater than the inherent SNR.

RF Gain

The previous calculations examined the dynamic range expected from the ADC. Since the RF input signal to the ADC is usually amplified and or attenuated, we must examine the effects of the RF signal paths to come up with the system dynamic range. There are tradeoffs between noise figure, RF and IF gain, and ADC sensitivity.

To determine the optimum gain and noise figure for the system, the ADC can be treated as an RF element, and the noise figure equation can be used. The ADC noise figure, assuming a 2 MHz noise bandwidth and full-scale input of 2.25 $V_{p\text{-}p}$ (+11 dBm), is then:

$$ADC_{NFIG} = ADC_{NoiseFloor} - Noise_{System}$$

$$Noise_{System} = kTB + 10\log(BW_{Noise})$$

$$ADC_{NoiseFloor} = FullScaleLevel - SNR_{ADC}$$
$$= 11\ \text{dBm} - 90\ \text{dB} = -79\ \text{dBm}$$

$$ADC_{NFIG} = -79\ \text{dBm} - [-174\ \text{dBm}/\sqrt{\text{Hz}} + 10\log_{10}(2\ \text{MHz})]$$
$$= 32\ \text{dB}$$

If the desired system noise figure (F_S), ADC noise figure (F_{ADC}) and RF front end noise figure (F_{RF}) are known, the required gain (G) for the system preceding the ADC can be calculated by using the following equation:

$$F_S = F_{RF} + \left(\frac{F_{ADC} - 1}{G}\right)$$

Solving for G:

$$G(dB) = 10 * \log 10\left(\frac{F_{ADC} - 1}{F_S - F_{RF}}\right)$$

For example, assume the required system noise figure is 5 dB, and the low noise amplifier noise figure is 2 dB. Using the gain equation, the required gain is 30 dB. Note that this is not an exact calculation, as it does not include the effects of all the RF and IF components. However, it is a good starting point for a detailed cascade analysis.

Clock Jitter

As discussed previously, the SNR for a high speed ADC rarely approaches ideal. One of the important contributors to system SNR is clock jitter. Hence, a very low-jitter clock is essential to good SNR.

Clock jitter limits the SNR of an ADC according to the following equation, where F_{IN} is the maximum frequency of the analog input signal:

$$SNR_{Jitter} = -20 * \log_{10}(2 * \pi * F_{IN} * t_{jitter})$$

For example, assume an input signal of 30 MHz and a required SNR of 80 dB. This, in turn, requires a clock with jitter of no more than 531 picoseconds. This assumes an ADC SNR that is much better than 80 dB, making jitter the limiting factor.

Clocks and oscillators are often specified in terms of phase noise rather than timing jitter. The two are similar, and phase noise can be converted to jitter. Raltron offers a Web-based calculator [2] for this purpose.

Wide Dynamic Range Digitizing

As mentioned previously, recording weather radar signals requires a minimum of 105 dB of dynamic range. Since the dynamic range of available high speed ADCs is limited to 90 dB (with processing gain), with further reductions down to 80 dB due to the clock source (jitter), a simple ADC is not sufficient.

Symtx Inc. has implemented a dual ADC scheme to increase digitizer dynamic range as shown in Figure 3. The design uses a high-gain channel to process low-level signals and a low-gain channel to process high-level signals, with simultaneous sampling of both channels in parallel. The gain difference between the high-level and low level ADCs is compensated with an appropriate *n*-bit left shift to give the correct scaling. A DSP after the two ADCs then selects the correct ADC output, adjusts for gain, and merges the two to create a 20-bit word with the desired dynamic range.

The process is essentially an instantaneous AGC which responds to the signal amplitude at the input. Since range bins for weather radars are on the order of 1 microsecond, the DSP operates by scanning the data for each range bin to determine the maximum signal amplitude. If this is within the maximum level for the high-gain (low-signal-level) ADC, it is used for data collection (to maximize signal resolution). If any sample exceeds this threshold, all data in the range bin is collected using the low-gain (high-signal-level) ADC.

Notes on Clocks

For ultra low jitter performance, OCXO oscillators with SC cut and AT cut crystals will provide the best performance. For example, ULN OCXOs from Wenzel Associates offer femtosecond jitter performance with ultra low phase noise. The main drawbacks of these oscillators are their size and cost. They also consume up to several amps of current and are generally not suited for PCB mounting.

PCB mounted low cost oscillators may not achieve sub picosecond performance, but for many applications they are sufficient. Some of the better PCB mounted oscillators offer jitter performance of 1 ps maximum and 0.5 ps typical at a unit cost of $2.

Low jitter clock distribution ICs are also readily available that fan out the ADC clock to handle multiple components, while adding insignificant amounts of additional jitter.

As shown in Figure 3, AT1 and AT2 are set to provide gain separation between the two input channels. This gain separation represents the increase in dynamic range possible with this scheme.

For example, if a dynamic range of 105 dB is required and the separation between the two channels is 24 dB, the high level ADC output is shifted left 4 bits. The required ADC dynamic range is reduced to 81 dB, which is achievable with typical ADC SNR and clock jitter specifications.

Calibration

When selecting between the high- and low-gain ADC outputs, an error modulation signal will be imposed on the captured waveform if there is an offset or gain error between the two channels. Depending on the application and the size of the error, calibration may be required to remove the offset.

The offset error is generally small if a matched ADC pair is used (typically used for I-Q applications). This is particularly true for RF designs that use AC coupled inputs. The dominant error is typically differential channel gain, due primarily to the components preceding the ADCs (i.e., amplifiers, attenuators, and power splitters). If significant, this gain error can be corrected via analog tuning or digitally following signal capture.

Digital Down-Conversion (DDC)

For the weather radar capture and playback system shown previously, signal capture is performed at IF followed by several functions in the DSP (FPGA):

- Combine the two ADC inputs into a single, 20-bit digital signal output
- Convert these into in-phase (I) and quadrature (Q) outputs
- Decimate
- Low-pass filter

The result is a baseband signal, stored in I-Q format.

The process of down-conversion and conversion to I-Q outputs is accomplished by multiplying the input signal by

$$\cos[(2\pi * f)/(F_S * n)] \quad \text{and} \quad -j\sin[(2\pi * f)/(F_S * n)]$$

and sampling the resulting signals where:

f = Input signal center frequency
F_S = Sample rate

This process is greatly simplified by selecting a sample rate which is 4× the 30 MHz IF center frequency (120 MHz). In this case, $f / F_S = 1/4$; thus, $2\pi * f / F_S * n = \pi * n / 2$. In degrees, $\pi * n / 2$ is 0, 90, 180, 270, etc. Therefore, these expressions resolve to:

$$\cos(2\pi * f / F_S * n) = 1, 0, -1, 0, \ldots$$
$$-j\sin(2\pi * f / F_S * n) = 0, -1, 0, 1, \ldots$$

Since the sine and cosine sequences (I-Q values) now contain alternating zero values, the zero valued data can be eliminated. Figure 4 shows the resulting effects on the input signal spectrum.

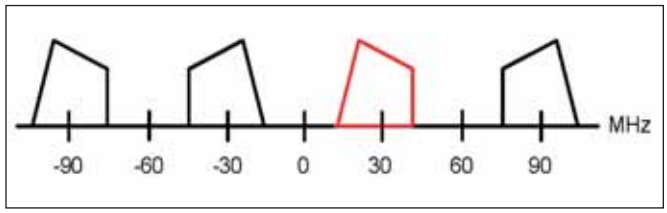

Figure 4 · Real signal spectrum.

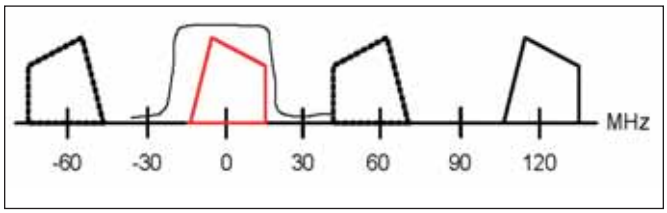

Figure 5 · Spectrum after down-conversion and filtering.

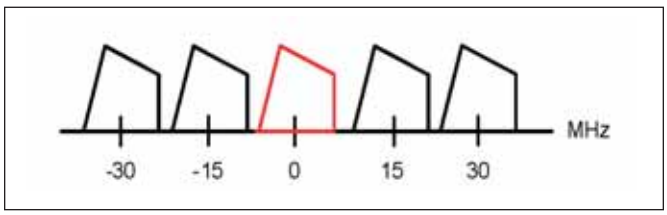

Figure 6 · Output after decimation.

Summary

High-speed RF signal capture with wide dynamic range signals is readily achievable with today's high-speed ADCs. With careful design followed by the appropriate digital signal processing, it is possible to capture and recreate signals with dynamic ranges in excess of 100 dB.

References

1. Brad Brannon, "Sampled Systems and the Effects of Clock Phase Noise and Jitter," Analog Devices App. Note AN-756.

2. Phase Noise to Jitter Calculator, http://www.raltron.com/cust/tools/osc.asp.

3. Raymond Cerda, "Impact of ultralow phase noise oscillators on system performance," *RF Design,* July 2006.

Author Information

Paul Hiller is chief technology officer for Symtx. Ed Crean serves as a Senior RF Engineer for Symtx. Located in Austin, Texas, Symtx Inc. is a manufacturer of functional test systems for electronic systems including engineering, depot, and production line applications; commercial and military satellite systems; and commercial and military avionics systems. Interested readers may contact Ed Crean by e-mail at: ECrean@SymTX.com