

Effective Use of Ceramic Capacitor Tuning Sticks for Impedance Matching

By Saroj K Patro, Yatin Buch and Ravi B Kishore

Even with advanced EDA tools, manual tuning methods still have a place in RF engineering, particularly in the matching of high performance power amplifiers

This article explains how to make use of the well known industry standard multilayer ceramic capacitors of larger pad size, including the self-inductance effect of the lead lengths.

The article also describes an effective way of calculating resonance effects in the frequency band of interest so as to transform that parasitic effect into smaller size, more cost effective, low loss capacitors. Practical results are also demonstrated to support the theory.

Introduction

Advanced radio frequency (RF) power amplifier designers and manufacturers are facing increasing pressure in terms of delivering linearity while maintaining reasonable efficiency at the same time. To this end, the use of very high end linearization techniques, supported with high efficiency architectures are definitely becoming popular [1-4]. In a complex PA system, use of very low loss passive components are as important as any other high power devices sitting on the same board. Any amount of extra loss contributed by the matching capacitors is not desirable due to the fact that it will require both high power and small signal driver sections to deliver extra power and gain, along with the related cost implications. Keeping this in mind, designers are increasingly making use of low loss multilayer ceramic capacitors, both in the small signal and high power sections. Capacitors of 0603 size are one of the best alternatives from low Effective Series Resistance (ESR) and cost points of view [5-6].

Nearly all new designs for contemporary amplifiers use very small size capacitors and other passive parts to reduce one or more combinations of loss, board space and cost. Due to this, the bigger size capacitors (110 × 110 mils) are becoming less popular for design use. But, these capacitors can definitely be used for tuning of impedance matching circuits in the laboratory environment when they are available in the inventory.

Matching Circuit Tuning

Even with the availability of powerful EDA simulation tools like ADS to give the RF designer a first cut matching circuit for amplifiers, it is never a 100 percent solution to the practical result achieved at the test bench environment. This is due to many factors like the imperfect modeling of the entire system in the EDA environment, or all the parasitics of various circuit components. Also, there may not be models of all components available for simulation. Being aware of this design imperfection, experienced RF designers still follow the empirical method of RF board tuning in the final test bench set up to finalize the circuit topology.

While the empirical technique for coming up with an impedance matching circuit is well known, it can be more valuable when one can visualize the parasitic effects of the tuning elements (such as inductors and capacitors) used in the laboratory environment. RF designers mainly follow two ways of board tuning: one, by trial and error method of putting additional components either in series or in shunt path in line with the amplifier device positions and at fixed relative locations with respect to the active device while the DC

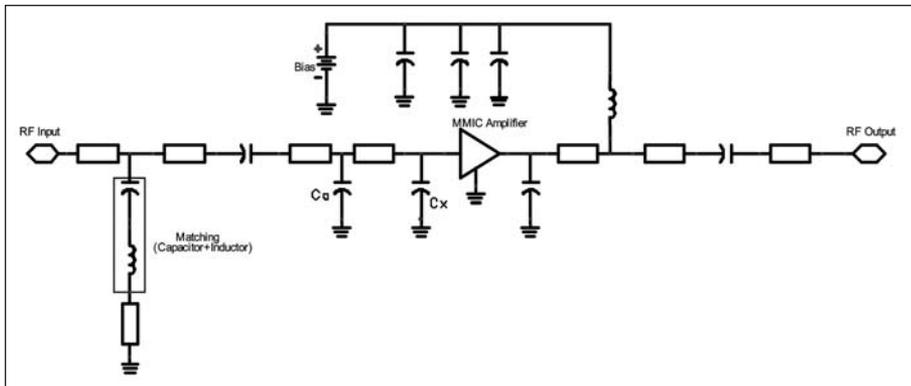


Figure 1 · Existing 1900 MHz amplifier circuit.

and RF signals are active in the circuit elements. The other is doing the above exercise with DC/RF OFF condition for functional testing.

An Example Circuit and Its Tuning

This section illustrates the approach adapted here for determining a first-cut matching circuit while “up-banding” an existing circuit. Figure 1 shows a MMIC amplifier with its associated lumped and distributed matching components. The following sections will illustrate the step-by-step methodology for finding an optimum impedance matching circuit for

a higher frequency band where this amplifier circuit is now intended to operate.

I. Existing Amplifier Results

First, the plots of the existing circuit (1900 MHz) are shown in Figures 2-4. Here, we followed the empirical method of test bench tuning of the available matching circuit as shown in Figure 1. The circuit was biased with +5 volts DC supply by feeding at the L3 end. First, swept measurements were taken for S_{21} , S_{11} and S_{22} for 1900 MHz band with no component changes.



Figure 2 · S_{21} plot in the 1900 MHz band.



Figure 3 · S_{11} plot in the 1900 MHz band.

II. Existing Amplifier Swept for High Band

Next, we swept the 1900 MHz circuit for 2100 MHz with no component changes. Those results are shown in Figures 5-7.

Reduced gain (gain reduced by more than 1.6 dB) is noticed in this band, which is obvious and which means that the circuit is non-optimal for this band and needs tuning. Our aim should be to get same or more gain in the 2100 MHz band as like the 1900 MHz band.

III. DC Blocking Capacitor Replacement

The next phase of our tuning consists of replacing all the DC blocking capacitors to be suitable for 2100 MHz band.

The amplifier circuit of 1900 MHz was swept for 2100 MHz with all the DC blocking capacitors changed to 6.8 pF. By doing this, the gain is further reduced; though the reduction in gain is only marginal. In this case, the designer can always retain the same old DC blocking capacitors (all 10 pF). The results after these changes are shown in Figures 8-10.

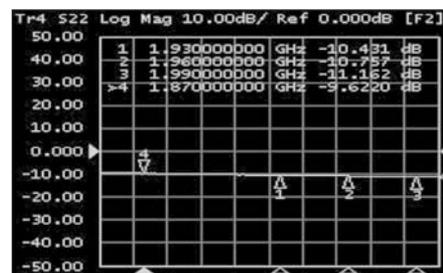


Figure 4 · S_{22} plot in the 1900 MHz band.

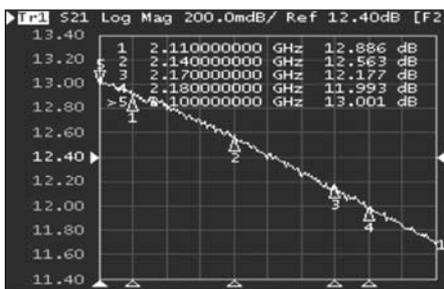


Figure 5 · S_{21} plot in the 2100 MHz band (unchanged).

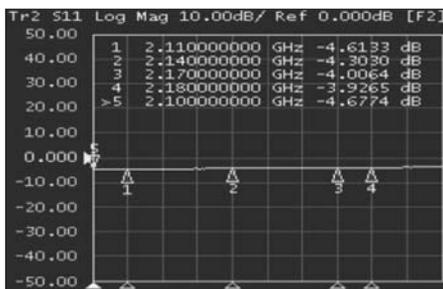


Figure 6 · S_{11} plot in the 2100 MHz band (unchanged).



Figure 7 · S_{22} plot in the 2100 MHz band (unchanged).

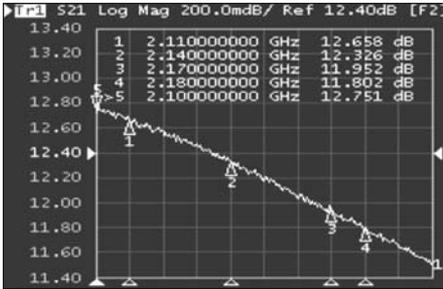


Figure 8 · S_{21} plot after changing DC blocking capacitors.

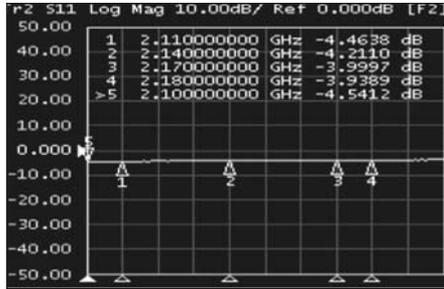


Figure 9 · S_{11} plot after changing DC blocking capacitors.



Figure 10 · S_{22} plot after changing DC blocking capacitors.

IV. Tuning with 100B Series Capacitor Stick

This step is crucial as we aim to get the proper gain by doing input circuit tuning. We first start with the R22 position (the series L-C network in Figure 1) and try to use a tuning capacitor stick as available in the lab. This happened to be a 100B series tuning stick and with this, we get good gain as like 1900 MHz band. We have also soldered the extended pins of the tuning stick to keep the circuit operational for more duration without touching for consistency in the result achieved. 2100 MHz swept with R22 = 5.6 pF (100B series tuning capacitor stick). The S_{21} result is shown in Figure 11.

V. Use of 600S Series Capacitor On-board

In this step, we then replaced with a 5.6 pF 600S series capacitor for the reasons as mentioned earlier. But, by doing this, we noticed a drastic change in the S_{21} results, which is the main theme of this article. With

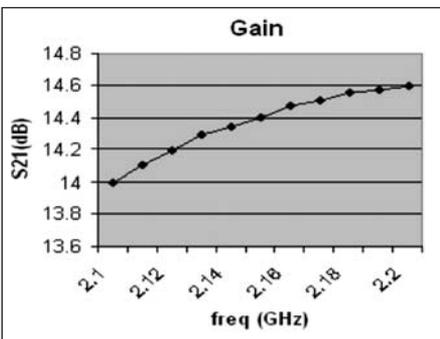


Figure 11 · S_{21} plot with a 5.6 pF 100B series capacitor at R22.

this capacitor, we got deep negative gain and also the input/output return loss was badly affected. This is mainly due to two things: one, we had used a larger size 100B series capacitor, with series resonance at a different frequency, and which does not match the SRF of the 600S series capacitor (see Figures 12 and 13). Second, we have not accounted for the “lead inductance effect” of the tuning stick capacitor mounting.

By comparing the SRF of the two data, we find that 100B series 5.6 pF capacitor has SRF at 2.7 GHz and that of 600S series has SRF at 5.5 GHz with the same value of the capacitance. Now, to get a 600S series

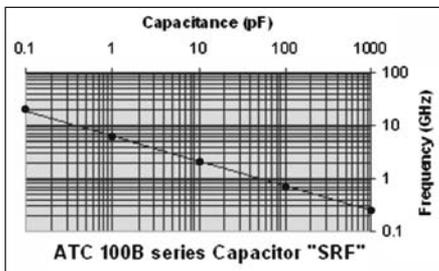


Figure 12 · SRF vs. capacitance of the 100B series capacitor.

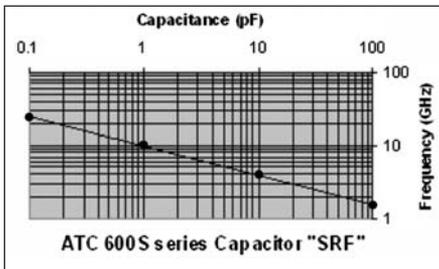


Figure 13 · SRF vs. capacitance of the 600 series capacitor.

capacitance value, which has an SRF at 2.7 GHz, we again see the plot and find that value to be 30 pF (approx.) in the 600S series. Figure 14 shows the poor result with the 5.6 pF 600S series tuning capacitor.

VI. Mapping of 600S and 100B Series Capacitors

We tried to take care of the first effect, that is, by trying to match the SRF of 100B series 5.6 pF capacitor with an equivalent capacitor from 600S series and having the same SRF. From the published data [7-8] of ATC capacitors and by doing a relative comparison, we found that 5.6 pF (of 100B series) is equivalent to 30 pF (of 600S series) in terms of SRF. So, then, we soldered a 600S series 30 pF capacitor in R22 position. By doing this, the gain rose to positive region but was not sufficient, as we had not yet considered the second effect. Figure 15 shows the 2100 MHz swept results with the 30 pF 600S series tuning capacitor only, without considering the lead inductance effects of the tuning sticks.

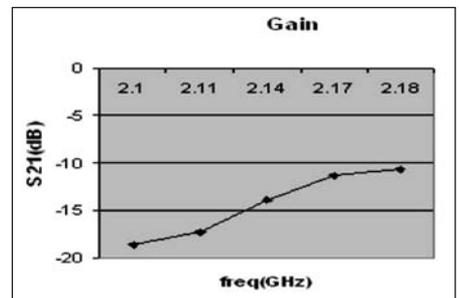


Figure 14 · S_{21} plot with a 5.6 pF 600S series capacitor.

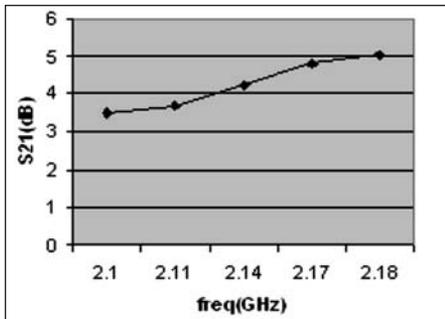


Figure 15 · S₂₁ plot with a 30 pF 600S series capacitor.

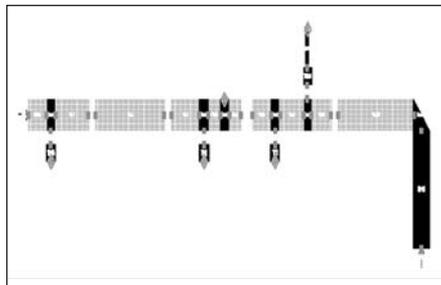


Figure 19 · Layout of the amplifier.

VII. Lead Inductance Effect

Next, we started to investigate the lead inductance effect. Since 100B series tuning stick’s leads are 10 mm long (approx.) on both sides, we found that the self inductance of this straight wire is around 7 nH [9-11]. Nearest available standard inductor was 6.8 nH (0805 series). Now, both 30 pF (600S series) and 6.8 nH were soldered in series in R22 position and S-parameters were plotted. Immediately, gain increment was seen with this change. Another thing was tried finally to improve the gain flatness further with C_x = closer to device input = 0.4 pF and C₄₅₉ = 1 pF and with input L-C combination (at R22 position): L = 6.8 nH (0805 size) and C = 30 pF (0603 size). The final amplifier plots are shown in Figures 16-18, and its layout is shown in Figure 19.

Conclusion

This approach, as described in this paper, is applied to an existing and working power amplifier module, the results of which are shown.

Theoretical predictions were very close to the practical implementation. This unique and practical method is applicable to all the RF active as well as passive circuits. Also, this is helpful in the lab environment, where, one can effectively utilize the existing and available matching components and can still come up with a very good impedance matching circuit without going for all-new components at the prototype phase of sub-block characterization.

References

1. David M. Upton, “A New Circuit Topology to Realize High Efficiency, High Linearity, and High Power Microwave Amplifiers,” *Proceedings 1998, RAWCON*, pp. 317-320.
2. M. Iwamoto, A. Williams, P.F. Chen, A. Metzger, C. Wang, L.E. Larson, P.E. Asbeck, “An Extended Doherty Amplifier with High Efficiency over a Wide Power range,” *IEEE MTT-S Digest*, 2001, pp. 931-934.
3. Jangheon Kim, Jeonghyeon Cha, Ildu Kim, Sang Yeon Noh, Cheon Seok Park, and Bumman Kim, “Advanced Design Methods of Doherty Amplifier for Wide

Bandwidth, High Efficiency Base Station Power Amplifiers.”

4. Ray Gutierrez, “High-Efficiency Linearized LDMOS Amplifiers Utilize the RFAL Architecture,” *High Frequency Electronics*, February 2006, pp. 22-28.

5. Richard Fiore, “RF Power Amplifiers Operate Cooler with Improved Reliability Using ATC’s EIA 600 Series Ultra-Low ESR Ceramic Capacitors,” *Microwave Product Digest*, May 2003.

6. Richard Fiore, “RF Ceramic Chip Capacitors in High RF Power Applications,” *Microwave Journal*, April 2000.

7. 100B Series data sheet, American Technical Ceramics.

8. 600S Series ATC data sheet, American Technical Ceramics.

9. Biswajit Ray, “When Is A Capacitor Not A Capacitor?” *The Physics Teacher*, Vol. 44, Feb. 2006.

10. J. Cain, “Parasitic inductance of multilayer ceramic capacitors,” AVX Corp., <http://www.avx.com/docs/techinfo/parasitic.pdf>.

11. Richard Fiore, “Capacitors in Broadband Applications,” *Applied Microwave & Wireless*, May 2007, pp 40-53.

Author Information

Saroj K Patro is working as a Technical Lead in HCL Technologies (PIDC), Chennai, India. He can be reached at: sarroj.patro@gmail.com

Yatin Buch is a Senior Principal Project Engineer at Powerwave Technologies, USA.

Ravi B Kishore is Senior Program Manager at HCL Technologies.

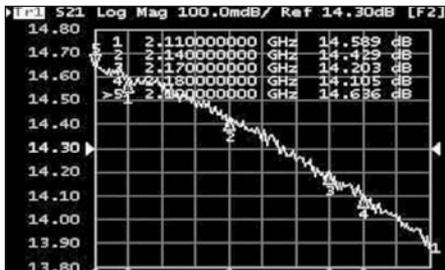


Figure 16 · S₂₁ plot after inductance correction and final tuning.

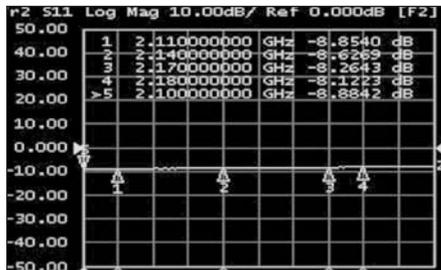


Figure 17 · S₁₁ plot after inductance correction and final tuning.

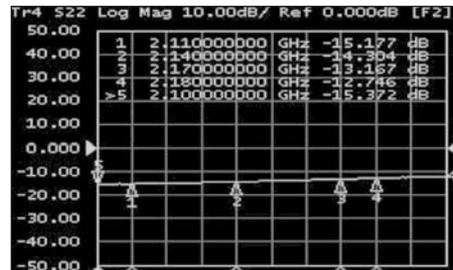


Figure 18 · S₂₂ plot after inductance correction and final tuning.