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CAD Analysis of Microstrip Lines Using Micromachining Techniques

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This article provides an analysis of microstrip lines on a silicon substrate, using the method of a thicker inteface layer to reduce losses and increase *Q*

The possibility of low cost RF and microwave circuits integrated with digital and analog circuits on the same chip is creating a strong interest in silicon as a microwave circuits. Semiconductor silicon substrates with 1 to 20 Ω-cm resistivity are typically used to manufacture mixed signal RFICs, and this type of conductive substrate is the well-known cause of signal losses in passive circuits. Commercial foundries employ low resistivity wafers, having higher losses or low *Q* factor due to leakage in the substrate. To overcome this problem, different topologies have been demonstrated. The commonly employed method is the use of a high resistivity substrate (>2k Ω-cm), and circuit realization on this substrate shows performance on par with other dielectric substrates like GaAs [1]. Another method employs the use of polyimide on top of the CMOS substrate to create an interface layer [2]. The third approach employs ground plane patterned between silicon substrate and the interface layer so that the electric field leakage can be reduced to zero [3]. However all these approaches are either costly or are complex to analyze. The simpler approach is the use of thicker interface layer.

This paper can be subdivided into two parts. In the first part, an interface layer of silicon with varied thickness is deposited and microstrip line characteristics are found out. This approach was tried by Wang et al. [4] for FG-CPW lines but not for the characteristics of the microstrip lines. The second subset is the combination of two and three interface layers namely oxide-nitride as well as oxide-nitride-oxide, respectively, and characteristics of lines are observed.

Propagation Characteristics

Microstrip lines are important and simpler structures to analyze for the lower end of the mm-wave frequency range. A quasi-TEM microstrip lines can be characterized by frequency dependent *RLGC* distributed circuit model as shown in Figure 1a. The line can be characterized by primary and secondary parameters. The series resistance *L* represents the total self-inductance of signal and ground, the series resistance *R* represents the resistance due to finite conductivity of the signal and ground and the shunt conductance *G* is due to current induced in the substrate from dielectric loss. Using the interface layer above the silicon, the structure may be thought of Metal-Insulator-Semiconductor (MIS) that may support three modes of propagation namely: skin effect mode, dielectric quasi-TEM mode and a slow-wave mode. These phenomenons are due to the electric and magnetic losses of the silicon substrate and are highly dependent on the conductivity and working frequency [5]. The silicon substrate acts as the dielectric layer if conductivity is very low and it will support dielectric quasi-TEM mode. High frequency and high conductivity will make the silicon substrate act as a metal layer and it supports skin effect mode. Moderate conductivity and working frequency will lead to slow wave mode. Each propagation mode has the corresponding equivalent circuit model as shown in Figure 1.

The capacitance values shown in Figure 1

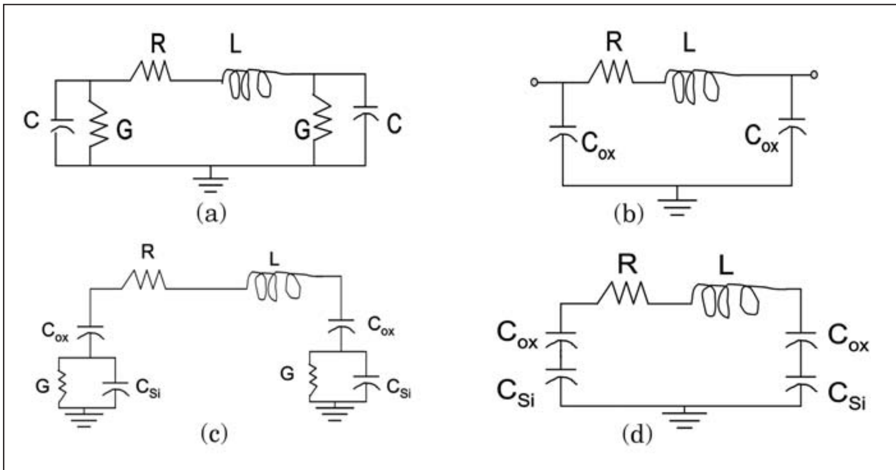

Figure 1 · Simplified models for different resistivities: (a) Transmission line, (b) Zero resistivity, (c) Moderate resistivity, (d) High resistivity.

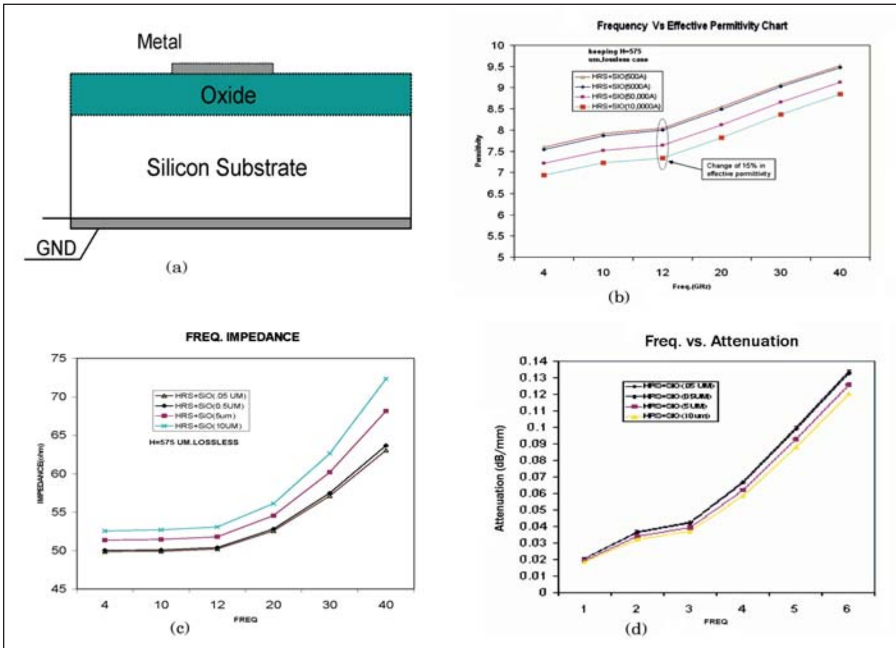

Figure 2 · Interface layer of oxide: (a) Simplified view of the structure, (b) Variation of thickness, (c) Variation in impedance, (d) Attenuation characteristics with varying thickness.

for both C_{ox} and C_{si} can be obtained as

$$C = \frac{\omega.\ell.\varepsilon_0\varepsilon_{eff}}{t_{eff}} \quad (1)$$

where,

$$t_{eff} = \frac{\omega}{2\pi}\ell n\left(\frac{8t}{\omega}+\frac{4\omega}{t}\right)$$

and,

$$\varepsilon_{eff} = \frac{1+\varepsilon}{2}+\frac{\varepsilon-1}{2}\left(1+\frac{10t}{\omega}\right)^{-1/2}$$

The value of G is then obtained by

$$G = \frac{t_{eff}}{\sigma_{eff}\omega.\ell} \quad (2)$$

where,

$$\sigma_{eff} = \sigma\left[\frac{1}{2}+\frac{1}{2}\left(1+\frac{10t}{\omega}\right)^{-1/2}\right] \quad (3)$$

and ω is the width of the metal line, σ is the conductivity, is the line length, t is the thickness and ε is the dielectric constant.

CAD Analysis of the Microstrip Line

The coplanar waveguide was studied by Schollhorn et al. [6] and found out the loss mechanism. In this paper microstrip lines over different interface layer have been studied up to 40 GHz and the variation in the interface thickness along with the substrate height variation is studied. The effect on the attenuation characteristics is also observed. The total attenuation is the contribution of conductor as well as dielectric losses. The total loss tangent of a lossy substrate can be written as [7]

$$\tan\delta_T = \frac{\omega\varepsilon''+\sigma}{\omega\varepsilon'} = \tan\delta_D + \tan\delta_L \quad (4)$$

where $\tan\delta_D$ is the polarization loss of the silicon substrate, and $\tan\delta_L$ is the extrinsic loss due to finite conductivity of the silicon substrate All these analysis assumes constant line width of 0.45 mm and idealized ground plane along with the metallization thickness of 1 µm. The analysis is carried out using the 2D EM field theory based full-wave simulator MMICTL [8] using the enhanced spectral domain method.

Interface Layer of Silicon Dioxide

The Spectral Domain Approach has been used to analyze the lines on the standard silicon substrate. The 575 µm standard silicon substrate (denoted as HRS) is taken, over which oxide layer has been deposited. Figure 2 shows the simplified view along with the effect of the varying thickness on the effective permittivity. The permittivity decreases by 15%

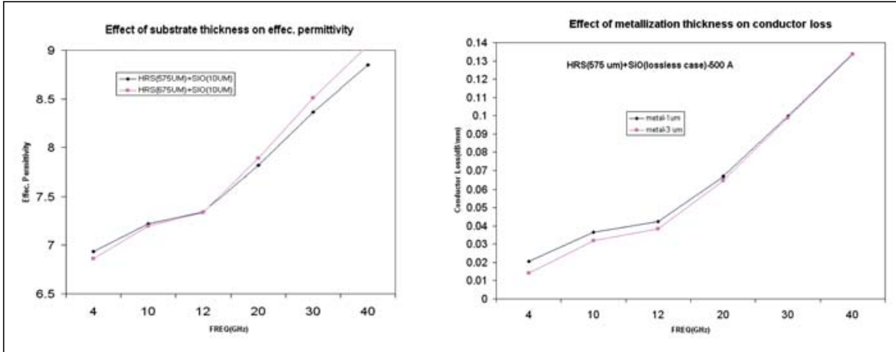

Figure 3 · Effect of substrate and metallization thickness.

with the variation of the thickness from 500 Å (0.05 µm) to 10,000 Å (1µm). The polynomial expression for effective permittivity can be written as follows

$$y = 0.008775f^5 - 0.1681f^4 + 1.3574f^3 - 3.8902f^2 + 5.9159f + 4.3544$$

The effects of impedance variation as well as attenuation characteristics are shown in Figure 2. The losses of silicon substrate minimizes as the thickness of interface layer increases.

Effect of Substrate and Conductor Thickness

The effect of substrate thickness on the effective permittivity is also studied. The parameters like oxide interface layer thickness and width of the microstrip is kept constant. The result indicates an appreciable change in effective permittivity after 20 GHz.

The effect shows metal thickness (Figure 3) has minimal effect on the conductor losses after 12 GHz. This result should be self-explanatory, as it is consistent with the theory of skin depth.

Interface Layers of Oxide and Nitride

Most commonly used interface layer of oxide (500 Å) and nitride (1500 Å) is commonly used in MEMS structures. The effect of these layers on the effective permittivity and attenuation is shown as in Figure 4.

Interface Layers of Oxide, Nitride and Oxide

The effect on line characteristics due to the combination of three interface layers of oxide (7000 Å), nitride (3000 Å) and oxide (7000 Å) is also studied. Figure 5 shows that this combination not only minimizes the substrate losses effect, but effective permittivity also remains constant in the full band. These concepts also reduces the inter-layer stress level to the minimum. The assumption of an ideal ground plane has tremendous effect on the attenuation characteristics which can be seen in Figure 5(d).

Conclusion

The paper presents the effect of the oxide layer on the different parameters of the microstrip line. For stress relieving, the designer can use use the oxide along with nitride. But these methods need still higher thickness to avoid substrate effects. Authors believe that, instead of two passivation layers, if three passivation layers namely oxide, nitride and oxide are used then the effect of lossy silicon can be minimized. This combination is also useful in stress relieving while device fabrication. The optimum thickness depends on the stress relieving criteria for these types of

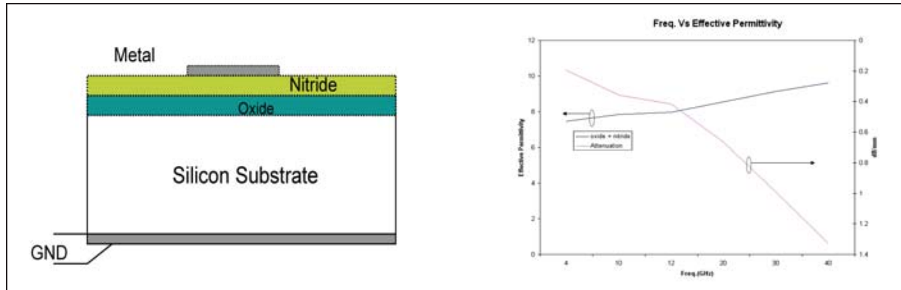

Figure 4 · Two layer concept and its characteristics.

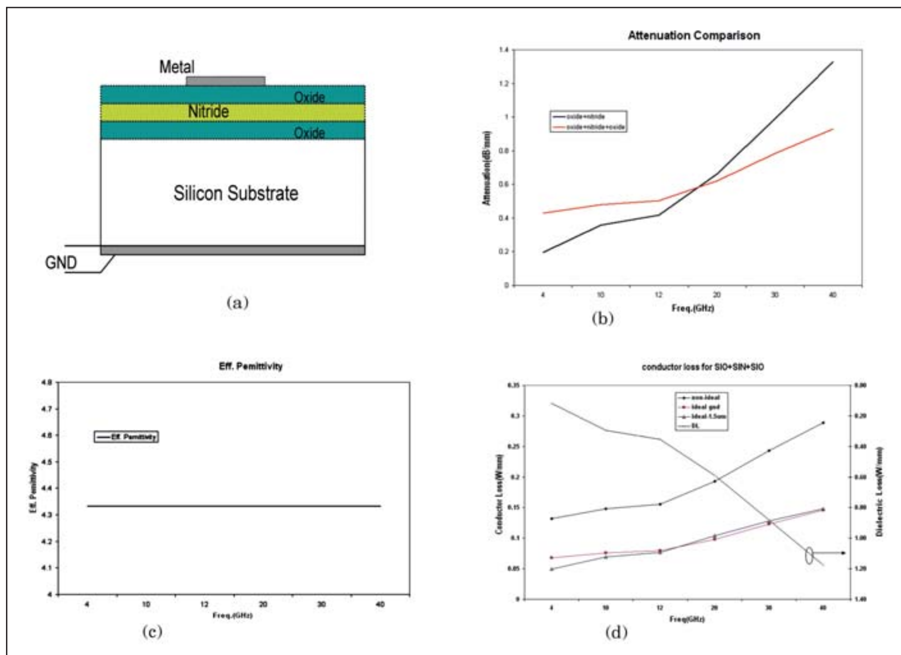

Figure 5 · Three layer concept (a) simplified view (b) attenuation comparison with two layer concept (c) effective permittivity variation (d) losses variation.

films along with foundry limitations. Further study on the package effects, and coupled lines expressions have to be carried out.

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