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Designing Resistive Unequal Power Dividers

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This article presents the design methods for resistive power dividers that provide a simple means of achieving unequal outputs over a wide bandwidth

The resistive power splitter of Figure 1 has long been a favorite of RF and microwave engineers. It divides an RF input signal equally between its two output ports. This splitter is a natural choice when flat frequency response is required over a very broad frequency range. Its simplicity makes it an attractive option for many designs.

When unequal output amplitudes are desired, a similar splitter can be constructed. Figure 2 illustrates a power splitter with unequal outputs. The power loss at the primary output port can be any value between 0 dB and 6.02 dB. The power loss at the secondary output port will be some value greater than 6.02 dB. For example, a splitter that has 1.72 dB loss at its primary output will have 20 dB loss at its secondary output. All ports are matched to some characteristic impedance, Z_0.

Since the unequal splitter consists of only four resistors, its size and cost are negligible in most applications.

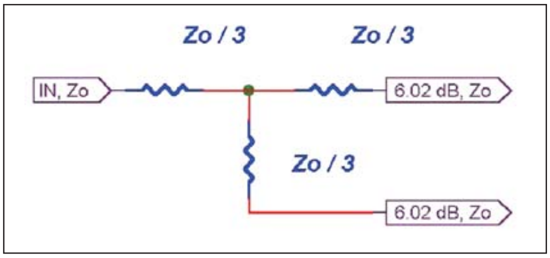

Figure 1 · Resistive power divider with equal outputs.

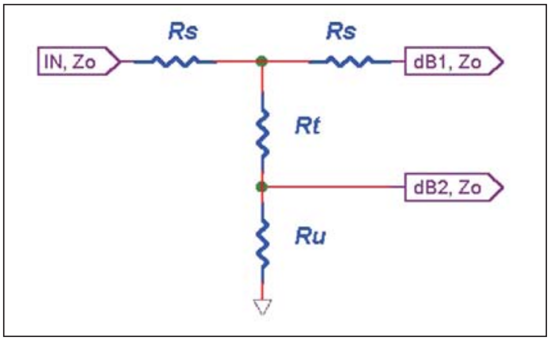

Figure 2 · Unequal resistive power divider.

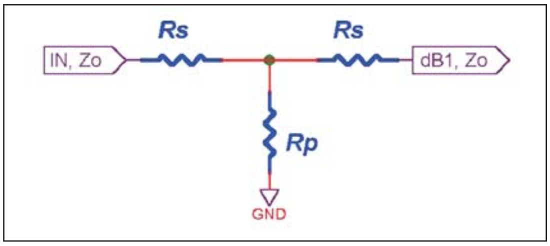

Figure 3 · The familiar Tee Pad resistive attenuator.

Design Procedure

In order to design the unequal splitter, first consider the Tee pad of Figure 3. This pad can be designed to have some value of loss, less than 6.02 dB. To get the second output, we'll replace the parallel resistor R_p with a voltage divider, as shown in Figure 2. The resistor values Rt and Ru will be chosen so that when output 2 is terminated in Z_0, the resulting network has the same resistance as R_p, and so that port 2 presents an impedance of Z_0 to its load when the other ports are terminated in Z_0. The attenuation at output 2 will depend on the attenuation value that we choose for output 1. The lower the attenuation at output 1,

*dB*1	*dB*2	R_s (ohms)	R_t (ohms)	R_u (ohms)
0.1	44.80	0.287	4317.704	50.582
0.5	30.81	1.438	842.368	53.055
0.55	30.00	1.582	763.280	53.382
1.00	24.78	2.875	406.805	56.523
1.72	20.00	4.94505	222.527	62.499
2.00	18.68	5.731	186.947	65.168
3.00	15.01	8.549	111.529	77.531
4.00	12.25	11.313	71.755	97.698
4.92	10.00	13.794	47.159	136.037
5.00	9.80	14.006	45.288	141.601
6.00	6.45	16.613	19.254	1026.093
6.02	6.02	16.666	16.666	OPEN CKT

Table 1 · Component values for resistive dividers with various common attenuation values.

the higher the attenuation at output 2. Some typical values are shown in Table 1 and plotted in Figure 4.

First, choose a value of attenuation for output 1, and design the Tee pad of Figure 3 for that attenuation value.

Z_0 is its characteristic impedance.
*dB*1 is its attenuation.
α is its voltage gain. ($0.5 < \alpha < 1$).

Given the value of *dB*1, and normalizing Z_0 to unity, we can solve for the resistor values R_s and R_p.

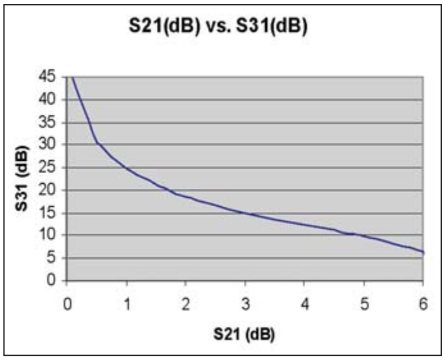

Figure 4 · Plot of power division values given in Table 1.

$$Zo = 1$$

$$\alpha = ALOG\left(-\frac{dB_1}{20}\right)$$

$$Rs = \left(\frac{1-\alpha}{1+\alpha}\right)$$

$$Rp = \left(\frac{1-Rs^2}{2\cdot Rs}\right)$$

Now, let R_p from the network above be broken up into a network consisting of R_t, R_u, and the port 2 load impedance Z_0. We require that the resistance of this network, from the top of R_t to ground, be equal to R_p above. We also require that the output impedance at port 2 be equal to Z_0. With these two conditions, we can solve for the values of R_t, and R_u.

$$Ru = \sqrt{\frac{1}{1-\frac{4}{2\cdot Rp+Rs+1}}}$$

$$Rt = Rp - \left(\frac{Ru}{Ru+1}\right)$$

At this point, we have chosen values, which satisfy the conditions for a desired attenuation value at port 1, and for all ports to be matched to Z_0.

There are no more degrees of freedom, since all of our resistor values have been assigned. We now solve for the attenuation at port 2.

In order to simplify the notation, we introduce the intermediate variable Q.

$$Q = \frac{Rp + Rp \cdot Rs}{Rp + Rs + 1}$$

$$\beta = \frac{Q^2 + Q \cdot Rs}{\left(1 + \frac{1}{Ru}\right) \cdot Rp}$$

where β is loss at port 2, as a voltage ratio, that is: $dB2 = 20\,Log(\beta)$

The design equations will now be restated in cookbook form:

Variables S, P, and T are the normalized values of R_s, R_p, and R_t, respectively.

Given: Z_0 is the system characteristic impedance and $dB1$ is Loss at port 1

$$S = \left(\frac{1 - \alpha}{1 + \alpha}\right)$$

$$P = \left(\frac{1 - S^2}{2 \cdot S}\right)$$

$$U = \sqrt{\frac{1}{1 - \frac{4}{2 \cdot P + S + 1}}}$$

$$T = P - \left(\frac{U}{U + 1}\right)$$

$$Q = \frac{P + P \cdot S}{P + S + 1}$$

$$\beta = \frac{Q^2 + Q \cdot S}{\left(1 + \frac{1}{U}\right) \cdot P}$$

Loss at port 2, as a voltage ratio is: $dB2 = 20 \cdot Log(\beta)$

$$Rs = Zo \cdot S$$

$$Rt = Zo \cdot T$$

$$Ru = Zo \cdot U$$

All logarithms are to the base 10.

A calculator program is available to conveniently evaluate the design equations for any attenuation value and any characteristic impedance. Interested readers can find this program at the author's Web site: www.rfcascade.com.

Author Information

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