# Developments in Packaging: RFIC, MMIC, LTCC, SiP, SoC

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All electronic products are either getting smaller or becoming more complex in their capabilities. To achieve these twin objectives, circuits are now being packaged in a wide variety of miniaturized form factors. The first step in the process occurred many years ago with the evolution of integrated circuits from dual-inline packages (DIP) to SOIC, SSOP, TSSOP, etc. As surface-mount technology grew in popularity, numerous proprietary packaging options were developed for functional modules—mixers, oscillators, couplers, etc. Many of these modules are still in existence, but have been shrunk to the point where they are no longer "modules" but can be treated as individual SMT components.

Recently, packaging had taken two distinct paths—one for "conventional" building block components, the other for highly complex chips or multiple chip subsystems. There are some common elements, mainly in the board attachment methods: pads, solder bumps or solder balls. Differences are in the number of pins, and the physical enhancements needed for mechanical support in larger packages.

An area of significant development is thermal management. RF/microwave ICs do not have the same advantage of digital ICs regarding scaling of power consumption with size. Thus, smaller die and higher density circuits make it difficult to remove heat form areas where currents are concentrated. To address thermal issues, many recently-developed packages include exposed metal pads that provide heat dissipation via the PC board or an external heat sink. A major development is flip-chip technology, where the IC die is mounted upside-down. The substrate is attached to a heat spreader on the top of the package, which has lower thermal resistance than previous packaging methods. Also, the metal layer connections are much closer to the package's external connections, improving high frequency performance.

Advanced research work includes thermal enhancement using carbon nanotubes. An array of these structures can be used to conduct heat from the die, or from specific areas of the die, to a heat dissipating pad on the top or bottom of a package. With the short lengths involved, and encapsulation with a package, this is considered one of the most practical near-term applications for carbon nanotube technology.

To illustrate some of the recent developments in the packaging, we include the following news items:

| Package | Description |
|---|---|
| SOIC | Small Outline IC – 0.05 in. pitch |
| SSOP | Shrink Small Outline Package – 0.025 in. pitch |
| TSSOP | Thin SSOP – reduced vertical dimension |
| QFP | Quad Flat Pack – terminal pins four sides, pitch may be 0.4 mm to 1.0 mm |
| QFN | Quad Flat No leads – 0.5 mm pitch typical |
| LCC | Leadless Chip Carrier – usually high pin count, 0.7 mm pitch |
| BCC | Bump Chip Carrier – Solder bump version of LCC |
| BGA | Ball Grid Array – very high pin count package, 45 µm pitch typical. |
| LTCC | Low Temperature Co-fired Ceramic, accommodates a wide range of structure options |
| Flip-Chip | Die mounted substrate up, metallized top layer down — shorter distance from top-side connections to bumps or solder balls. Substrate may have top-side heat sink. |

Many specifications include pin count, e.g. SO-8, TSSOP-24, QFN-24, etc.

Many styles include sub-group or special material notations, e.g., TQFP (thin QFP), PLCC (plastic LCC), LBGA (low-profile BGA), etc.

Package choices are based on die size, operating frequency/speed, pin count requirements, plus size and cost considerations, including compatibility with existing assembly methods. Many IC products are offered with multiple package options.

**Table 1 · A partial list of major packaging types for RFICs, MMICs, multi-chip or system-on-chip devices.**

## LTCC Software to Speed Design

DuPont Microcircuit Materials (http://mcm.dupont.com), part of DuPont Electronic Technologies, and CAD Design Software have announced the integration of DuPont™ GreenTape™ low temperature co-fired ceramic (LTCC) materials and manufacturing processes into CAD Design Software's Electronic Design Automation (EDA) design tools for Ceramic (Hybrid/

MCM – LTCC) circuit design. By incorporating the widely used DuPont™ Green Tape™ 951 and 943 systems, CAD Design Software's Ceramic Design tool automates DuPont's recommended LTCC processes, and significantly improves cycle time for advanced circuit design.

The ability to select materials from CAD Design Software's Materials Library allows the user to setup custom technology parameters to begin a ceramic design or choose one from the list of preset technology files. The preset technology files have all of the DuPont recommended minimum entity widths and spacings incorporated for efficient design and manufacturing flow. CAD Design Software has incorporated many CAM tools for the ease of processing a ceramic design, such as nibbler data for removing cavity material in bulk or in steps, and control of the Gerber, hole and punch data for correct output to manufacturing.

DuPont Microcircuit Materials has over 40 years of experience in the development, manufacture, sale, and support of specialized thick film compositions.

## Fine Pitch Bump Adapters for Alternate ICs

Aries Electronics (www.arieselec.com) has launched a new series of adapters that enable the use of virtually any SMT IC device on a pitch of 0.4 mm or higher on PC boards with 0.5 mm pitch. These are ideally suited to adapting an IC device to some of the more popular TSSOP and QFP packages on 0.5 mm pitch. This adapter will enable the user to solder a BGA or other SMT device to pads on the component side of the adapter, which will then connect through the adapter to the 0.5 mm pitch raised connection pads (up to 0.010") on the bottom. The connection scheme comes standard in a pin 1-to-pin 1 routing, but can easily be customized to accommodate virtually any connection requirement.

The Aries Fine Pitch Bump Adapter boards are fabricated from 0.032" thick FR4 or Rogers 370 HR, with 1/2 oz. copper traces on both sides. The NSMD pads are finished with ENIG. The adapters operate at up to 221°F (105°C) for FR4 versions and 226°F (130°C) for the lead-free version. They are available in a panelized form for easy pick-and-place assembly of the new device, as an adapter only, or as a complete, turn-key solution with devices mounted.

## 3-D Packaging Initiative

Rohm and Haas Electronic Materials (www.rohmhaas.com), a supplier of materials for semiconductor packaging, has entered into a joint development agreement with IBM to develop and evaluate new materials for emerging packaging technologies. The agreement will focus on the evaluation of photoresists and supporting ancillaries, and low-temperature photodielectric materials for IBM's 3D packaging technologies. Rohm and Haas and IBM will also develop new materials for wafer-level and capillary underfill applications.

The joint collaboration will be performed at IBM's T. J. Watson Research Center in Yorktown Heights, NY, and at Rohm and Haas Electronic Materials' Technology Center in Marlborough, MA.

## New Leadframe Technology from DNP

As manufacturers attempt to cut costs, chips are becoming smaller and smaller. Because there is a limit to how short bonding wires can get as chips become smaller, it is necessary to stretch the inner lead to reach the chip. As a result, demand for even finer pitches on the inner lead becomes inevitable. It is believed that the existing minimum lead bonding pitch is 0.17 mm. If chips become any smaller, it is feared that it will become difficult to continue using leadframes, which are very inexpensive for packaging. In response, DNP Electronic Device (www.dnp.co.jp) has developed and begun mass production of a new leadframe, called New-LF, using an innovative process that makes use of DNP half-etching and taping technology.

New-LF is created using selective half-etching on only the fine pitch areas. By doing this, DNP can achieve a fine pitch of less than 0.15 mm without having to make the entire material thinner. The use of this method will enable the future incorporation of 0.18 micron chips and allow for even shorter wires in existing products. As an example, DNP will be able to shorten the wire for each lead on a 60 micron LSI pad pitch, 256-pin QFP to a length of just 4 mm.

## Thermally Enhanced Packages

In late 2008, StratEdge (www.stratedge.com) introduced a new family of small outline thermally enhanced molded ceramic packages for power semiconductors. The new line of packages can be used for silicon, silicon carbide, gallium nitride, and other compound semiconductors in power integrated circuit applications. Specific devices include amplifiers, discrete transistors, and diodes where greater than 0.5 watt power is consumed.

These thermally enhanced packages are designed for reliability and to mitigate the inherent stresses of brazing dissimilar materials together. All materials used in the packages have matched coefficients of expansion. They are assembled using a glass-to-metal seal process combined with gold germanium brazing, resulting in a rugged and reliable package. The packages can handle temperatures up to 360° C. A hermetic seal provides enhanced reliability for the device and offers protection from harsh environmental conditions, meeting military standard requirements.

The packages incorporate copper composite bases or copper inserts for enhanced thermal dissipation. Devices are mounted directly to the metal bases thus providing excellent electric ground to the backside of the chip. They provide superior electrical performance for frequencies up to at least 6 GHz. Packages are available in various shapes, sizes, and lead counts. All can be provided with gull wing-shaped leads for surface mounting.

## Summary

As this report illustrates, the importance of device packaging means that it is receiving much research and product development attention. Some work is unique to high frequency applications, but there is also much that can be shared with high-volume digital circuits.