A Constant Mismatch Analysis of Power RF Transistors Using EDA Tools

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This article presents a method for analyzing RF device behavior under mismatched conditions which may occur during the operation of a power amplifier system

The proliferation of EDA tools in the RF industry mainstream has narrowed the traditional separation between RF device designers and the users of those devices. The availability of accurate nonlinear large signal models demonstrate device characteristics by simulation rather than performing tedious, expensive or time prohibitive measurements. Thus, RF device designers and users are more easily able to arrive at a common understanding of an application specific result.

Generally, introductory EDA users rely on the embedded circuit analysis templates to provide information on a particular device behavior, but sometimes it is desirable to develop a custom simulation circuit. An example of a custom EDA circuit development is presented here, using Agilent's EEsof Advanced Design System.

Analysis with Mismatched Loads

Most RF power transistors, at some point during their lifetime, are subjected to non-optimum loads arising from a variety of situations. The transistor's active characteristics are dictated by these impedances and, in the least, affect the delivered power and dissipation. More specifically, drain load conditions are often defined in terms of VSWR and any mismatch presented to the high impedance side of a matching network, generally 50 ohms, results in the same variation about the optimum drain load impedance. Figure 1 shows a basic example of an impedance matching net-
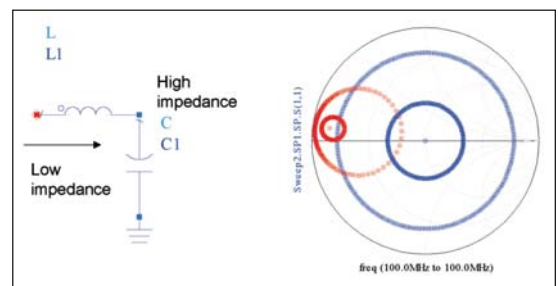

Figure 1 · Mismatches applied to the 50 ohm port will also appear at the device.

work with several VSWRs applied to the high impedance port and its subsequent effect at the low impedance port. The circles are high and low impedance 1:1, 2:1 and 8:1 VSWR. Thus, any mismatch present at an amplifier output is also presented to the device.

With respect to an RF power transistor, one might consider passive networks such as antennas, splitters, combiners or filters as simplified "black boxes." Often such passives are specified with a maximum VSWR. As an integrator of RF PA systems, it is desirable to know the active characteristics of a device having a constant mismatch from the optimum drain load. Usually the RF transistor's optimum series equivalent drain load impedance takes the form of R + jX, and in many cases the reactance is considerable.

Standard EDA embedded load pull analysis templates provide a means to simulate device characteristics such as constant gain, power compression and drain efficiencies using an impedance center and RHO radius of reflection coefficients [1]. However, these characteristics do not easily relate to performance into a constant VSWR.
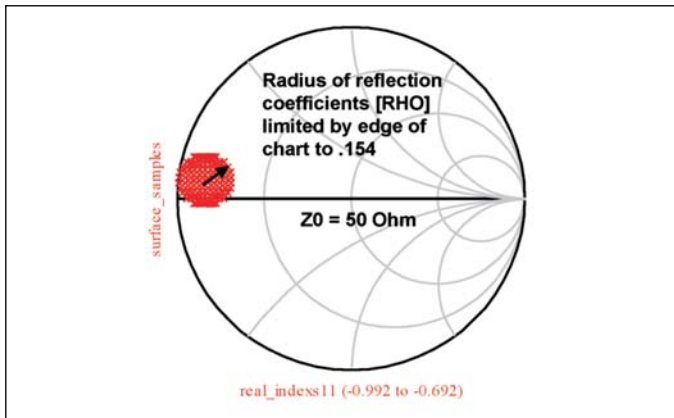
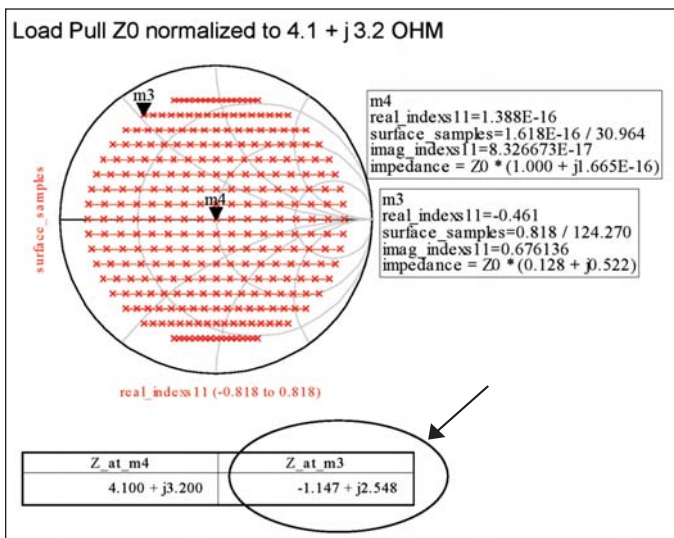Figure 2 · Complex impedance may not allow a 10:1 load pull.

Figure 3 · Attemping to normalize the sweep using a RHO radius results in negative impedances.

Figure 4 · Constant VSWR sweep from 1:1 to 10:1.
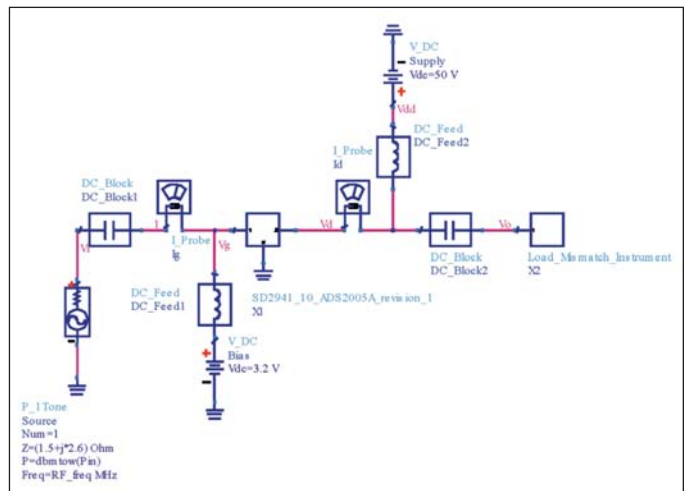
Figure 5 · ADS setup of the load mismatch instrument.

Figure 6 · Parameter sweep setup in ADS.

Using a complex impedance center of 4.1+ j3.2 ohms with the embedded load pull circuit template shows that a 10:1 load pull cannot be accomplished, as the radius of the reflection coefficients is reduced to prevent impedances from being negative (Figure 2). Trying to circumvent this by normalizing the Z_0 of the load pull sweep to the actual complex impedance using a RHO radius to give a 10:1 mismatch produces negative impedances (Figure 3, Z_at_m3). This can be calculated by the complex multiplication of the Z_0 and un-normalized impedances of marker 3, $(4.1 + j3.2) \times (.128 + j.522) = -1.15 + j2.55$. Sweeping around complex impedance in terms of RHO will not produce a constant VSWR in all cases.

A constant VSWR sweep around a complex impedance requires an EDA phase shifter tool, having a characteristic impedance set equal t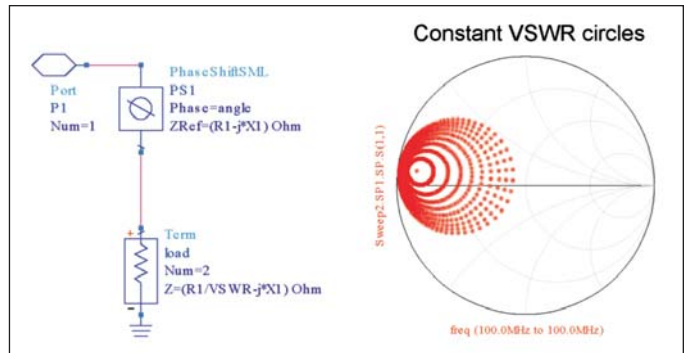o the optimum drain load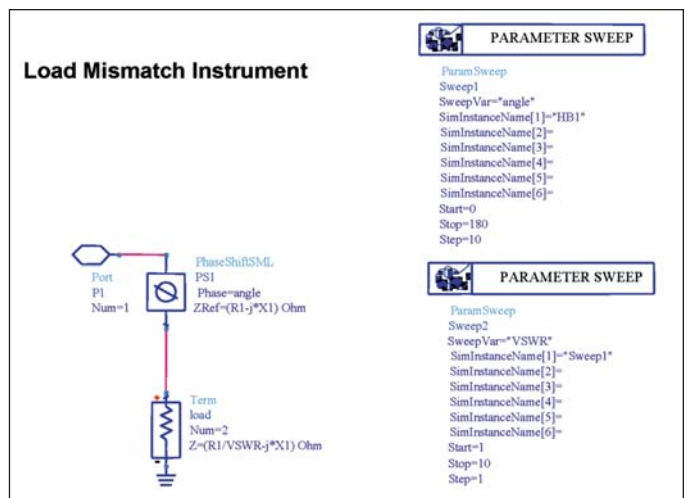, and a termination set equal to the required VSWR. Figure 4 shows a 1:1 to 10:1 constant VSWR all phase angle sweep around 4.1 + j3.2 ohms. In practice, an RF power combiner may have a maximum input VSWR specification of 2:1,
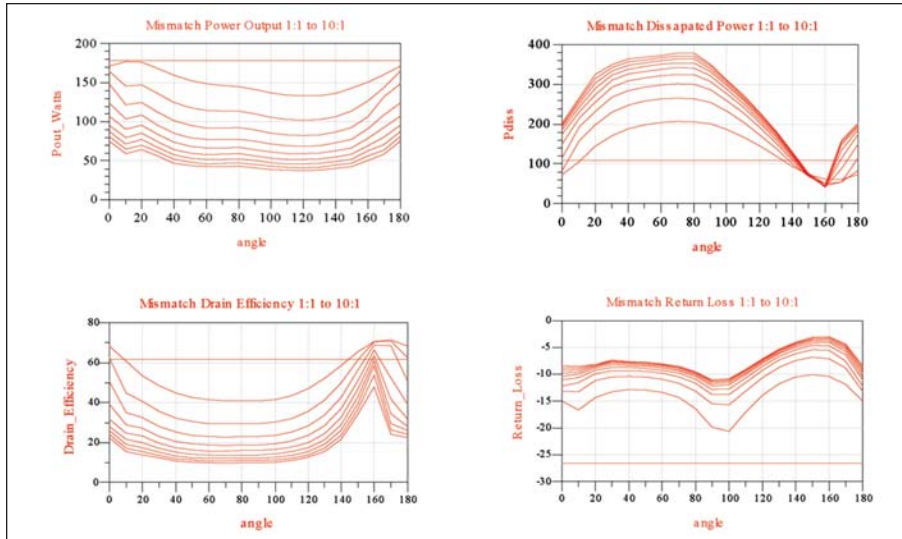
Figure 7 · Plots showing analysis results for a SD2941-10 RF MOSFET.

but a snapped-off antenna may present a 10:1 VSWR, including the losses of the cable.

An example analysis is presented using an SD2941-10 RF MOSFET model, which, not coincidentally, has an optimum 100 MHz drain load impedance of 4.1 + j3.2 ohms. Figures 5 and 6 depict a large signal EDA circuit with the load mismatch instrument's associated components attached to the device's drain terminal. The relevant large signal constant mismatch device behavior is shown in Figure 7.

Application of the Technique

With relative ease, the load mismatch simulation instrument provides RF and PA system designers rapid feedback for a variety of applications. For example, a designer might need to estimate the change of power dissipation for each device in a pair of combined transistors in order to take precautions against exceeding maximum ratings, or to choose an adequately rated product for a more robust design.

A second potential use for a rapid simulation tool would be to tailor the phasing of an expected failure mode to ensure the device will see an impedance that results in minimum power dissipation. A further application would be to examine device performances with small perturbations of load VSWR around the drain load as a means of optimizing a circuit design for additional tolerance to mismatch conditions.

It is shown that constant mismatch analysis, when used with accurate large signal transistor models, provides RF and PA systems designers with valuable and rapid feedback for a variety of applications.

Reference

1. Andy Howard, "Load Pull Simulation Using ADS," white paper, Agilent Technologies, Santa Rosa, CA, www.agilent.com.

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Interested readers may request the Agilent ADS archived Constant Mismatch project file by contacting Serge Juhel, STMicroelectronics' RF Product Marketing and Technical Support Manager, by e-mail at: serge.juhel@st.com.