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Circuit Extraction Techniques Provide Faster Interconnect Modeling and Analysis

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This article introduces an EDA technique that automates the of analysis of complex interconnections in high frequency circuits and packages

Communications designers developing products with GHz frequencies and Gbps edge rates who are using traditional printed circuit board (PCB) signal integrity (SI) solutions are finding that while their designs behave well under virtual prototype or simulation scenarios, they are failing when migrated to build and test. Why? Because the design of the interconnects above 1 GHz is an increasingly important issue—no longer a second- or third-order effect that can be largely ignored. Due to both large-scale integration and higher operating frequencies, interconnects no longer operate as simple lumped RLC circuits and so the modeling and simulation of these high-performance and complex design inter-connections must be taken into account from the get-go. If not, designers find themselves spending excessive time and money on redesigns and re-spins, and experimenting on the test bench, which adds cost to the final products not only with additional "fix-it" components, but ultimately in lost market window opportunities.

The new Microwave Office® 2007 Design Suite from Applied Wave Research, Inc. (AWR®) introduces innovative circuit extraction technology developed specifically to deliver productivity benefits to the designers of today's complex, next-generation communications products. This novel circuit extraction design approach, coined ACE™ for Automated Circuit Extraction, dramatically reduces from hours to seconds the time required to do the initial modeling of complex interconnects. In addition, it enables the designer to perform interconnect modeling at the earliest stages of the design flow, where problems can be identified and corrected before costly and time-consuming redesigns are required. These benefits deliver a higher degree of confidence in less design cycle time, ensuring that products will be volume manufacturable, cost-effective, and achieve their market window of opportunity.

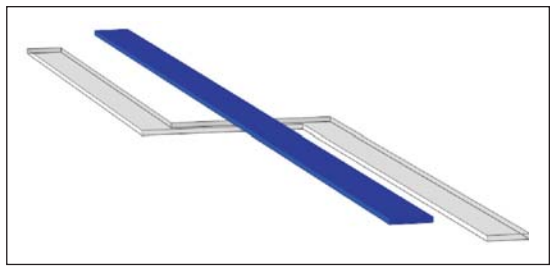

Figure 1 · A simple interconnect crossover of layer one (blue) over layer two (gray) on a four-layer FR4 module.

The AWR circuit extraction technology enables designers using Microwave Office software to leverage layout-based models for circuit extraction as opposed to traditional schematic based designs/flows. It provides a dramatic and revolutionary methodology shift to layout-driven simulation through a sophisticated mechanism for automating the bookkeeping and partitioning of structures into pre-existing models. The introduction of this technology is ground-breaking in that productivity is enhanced further through the use of AWR's Intelligent Net™ (iNet) schematic-layout interconnect automation technology. This capability is ideal for RF/microwave designs where the modeling of interconnects is not well suited to traditional circuit-based

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CKT
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        TandC=0.        HC=700. HB=0.25 T={27.,27.}     Rho=0.86281     Cover=1 Gnd=0
        SW=0.   Name="SUB24"    SWRight=0.      SigmaC=0.       Sigma={2.5e-002,1.7e-002}
        RhoV={0.86281,0.86281}
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        CL1=1   CL2=2
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        SaveToFile=0    FileName=""     W1=160. W2=160. Offs1=0.        Offs2=360.
        CL1=1   CL2=2
MLIN    12      15      ID="11" W=160.  L=80.   MSUB="SUB21"
MBENDR  7       8       ID="12" W=160.  MSUB="SUB25"
MLIN    9       11      ID="13" W=160.  L=280.  MSUB="SUB25"
MBENDR  9       10      ID="14" W=160.  MSUB="SUB25"
DEF4P   1       2       3       4       ExtractedNetlist
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Figure 2 · A netlist created in ACE representing interconnects in Figure 1.

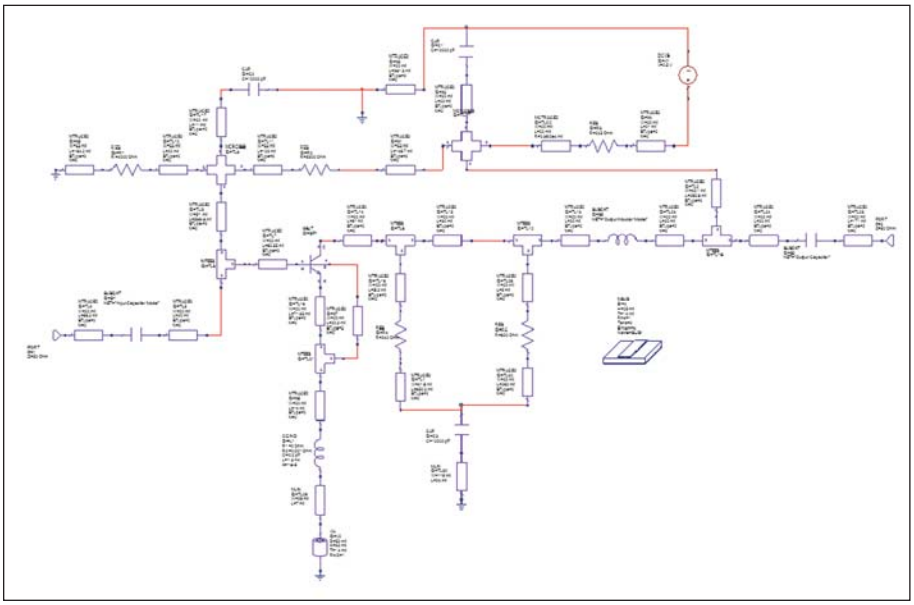

Figure 3 · A microwave-style schematic with explicit microstrip for routing and initial modeling.

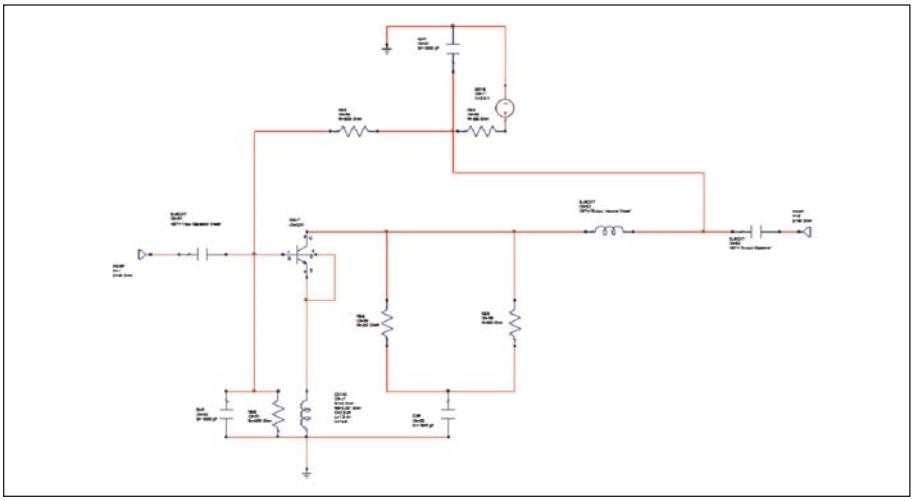

Figure 4 · An RF-style schematic.

approaches, or where the interconnects are parasitic and dense, yet critical to overall product performance. The ACE technology, which is similar to parasitic extraction techniques for digital and analog designs, is orders of magnitude faster than the traditional EM methods normally used for RF/microwave interconnect extraction because it groups interconnects together and effectively creates a schematic model using distributed and coupled-line circuit elements. Similarly, rather than using generalized finite element method (FEM) or method-of-moments (MOM) solvers designed for arbitrary arrangements of geometries, many of these circuit elements leverage highly optimized EM solvers, providing a tremendous speed advantage.

This article will discuss the features and benefits of the new AWR ACE technology and will provide examples of how the software can be easily and practically applied in the design of communications products. Designers who embrace this technology are able to more proactively address interconnect issues up front in the design flow and with comparable accuracy and greater speed, when compared to traditional back-end EM methodologies.

ACE—What is it?

ACE, at its heart, would be described as a circuit extractor by most of the digital and analog-mixed signal design community. The technique is not well known to the RF/microwave world because it has traditionally been used with RC models of the interconnects-corresponding to a low-frequency view of interconnects. The ACE software's breakthrough is to combine high-frequency sensibilities in the way the geometries are viewed by employing proven distributed models from many years of successful microwave and millimeter-wave designs.

Inherent in the technology is a necessary awareness of the current

return path. Low-frequency extraction techniques nominally ignore the consideration of a "ground" and leave it up to the user or simulator to determine current return paths after the fact. The consequent of such an assumptive approach is that the result is unreliable or unrealistic. The ACE software inherently understands the current return path and incorporates its dynamic change automatically in the generation and selection of multiple substrate definitions for the same integrated circuit (IC), module, or PCB technology.

Unlike traditional EM solvers, the ACE technology creates frequency-dependent circuit models from geometric structures without the need to directly solve Maxwell's equations. Coupled multi-layer lines (Figure 1) are analyzed for their length, width, layer, and position of each segment relative to every other segment on all the other lines.

Based on user-specified criteria, this analysis generates a circuit-based netlist (Figure 2) containing distributed models for all of the interactions among the interconnects: coupled lines, discontinuities, crossovers, vias, and independent segments. The speed improvement over the traditional method of directly solving Maxwell's equations with a generalized three-dimensional (3D) volume or planar solver is dramatic—as much as 1000x or more—because the solution is first approached by reducing the complexity geometrically, identifying coupled-line configurations and other grouped structures. Modeling of these structures can then be done with optimized EM solvers in critical areas. The accuracy is determined by the models to which the geometric structures are mapped and the applicability of the user-selected criteria for issues such as coupling distances and minimum line lengths. These models are useful in linear and nonlinear frequency-domain simulation as well as time-domain simulation, such as HSPICE.

ACE—What's the Benefit?

RF-Style Schematic

Typical RF/microwave designs would explicitly define all of the interconnects in the schematic, as shown in Figure 3.

This approach requires significant effort on the part of the user, not only to capture the schematic topology, but to ensure that each line length, bend angle, etc. is accurately accounted for and represented in the layout. While this enables the use of distributed circuit modeling (microstrip and stripline lines, bends, discontinuities, etc.) in order to obtain first-order performance of the interconnects, it ignores the coupling and parasitics. Initial distributed effects are easily captured in this approach, but finding all of the couplings becomes a bookkeeping nightmare, especially as segments are often added to individual routes later in the design.

In another approach, many designers forgo this step and go straight to layout, expecting to generate an extensive and intensive amount of EM-layout iteration in order to achieve the right design. In this case, the designer has already decided the metal is not driving the overall circuit performance and is simply parasitic. The corresponding schematic contains no distributed elements in the interconnects (Figure 4). The design achieves the second-order couplings much more quickly than in the former approach, but the primary effect of the interconnects must wait until the entire circuit is run through a generalized EM solver late in the design flow process, where work-arounds and fixes are more costly and time-consuming to make.

For the case of a microwave-style design, the user needs to put in all the microstrip-stripline explicitly. AWR's ACE software effectively eliminates this requirement with the mechanization of routable, meandered microstrip lines including

curved, mitred or differential. Even with this automation, however, the schematic is still cluttered with elements whose sole purpose is to route lines. But what happens when there is significant interconnect coupling such that putting in coupled line models adds so much more complexity to the situation that the designer can't see where all the couplings are?

Layout Automation and Incremental Modeling

AWR's iNet technology is used to automate layout implementation of the interconnects as represented on the schematic by wires. A layout net, represented as a rat's nest, is selected in the layout and then routed (Figure 5a). The user simply clicks the path from component-to-component and the line is routed using specified default vertical and horizontal routing layers and widths (Figure 5b). Layers are changed using the mouse wheel, and route widths and via types can be changed globally or segment-by-segment. Vias are generated automatically in any technology—RFIC, monolithic microwave IC (MMIC), PCB, low temperature co-fired ceramic (LTCC)-by parametric cell generators using technology-specific, design-rule-correct data from the user. Typically iNet routing takes less then one-tenth the time of explicitly defining microstrip lines, bends, crosses, and tees, and about one-half the time as using paths and manually-inserted vias. The ACE method can be done on the single route (Figure 3), the completed design (Figure 6), or anywhere in between.

In other words, the ACE technology can be implemented at any time during the formation of the schematic; the user does not need to wait until the design is completed, captured, and laid out. Small sections of the design, such as bias circuitry or control lines, can be analyzed individually and then combined with larger portions of the design as it matures. ACE structures can be instantly re-analyzed during final design verification with any EM solver connected to AWR tools through AWR's EM Socket™ open industry standard interface for the direct integration of popular EM solvers into the AWR design environment. The iNet's automation and EM Socket open integration speeds design completion because all EM solvers can share the same structures that the ACE software uses: going from ACE to any EM solver simply requires "clicking" to select the solver(s) of choice.

Flexibility of Model

Mapping of geometric structures to appropriate circuit models in the ACE software can be specified to tune for accuracy and speed. The technology operates fastest when it does not use any models with built-in EM solvers; in this mode it uses traditional closed-form models for microstrip and stripline couplings. Changing from closed-form models to EM quasi-static models improves accuracy, but takes additional time as the ACE product now maps coupled line structures into AWR's specific model set, which is capable of modeling all practical coupled line configurations using built-in EM quasi-static analysis. The 2D cross-sectional EM solver inside this model is solved at one frequency point and then scaled over the entire frequency range. The ACE technology is most accurate when used with AWR's model set that employs FEM techniques solved at each frequency.

Other geometric structures can be similarly controlled. Junctions and discontinuities can be modeled with closed-form models, such as T-junctions. If greater accuracy is required, AWR's X-models can be used, providing EM accuracy at circuit-model speed by using pre-calculated EM-based tables for the specific arrange of dielectrics in the design.

Vias can be explicitly modeled in numerous ways. *S*-parameter files from measured or simulated data can be specified for each via type. The iNets feature supports multiple via types for any given layer-to-layer transition and the ACE software is able to identify the unique structure and its *S*-parameter dataset. Alternatively, ACE technology can use a closed-form model to netlist the via based on the geometric descrip-

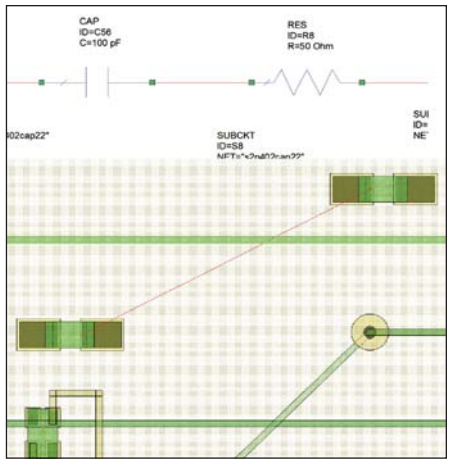

Figure 5a · A schematic and pre-route layout showing a rat's nest between a surface-mounted capacitor and resistor.

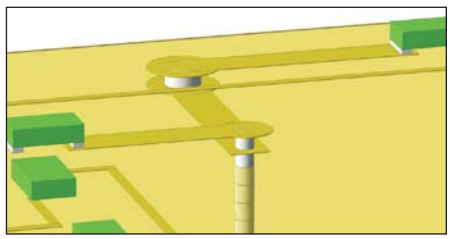

Figure 5b · A completed route, with the default via in the background changed from thru-via to blind.

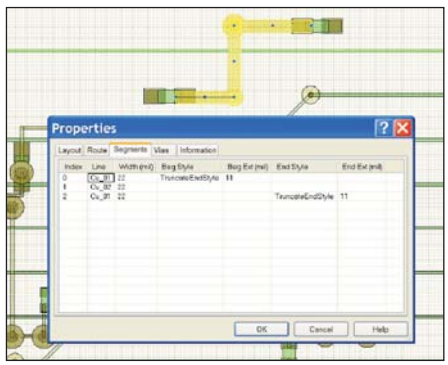

Figure 6 · A route segment/via properties dialog box.

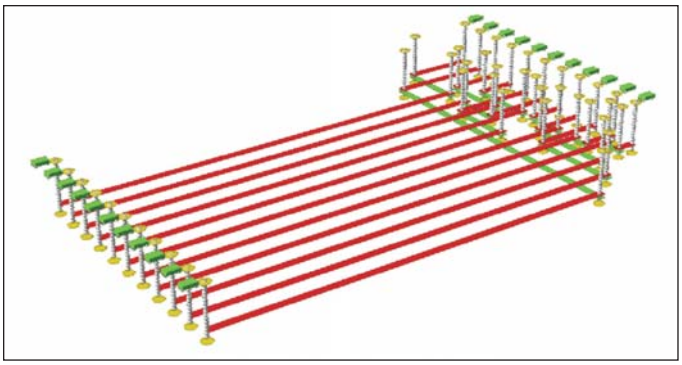

Figure 7 · The ACE technology solves this 16-layer PCB structure 1000x faster than EM solvers.

tion of layers, pads, and drill holes. If the user provides neither *S*-parameters nor specifies a closed-form model, the ACE software will default to the use of a simple RLC model of the via.

Speed

When using the most accurate of EM-based models, the ACE product's speed is the result of reducing the size of the EM problem to one where highly optimized EM solvers can be brought to bear on much smaller structures. In this mode, the software performs at 1000x or more than traditional, generalized EM solvers. The rather simple control line structure on the 16 layers of FR4 shown in Figure 8 takes approximately four hours for 200 frequency points with a 3D planar MOM solver, but less than 10 seconds using the ACE methodology.

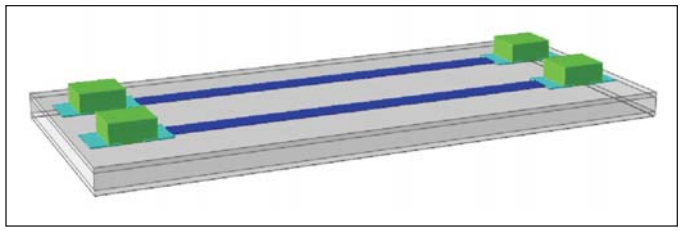

Figure 8 · A four-layer module coupled line.

Accuracy

Fast extraction is useful early in the design flow, becoming less so as the design solidifies and often demands greater accuracy. Since the ACE software uses distributed models (X-models derived with EM) and EM-based models with optimized, built-in EM solvers, it sustains accuracy much later into the flow and at a higher frequency. For a simple coupled line structure (Figure 8), ACE broadband models provide better than 0.1% accuracy from DC to 20 GHz (Figure 9) in a matter of seconds.

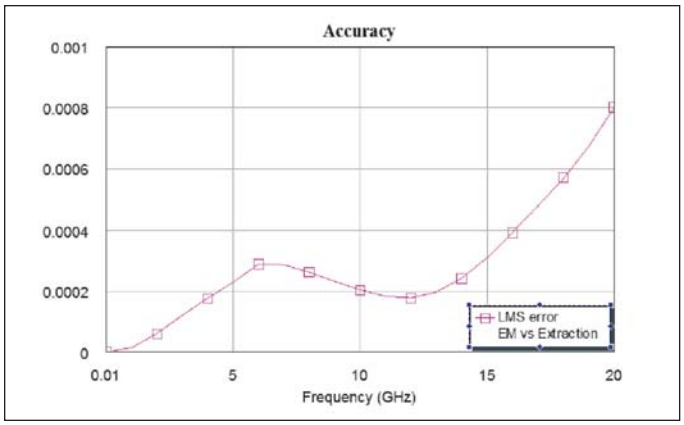

Figure 9 · ACE leveraged EM is 0.1% accurate up to 20 GHz and beyond.

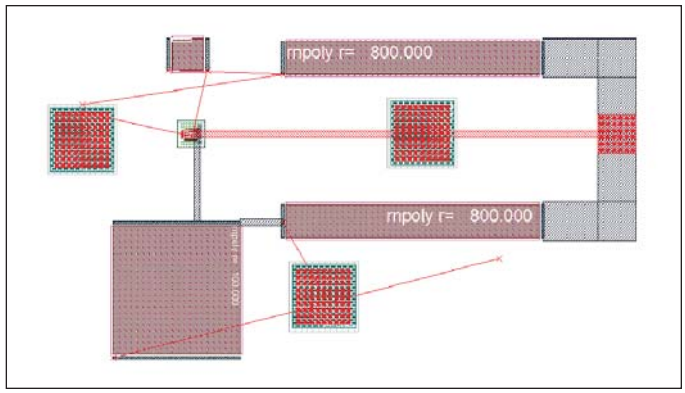

Figure 10 · The very early part of the layout in a MMIC design with multilayer interconnect routing completed in the left part of the circuit.

IC Example

Silicon, gallium arsenide (GaAs), or other IC technologies can benefit from AWR's ACE technology. Designs where interconnects are not explicitly captured, such as in Figure 3, are ideal candidates for this unique and novel AWR approach. Circuit designers would choose this design capture method, with no explicit interconnect modeling, when the components themselves dominate design performance. At frequencies above one GHz, the interconnects degrade the component-based performance and must be included prior to final design verification. ACE software enables fast, incremental consideration of these parasitics so that component values design centering can be done with respect to each interconnect as it is added. In contrast, it is much more challenging to do this at the final verification stage with large S-parameter files and shrinking timeframes prior to tapeout.

Module Example

Form factors and space severely constrain interconnect routing for power amplifier (PA) modules and front-end modules for handset applications. The ACE methodology is ideally suited to handle the combination of signal path, control lines, and bias interconnects. The interconnect from PA to coupler needs a few nH of inductance for a better match, so the user can nominally design this particular ACE model (Figure 12) and then later in the design flow, reassess the impact of the PA control lines (Figure 13). Before adjusting the interconnects, the impact can be viewed (Figure 14) and addressed by modifying either the signal path or the control lines.

PCB Example

EM analysis of multilayer PCB technology can be extremely time-consuming, especially when there are non-uniform thicknesses and varying dielectrics. The ACE approach cuts through these issues and provides fast, reliable, and repeatable results while designing and analyzing the design. The 16-layer PCB example shown in Figure 15 has a signal path on the upper two layers with a ground plane immediately below them, and control lines on layers 14 and 15. Through, buried, and blind vias are used. The effect of removing the ground on layer three and using the ground above the PCB is evidenced in the differences between the input match and through performance (Figure 16).

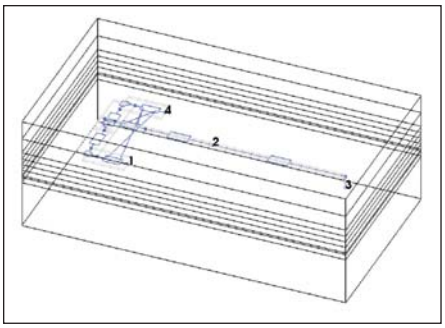

Figure 11 · A 3D extracted view of the interconnect showing three coupled lines and distributed line models.

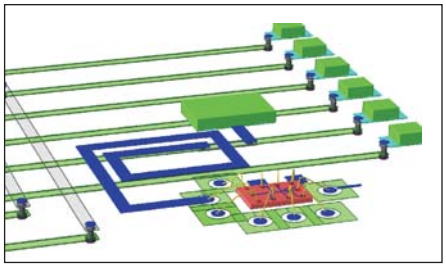

Figure 12 · A wirebonded and co-designed silicon germanium (SiGe) PA chip with the signal path (blue/pink spiral) on layers one and two and control lines on layers two and three.

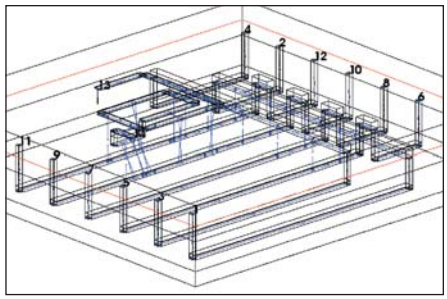

Figure 13 · ACE results show extensive coupling between the signal path and control lines (reverse view from Figure 12 for ease of visualization).

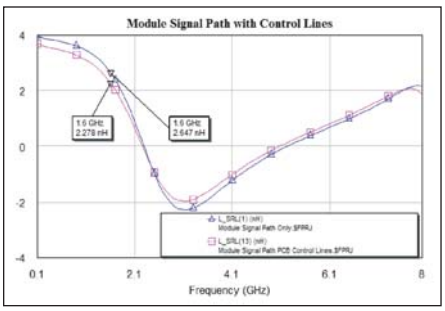

Figure 14 · Effective signal path inductance—the module control line coupling causes parasitic reduction in signal path inductance.

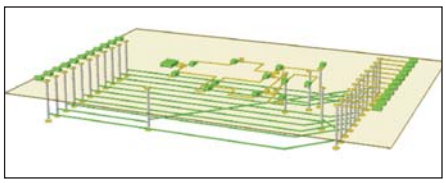

Figure 15 · A 16-layer PCB example shows the signal path on the upper two layers with a ground plane immediately below them, and then control lines on layers 14 and 15.

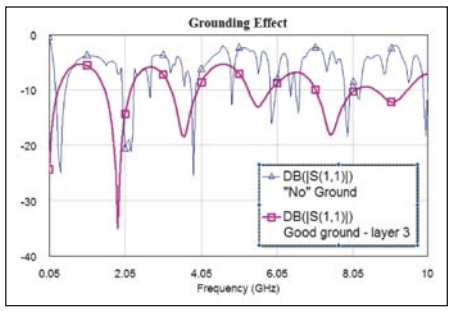

Figure 16 · ACE correctly shows the effect of removing the ground on layer three and using the ground above the PCB, as evidenced in the differences between the input match (blue) and through performance (pink).

Summary

The features and benefits of the ground-breaking new ACE automated circuit extraction technology have been showcased in this article, and examples of ways in which users can employ this technology to streamline and optimize their design flows have been presented. ACE has been shown here to provide comparable accuracy at 100x to 1000x speed improvement over generalized EM solvers when used during design and analysis. AWR has a rich tradition of leveraging its considerable experience in microwave design in order to provide innovative EDA solutions that dramatically improve design productivity and reduce product development costs for communications applications. The company has used its microwave expertise to deliver the ACE product by migrating the benefits of digital/analog circuit extraction technology into useful software for high-frequency design. The new software brings to the RF/microwave world the ability to model complex interconnects quickly and accurately, and, most importantly, to perform accurate and timely simulation and analysis early in the design cycle, before time-consuming design respins and costly hardware adjustments are necessary. Users of ACE software can be confident that this new technology will enable them to develop products more quickly and confidently, helping them take advantage of ever-smaller market windows.

Author Information

Dr. Michael Heimlich is currently AWR's Director of Product Marketing for Microwave Office and AWR SI. Mike received his BSEE, MSEE and PhD EE from the Renssalear Polytechnic Institute and joined AWR in 2001 as the Consulting Services Manager. Prior to joining AWR Mike was the Chief Technical Officer and founder of Smartlynx, where he was the chief architect for interoperability tools between various EDA tools such as ADS, Cadence, Mentor Graphics and Microwave Office. Prior to founding Smartlynx, Mike was co-founder of Vista Technologies, where he provided services and custom software to Mentor Graphics and its customers.

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