From June 2004 *High Frequency Electronics*

Jitter—Understanding it, Measuring It, Eliminating It; *Part 3: Causes of Jitter*

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Understanding and measuring jitter are important, but the ultimate objective is finding out what is causing excessive jitter, then reducing or eliminating it to achieve the desired overall system performance

This final article of this three-article series we discuss identifying jitter in the real world. In Part 1 we introduced jitter and its various kinds, in Part 2 we discussed jitter measurements, jitter measurements at high data rates and issues relating to the accuracy of jitter measurements. Now we move on to the task of identifying the causes of jitter.

Some real-time instruments can separate random and deterministic jitter components to predict/extrapolate worst-case total jitter (TJ) and eye-opening based on a user-specified Bit Error Ratio (BER), typically 10^{-12}. But when jitter measurements fail to meet a particular minimum standard, or if the results are "too close for comfort," then measuring the amount of component or system jitter is just half of the jitter test equation. Determining the root-cause of jitter is the other half.

The focus of this article is to provide practical "tips & tricks." In particular, we discuss how to employ real-time oscilloscopes with jitter analysis and high-speed pulse/pattern generators to separate and time-correlate specific deterministic jitter components.

Characteristics of Individual Jitter Components

In order to interpret measurement results and waveform views performed by real-time jitter analysis, you must first understand the characteristics and likely causes of individual jitter components. Knowing that Random Jitter (RJ) is Gaussian in distribution and Deterministic Jitter is non-Gaussian is a good beginning, but there is more.

Total Jitter is composed of a Random Jitter component and a Deterministic Jitter component, discussed in Article 1, and denoted in Figure 1. Random Jitter is unbounded, and it is for this reason (unlimited peak-to-peak) that it is usually measured in terms of an RMS value. In addition, Random Jitter is pre-

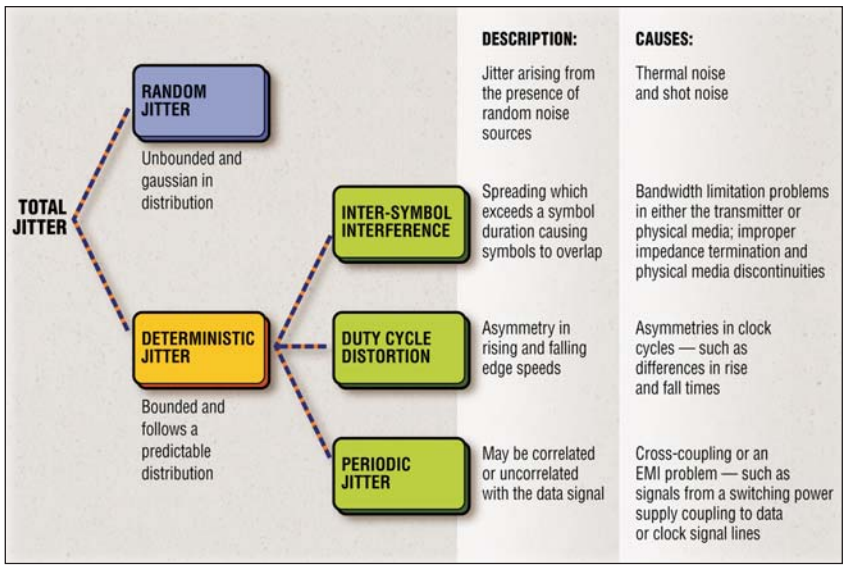

Figure 1 · Total Jitter is the sum of several components.

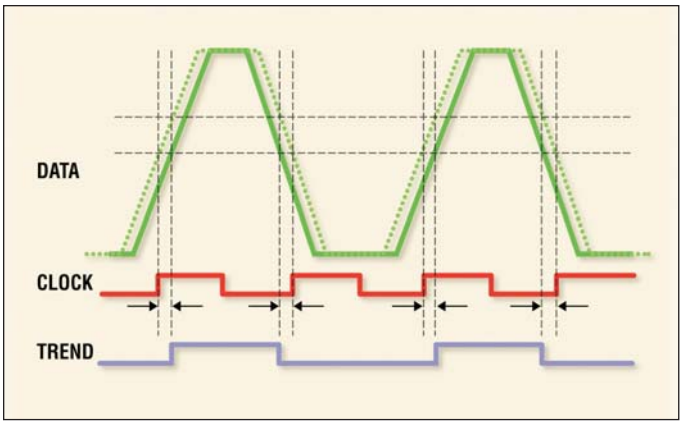

Figure 2 · Duty Cycle Distortion (DCD): The dashed green line represents a distorted output of a transmitter due to positive shift.

dictable in terms of distribution. Its probability distribution function is always Gaussian in shape.

Unfortunately, predicting the cause of random jitter is a more difficult task and is not within the scope of this article. Random Jitter is often caused by thermal effects of semiconductors and requires a deeper understanding of device physics. However, one piece of advice is to pay close attention to the amount of vertical noise in your system. Random vertical noise will directly translate into random timing jitter.

On the other hand, deterministic jitter is bounded and is always measured in terms of a peak-to-peak value. Although the distribution of deterministic jitter can be unpredictable, the likely causes and characteristics of the individual sub-components of measured deterministic jitter are very predictable. The sub-components of Deterministic Jitter consist of Duty Cycle Distortion (DCD), Inter-Symbol Interference (ISI), and Periodic Jitter, as shown in Figure 1.

Let's now take a closer look at possible causes and characteristics of each of the sub-components of deterministic jitter.

Duty Cycle Distortion

There are two primary causes of DCD jitter. If the data input to a transmitter is theoretically perfect, but the transmitter threshold is offset from its ideal level, then the DCD at the output of the transmitter will be a function of the slew rate of the data signal's edge transitions. Referring to Figure 2, the waveform represented by the solid green line shows the ideal output of a transmitter with an accurate threshold level set at 50% and with a duty cycle of 50%. The dashed green waveform represents a distorted output of a transmitter due to a positive shift in the threshold level. With a positive shift in threshold level, the resultant output signal of the transmitter will exhibit a duty cycle of less than 50%. If the threshold level is shifted negatively, then the output of the transmitter will exhibit a duty cycle that is greater than 50%.

Measuring Time Interval Error (TIE) relative to the software-generated best-fit clock (red waveform), results in a positive timing error on the rising edge of each data bit and a negative timing error on the falling edge of each data bit. The resultant TIE trend waveform (purple waveform) will possess a fundamental frequency equal to one-half the data rate. The phase of the TIE trend waveform relative to the data signal will depend on whether the threshold shift is positive or negative. With no other sources of jitter in the system, the peak-to-peak amplitude of DCD jitter will be constant across the entire data signal, at least theoretically. Unfortunately, other sources of jitter, such as ISI, are almost always present, often making it difficult to isolate the DCD component.

One technique to test for DCD is to stimulate your system/components with a repeating 1-0-1-0... data pattern. This technique will eliminate ISI jitter and make viewing the DCD within both the trend and spectrum waveform displays much easier. Using the jitter spectrum display, the DCD component of jitter will show up as a frequency spur equal to one-half the data rate.

Another cause of DCD is asymmetry in rising and falling edge speeds. A slower falling edge speed relative to the rising edge will result in a duty cycle of more than 50% for a repeating 1-0-1-0... pattern, and slower rising edge speeds relative to the falling edge will result in a duty cycle of less than 50%. Although not graphically shown in this paper, the results of jitter analysis and the TIE trend waveform will look similar to the results of the example illustrated in Figure 2.

Inter-Symbol Interference

ISI, sometimes called data dependent jitter, is usually the result of a bandwidth limitation problem in either the transmitter or physical media. With a reduction in transmitter or media bandwidth, limited rise and fall times of the signal will result in varying amplitudes of data bits dependent on not only repeating-bit lengths, but also dependent on preceding bit states.

In addition, improper impedance termination and physical media discontinuities will also result in ISI due to reflections that cause signal distortions. Although we will address these two phenomena—BW limitations and reflections—separately in this article as contributors to ISI jitter, in reality, waveform distortions due to reflections are also a bandwidth limitation problem. Shown in Figure 3 is an example of ISI due to bandwidth limitation problems. Limited bandwidth produces limited edge speeds, and limited edge speeds will result in varying pulse amplitudes at high-speed data rates. Varying pulse amplitudes will then result in transition timing errors.

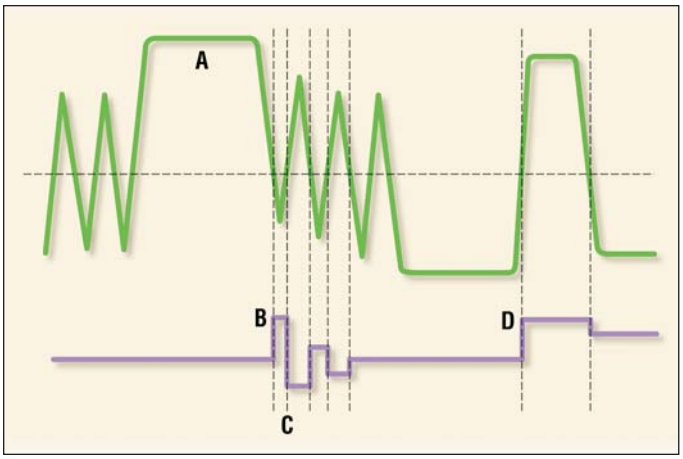

Figure 3 · Inter-symbol interference (ISI) due to bandwidth limitation problems.

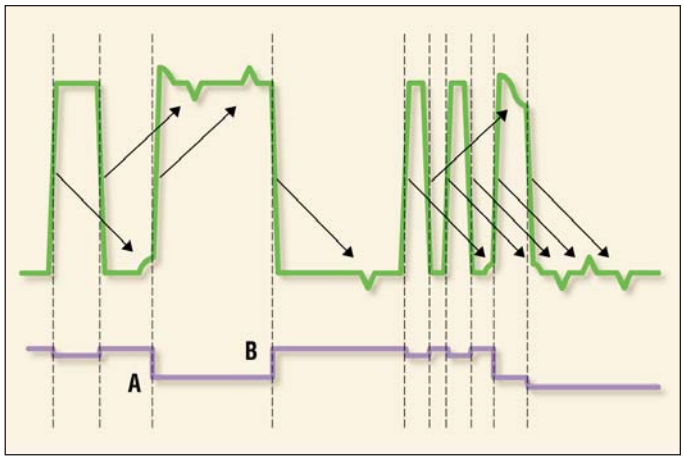

Figure 4 · Intersymbol Interference (ISI) due to signal reflections.

Let's examine this more closely:

With a long series of repeating "1s," the amplitude of the data signal will eventually rise to a full steady-state high level as illustrated by the long-high pulse at point **A** in Figure 3. When the state of the data changes to a "0," the signal will exhibit a relatively long transition time to reach the threshold level, resulting in a positive timing error. This will be manifested as a positive peak of timing error in the jitter trend waveform (purple) at point **B**. Note that this point on the jitter trend waveform is time-aligned with the negative data crossing point on the data signal.

The negative peak amplitude of the next "0" bit preceded by a long string of "1s" will be attenuated for two reasons: First of all, the preceding long string of "1s" means that the signal will take longer to transition to a true low level since the data signal starts from a higher initial level. Secondly, the following "1" bit causes the signal to reverse direction before it even reaches a solid low level. This reduction in signal amplitude will produce a negative timing error on the next transition to a "1" since the signal has a very short distant to travel to reach the threshold level. This is illustrated at point **C** on the jitter trend waveform in Figure 3.

The positive timing error illustrated at point D on the jitter trend waveform follows the same logic as the positive timing error at point B previously discussed. With a long string of "0s" the data signal has sufficient time to settle to a full steady-state low level. When this signal then transitions back to a high level, it again has a longer transition time to reach the threshold level, and hence produces a positive timing error.

The Unique Signature of Inter-Symbol Interference

Once you understand how bandwidth limitations produce ISI timing errors, it becomes more intuitive to understand the unique signature of the jitter trend waveform due to ISI and how it relates to the time-correlated serial data signal being measured.

In addition to bandwidth limitations, another common cause of ISI is signal reflections due to improper terminations or impedance anomalies within the physical media. Signal reflections will produce distortions in the amplitude of the data signal as shown in Figure 4. Depending on the physical distances between impedance anomalies, reflections produced by one pulse may not show up on a high-speed data signal until several bits later in the serial pattern. Notice which pulse the arrows begin on and where pulse distortion (reflection) occurs as illustrated by the end of each of the arrows in Figure 4.

If the amplitude of the signal becomes distorted on or near a data transition edge due to reflections, then a timing error may occur. If a signal reflection causes signal attenuation near the data edge, then a negative timing error will be detected since the signal will have less distance to travel when transitioning to the threshold level. This is illustrated at point **A** on the jitter trend waveform in Figure 4. If a signal reflection causes a boost in signal amplitude, then the result will be a positive timing error since the signal will have farther to transition to reach the threshold level. This is illustrated at point **B** on the jitter trend waveform.

ISI due to signal reflections can be very difficult to isolate and interpret. But if you have signal reflection problems in your system, it is likely that there is also a bandwidth limitation problem.

Periodic Jitter

Usually the result of a cross-coupling or EMI problem in your system PJ can be either correlated or uncorrelated to the data signal. An example of uncorrelated PJ would be signals from a switching power supply

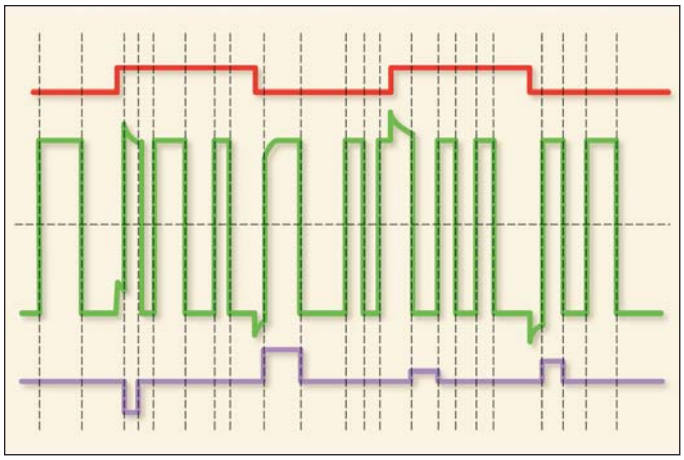

Figure 5 · Periodic Jitter (PJ) caused by capacitive coupling.

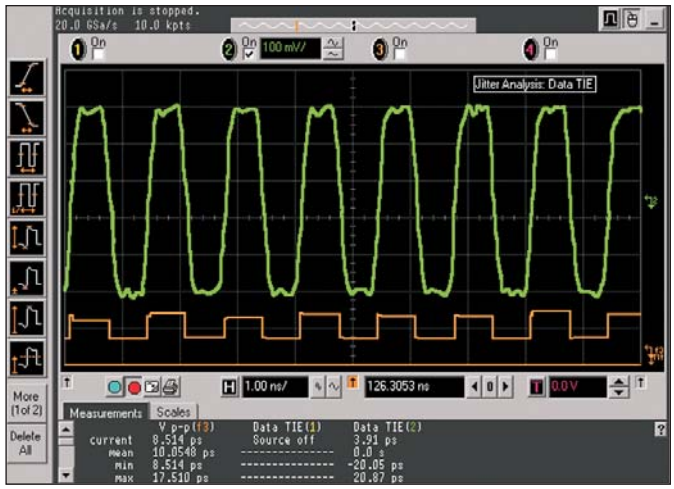

Figure 6 · Isolating Duty-Cycle Distortion (DCD).

coupling into the data or system clock signals. This kind of jitter is considered to be uncorrelated because it is not time-correlated with either the clock or data signal since it would be based on a different clock source. An example of correlated PJ would be coupling from an adjacent data signal based on the same clock—or a clock of the same frequency.

Shown in Figure 5 is an example of a "corrupter" signal (red trace) capacitively coupled to a serial data signal (green trace). This coupling will result in amplitude distortions on the data signal. Just like ISI due to reflections, if these amplitude distortions occur at or near a data signal transition, a timing error may occur.

Since most PJ will be uncorrelated with the data signal, any attempts to time-correlate the jitter trend waveform with the data waveform will be futile. As we will show later in this article, uncorrelated PJ can often be detected using the jitter spectrum view.

Isolating Jitter Components in the Real World

In the real world, jitter components are rarely isolated. If there are multiple jitter components contributing to the total system jitter in your system, you end up viewing composite results—which can be difficult to interpret. Fortunately, there are some novel stimulus-response techniques you can employ to isolate, measure and then view individual jitter components. Once you successfully isolate individual components, you can then often time-correlate worst-case peaks of jitter to specific data bit transitions and then use common-sense debug techniques to solve your jitter problems one jitter component at a time.

The primary tool to isolate jitter components is a real-time oscilloscope with responsive and interactive jitter analysis such as the 6-GHz Agilent 54855A. In addition, a high-speed pulse/pattern generator such as the 3.3-Gb/s Agilent 81134A can be very useful for generating known serial patterns of high-speed differential stimulus.

Let's now turn to some real jitter measurement examples using these two measurement tools.

Isolating and measuring DCD—One technique for isolating and measuring DCD is to stimulate your system/component with a repeating 1-0-1-0... serial pattern. This stimulus pattern will eliminate most of the ISI. Although ISI is eliminated with this repeating pattern, RJ and any PJ will still be present in the signal, which will contribute to convoluted measurement results. But there is also a measurement technique to eliminate both random jitter and uncorrelated periodic jitter in the jitter measurement results. Shown in Figure 6 is a captured serial pattern (green trace) of repeating ones and zeros. The jitter analysis results appear immediately below as the TIE trend waveform (pink trace).

To eliminate the random components (RJ and PJ), waveform math has been employed to average the jitter trend waveform. Before averaging, the TIE trend waveform would be "bouncing" vertically due to the random components with repetitive acquisitions. But averaging has eliminated the random jitter components to disclose a very stable trend waveform with an fairly constant level of peak-to-peak amplitude of jitter from cycle to cycle. We can then use the scope's manual markers or the scope's automatic parametric measurement capability to measure the peak-to-peak amplitude of duty cycle distortion. In this case, we measured approximately 10 picoseconds of DCD.

In addition to determining the level of DCD, we can also glean additional information about our measurement results. With the time-correlated display of the jitter trend waveform and data signal, we can see that the trend waveform is in-phase

with the data signal. This is an indication that the duty cycle of our pulse is less than 50%. Rising edges always occur late (+error), and falling edges always occur early (–error).

Perhaps our transmitter threshold level is too high, or perhaps the output of the our transmitter generates slower falling edge speeds as compared to faster rising edge speeds. At this point if we believe the peak-to-peak level of DCD is excessive, we can set up additional characterization tests to measure the duty cycle of each pulse in the data stream using jitter analysis.

In addition, if we suspect that the DCD is caused by asymmetry in the rising and falling edge speeds, we can then set up the instrument and jitter analysis to characterize each rising and falling edge in the data stream.

Additional Techniques—Reference [1] contains an example of isolating ISI that is caused by a system bandwidth problem. There is also a discussion of how to measure shape and frequency of designed-in modulation of serial data with spread-spectrum clocking.

Conclusions

Some real-time jitter analysis packages give answers in terms of the amount of total jitter that may be present in your system. (Agilent's jitter analysis packages are described in [2]). This can be important for determining if your high-speed digital system meets a particular worst-case jitter and eye-opening specification. But knowing how much random jitter and deterministic jitter is in your system usually doesn't give you a clue as to where it is coming from. The key to finding sources of jitter lies in the ability to time-correlate jitter measurement results with high-speed serial data signals, as well as with other possible sources of uncorrelated periodic jitter. A real-time oscilloscope with jitter analysis along with the stimulus-response techniques described in this article meet that critical time-correlation requirement to relate jitter trend measurement results to measured signals. Once you are able to time-correlate particular real-time timing error measurements to particular bits within a serial data pattern, it usually becomes a routine troubleshooting task to solve your deterministic jitter problems.

References

1. *Finding Sources of Jitter with Real-Time Jitter Analysis*, Agilent Technologies Application Note AN1448-2, www.agilent.com

2. *Jitter Solutions for Telecom, Enterprise and Digital Designs*, Agilent Technologies Product Note 5988-9592EN, www.agilent.com

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Parts 1 and 2 of this series on jitter appeared in the April 2004 and May 2004 issues of *High Frequency Electronics*. These articles, as well as all past technical articles and columns, are available online at: www.highfrequencyelectronics.com

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