# Building a Microwave Frequency Synthesizer— Part 3: From Sketch to Product

## By Alexander Chenakin Phase Matrix, Inc.

This series continues with a step-by-step review of the design sequence, from basic diagram and specifications to production Development of a new product usually starts from an idea or concept, followed by several design steps. In this article, a simple single-loop PLL

example is used to demonstrate the most important aspects of the design process, beginning with a specification and block diagram, then proceeding to schematic, PCB layout, assembly, troubleshooting, testing, and documentation release.

### **Specification**

A specification is a set of requirements that have to be met by a product. It can be generated through market research identifying particular customer needs and market demands. Alternatively, it can come from a customer, sometimes in a form of a "wish list." The requirements are analyzed and then gradually nailed down to a formal document that establishes all parameters describing the product. As an example, let's consider a customer who needs a signal between 5 and 5.5 GHz to be used as a stimulus source for some experiments. Although the requirements have not been completely defined, some desirable characteristics are as follows:

Frequency Range: 5.0-5.5 GHz Resolution: 1 MHz Tuning Speed: 1 msec Output Power: +7 dBm Spurious: -60 dBc Harmonics: -25 dBc Phase Noise: -90 dBc/Hz at 100 kHz offset External Reference Frequency: 10 MHz The synthesizer should come in a connectorized metal box and be programmed to any desired frequency within the indicated frequency range and 1 MHz step size using a personal computer. The 10 MHz reference is from the customer's own equipment.

Obviously, the specification is not complete; however, we have enough information to start defining the synthesizer architecture and selecting its main components. Other parameters can be marked as TBD (to be determined)—that gives us some flexibility at this stage, and those parameters can be analyzed and negotiated later in the process.

#### **Block Diagram**

A block diagram is a high-level pictorial model of a product that helps to understand the overall design concept. Taking a quick look at the indicated above parameters, one can conclude that the spec is straightforward: a single-loop PLL should probably do the job.

What components should be used? First of all we need a VCO. Hittite's HMC430LP4 seems to be an excellent candidate. It provides the desired frequency coverage and is available in a low-cost, surface-mount form. Moreover, we can also rely on the VCO freerunning noise at 100 kHz frequency offset, which is better than -100 dBc/Hz [42]. We also need PLL components (phased detector, dividers) to lock the VCO. Analog Devices' ADF4106 should be a perfect choice. The part supports the required frequency range and includes a digital phase-frequency detector, both RF and reference dividers as well as lock detector circuitry [43]. All division coefficients are programmed through a built-in 3-wire serial interface. The part also allows program-

# High Frequency Design SYNTHESIZER DESIGN



Figure 28  $\cdot$  A simple block diagram sketch is the usual starting point for synthesizer design.

ming the phase detector charge pump current to adjust PLL loop filter bandwidth if required. This is an especially useful feature for broad bandwidth synthesizers, since the VCO tuning sensitivity and the loop division coefficients may change with frequency.

Now we can draft a very simplified block diagram sketch like the one shown in Figure 28, which helps to quickly estimate some key design characteristics, such as phase noise, loop bandwidth, and tuning speed. According to the ADF4106 data sheets, the effective phase detector noise at 1 MHz comparison frequency is about -159 dBc/Hz. Assuming that PLL noise dominates (that means the external reference noise is sufficiently low), we can estimate the RF output phase noise generated by the PLL itself at -84 dBc/Hz. Since the VCO free-running noise at 10 kHz frequency offset is worse, the PLL bandwidth should be set slightly above 10 kHz (let's say 20 kHz) for optimal phase noise performance. The tuning speed corresponding to this loop bandwidth is in the order of 200 microseconds for a 45-degree phase margin. This should be verified with your choice of simulation methods.

Now, it is probably a good time to contact the customer again to discuss the characteristics we can potentially achieve (some margin should be added, of course) and clarify other parameters such as external reference phase noise. Then, we come back and proceed with the block diagram.

What else are we missing? The VCO tuning curve indicates that we need about 7.5V to steer the VCO to 5.5 GHz. However, the maximum voltage provided by the phase detector output is only 5.5V. Thus, an operational amplifier (such as AD820 by Analog Devices) should be added to scale up the charge pump output. Moreover, we also need to boost the VCO RF output in order to get the



Figure 29 · A block diagram with additional operating information.

desired output power. A number of parts can be used; Hittite's HMC476MP86 gain block should work sufficiently well. Thus, we can further refine our block diagram by checking all the system parameters and adding more parts as necessary. A good block diagram also includes extra information (e.g., signal frequencies and power levels, bias conditions, etc.) required to understand the circuit operation; an example is shown in Figure 29.

#### **Creating a Schematic**

The next step is to create a schematic, which is a detailed circuit diagram that shows all individual components as graphic symbols as well as connections between the components (Figure 30). The schematic is accomplished with specialized software (e.g., OrCAD) that allows creating a library of component symbols for use in schematic entry. In contrast to the block diagram, the schematic represents an exact model of the desired product; thus, all the details (such as component values) should be thoroughly checked and optimized.

Although the schematic shown in Figure 30 will probably work (after some manipulations), it is too far from perfect. What can be improved? Let's examine the RF signal path first. The RF output power looks too low, since some power will be lost in the output connector. On the other hand, we can save quite a bit of the energy we are losing in the resistive splitter (6 dB loss). Since the ADF4106 RF divider only needs -15 dBm signal to operate, putting a directional coupler (see Fig. 31) is a better alternative. It properly balances the RF power budget and also provides isolation between the synthesizer output and RF divider path. This helps to reduce undesired subharmonics products, which are generated by the dividers and reflected back to the RF output. From this point of view, the coupler should be preferably placed after the RF ampli-

# High Frequency Design SYNTHESIZER DESIGN



Figure 30 · Example of a basic schematic diagram.

fier to avoid unnecessary amplification of these products. It is worth mentioning, that the coupler can be printed on a PCB, which can lead to an overall component count reduction. Further subharmonic reduction is achieved by putting a surfacemount high-pass filter such as HFCN-4600+ manufactured by Mini-Circuits. For very tight spurious requirements, an additional RF amplifier can be inserted into the RF divider path to increase the isolation.

After removing the resistive power splitter we get more power in front of the amplifier, which puts it in a saturation regime. This stabilizes its output level and improves the output power flatness. On the other hand, keeping the amplifier oversaturated is not a good idea since it results in higher current consumption and can also reduce the device lifetime. Putting a small fixed attenuator between the VCO and amplifier allows us to keep the amplifier slightly compressed (but not oversaturated) and also provides a better termination for the VCO output. We can also add an attenuator at the amplifier output that improves the synthesizer output match. Another potential problem is the output harmonics generated by the VCO and amplifier. The indicated spec of -25 dBc can be handled by putting a low-pass filter at the amplifier output. The filter can be a purchased surface-mount part (such as LFCN-7200+ from Mini-Circuits) or can be printed on the board.

The next part to focus on is the ADF4106 PLL IC. The reference input exhibits very high impedance and should work well with square-wave CMOS signals. However, an additional resistor together with DC blocking caps is required to work in a 50-ohm environment. In contrast, the ADF4106 RF input looks fine, since its impedance at the indicated fre-



Figure 31 · Schematic diagram, with locations noted for performance optimization.

High Frequency Design SYNTHESIZER DESIGN



Figure 32 · Common PCB layer arrangements.

quencies is close enough to 50 ohms. Nevertheless, additional matching components may be needed at lower frequencies or to achieve better highpass filter termination.

The major area of optimization is the loop filter. The configuration shown in Figure 30 is probably not the best since the operational amplifier boosts both the phase detector output DC voltage and the noise. Thus, the amplifier gain should be optimized. There are many different types of loop filters well described in [10-22]; an operational amplifier integrator can be a better choice. Although the 45-degree phase margin provides the best trade-

off between the stability, noise picking and tuning speed, a better (flatter) noise performance can be achieved by increasing the phase margin to higher numbers. The penalty is a slower tuning speed that, perhaps, is not a problem at all. The final optimization should be done after clarifying all the key specifications, such as the required phase noise and tuning speed, available reference noise, etc. It is worth mentioning that this optimization could be done earlier at the block diagram stage. However, for more complex designs it is usually a back-andforward process due to the number of trade-offs and possible solutions.

#### From Schematic to PCB

Once we have refined the schematic, it is time to turn it into a printed circuit board. The PCB layout is the physical form of the circuit; thus, all connections are derived from the schematic. There are many computer-added PCB design packages tied to a schematic. Most of the job is performed automatically, although, the best results for high-frequency designs are still achieved with a certain amount of manual placement and routing in order to control various signal interactions effects.

A typical PCB design uses surfacemount components soldered flush to PCB pads. The components and connecting traces are preferably placed on the top of the board, while the bottom layer is used as a ground. This arrangement allows natural 50-ohm microstrip environment (Figure 32); the RF trace width is defined by the board material thickness and its dielectric constant. A multilayer board can be used for more complex designs such as multiloop synthesizers. The board is constructed as a sandwich where each layer is dedicated for specific signals as shown in Figure 32. Connections between layers are performed with metalized via holes. The components can also be mounted on both sides of a PCB to utilize the available space more efficiently.

A solder mask is normally put on a PCB exposing only the areas to be soldered. It should be, however, removed from certain high-frequency areas, too, since it introduces extra loss and slightly changes the impedance. The PCB is also silkscreened with component identification lettering and some other information, which assists people to assemble and troubleshoot the board.

#### Housing Design

The PCB assembly is placed into a metal housing, which is usually made from an aluminum alloy with a proper coating. The synthesizer connects to the outside world through RF connectors (such as SMA, K, etc.), while screw-in EMI feed thrus can be used to bring the external voltages. A certain effort should be applied to minimize discontinuity effects at the RF connector transition. For a singlelayer board the design is pretty straightforward since the RF ground is in direct contact with the housing floor as shown in Figure 33. For a multilayer board, however, the RF ground is in-between the layers and is connected to the bottom layer through multiple via holes. This connection represents a relatively high inductance in the ground path that can affect the performance at high frequencies. A better grounding can be achieved through the top layer (e.g., using an edge-mount connector shown in Fig. 34) due to a shorter distance between the RF ground plane and connector body. From this point of view, the upper level material should be as thin as possible, while other layers can be accommodated using a



Figure 33 · RF connector interface example.



Figure 34 · Top layer grounding with metal and via holes.

thicker, lower-frequency material. Using a coplanar waveguide transition is a good solution as well.

## **Control Software**

To program the output frequency and other parameters, synthesizers require a control mechanism, which can be implemented in many different ways depending on a particular application. Designing software for complex microwave synthesizers can be a challenging task, which is usually developed by a separate team. In our case no internal controller is required since the software resides in an outside computer and is connected through a PC interface. The control

High Frequency Design SYNTHESIZER DESIGN



Figure 35 · Amplifier failure symptom, determined by using circuit probes.

algorithm is fairly simple and well documented in the ADF4106 data sheets [43].

#### **Troubleshooting and Testing**

Very few microwave synthesizer designs work perfectly from the first cut. More likely, they exhibit some undesirable behavior and need troubleshooting. A basic principle in troubleshooting is to reproduce and isolate a particular problem. There is no troubleshooting harder than fixing a symptom that has more than one cause. The process normally starts from a visual inspection of a PCB assembly to look for obvious construction flaws, followed by checking DC bias for all active components. The next step is to check the RF power signal at the output, which should be in expected limits. Otherwise, the RF signal path is inspected by measuring and comparing signal levels at the individual components with an RF probe. Although, the probe does not provide accurate power reading, it can give an idea if a component is functional. For example, measuring no power difference (or even power drop) between the amplifier input and output (Fig. 35) indicates that the part is probably damaged. It is also a good idea to include designated RF test points at critical locations, using miniature coaxial connectors, which can be connected or disconnected as required (Figure 36).

The PLL debugging is greatly simplified since the ADF4106 IC provides



Figure 36 · RF test points aid in circuit troubleshooting.

a programmable access to some internal points such as RF and reference divider outputs. Measuring output frequencies at these points (which should be equal to the desired step size) can give an idea on what path is functioning. You can also check how the charge pump output responds on a division coefficient change. No response indicates a possible phase detector failure; otherwise, the problem can relate to the operational amplifier or VCO parts. The VCO can be checked manually by connecting its tuning port to an external DC supply; the VCO output frequency should follow the control voltage.

Some of the most difficult troubleshooting issues relate to symptoms that are intermittent. This often is the result of components that are thermally sensitive. Compressed air can be used to cool down specific spots on a PCB, while a heat gun raises the temperatures, if necessary. The main idea is to reproduce a problem and then find and replace a part responsible for the failure. Besides fixing the damaged parts, some component adjustments or tuning may be required, for example, with printed filters. A PLL loop filter is another sensitive area that needs further optimizing. Finally, all necessary parameters are measured, and various other specific functional and performance tests are conducted as well. The process is accomplished with a detailed failure analysis and possible design changes.

#### Moving to Production

At a certain point all necessary design documents (e.g., specifications, block diagram, schematic, PCB and mechanical drawings, assembly drawing and bill of materials, test procedure, etc.) should be properly documented and released. All further changes are implemented as an ECO (engineering change order) in accordance with a specific company's rules and standards. A good documentation system is vital for quality manufacturing of any product. To test the product manufacturability, a pilot run of a greater number of units (typically 10 to 25) follows the prototyping stage. It is an opportunity to evaluate the reproducibility of the design as well as documentation completeness. Following the pilot run there will likely be additional small changes until the design develops into a stable product.

This series will be continued in the next issue, showing how to improve the main synthesizer characteristics. Synthesizer design trade-offs and various solutions will be discussed. Past articles are available online at: www.highfrequencyelectronics.com

#### References

42. HMC430LP4 data sheets, available at www.hittite.com

43. ADF4106 data sheets, available at www.analog.com

#### **Author Information**

Dr. Alexander Chenakin is the Director of the F r e q u e n c y Synthesis Group at Phase Matrix, Inc., (www.phasematrix.com). He



earned his degree from Kiev Polytechnic Institute and has worked in a variety of technical and managerial positions around the world.

He can be reached by telephone at 408-954-6409 or by e-mail at achenakin@phasematrix.com.