Load Network Design Technique for Switched-Mode Tuned Class E Power Amplifiers

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Abstract – The switched-mode second-order Class E configuration with a generalized load network including the shunt capacitance, series bondwire inductance, finite DC feed inductance and series *LC* circuit is analytically defined with a set of the exact design equations. Based on these equations, the required voltage and current waveforms and circuit parameters are determined for both general case and particular circuits corresponding to Class E with shunt capacitance, even harmonic Class E and parallel-circuit Class E modes. The effect of the device output bondwire inductance on the optimum load network parameters is demonstrated. The operating power gain achieved with the parallel-circuit Class E power amplifier is evaluated and compared with the operating power gain of the conventional Class B power amplifier. A possibility of the load network implementation at microwaves also is considered. Two examples of high power LDMOSFET and low-voltage HBT power amplifiers, utilizing a transmission-line parallel-circuit Class E circuit configurations, are presented.

I. INTRODUCTION

The switched-mode Class E tuned power amplifiers with a shunt capacitance have found widespread application due to their design simplicity and high efficiency operation [1]. Such a circuit configuration consists of the shunt capacitance, series inductance, RF choke to provide the connection to the DC current supply and series fundamentally tuned *LC*-filter to provide high level of harmonic suppression. In the Class E power amplifier, the transistor operates as an on-to-off switch and the shapes of the current and voltage waveforms provide a condition when the high current and high voltage do not overlap simultaneously that minimize the power dissipation and maximize the power amplifier efficiency. Such an operation mode can be realized for the tuned power amplifier by an appropriate choice of the values of the reactive elements in its load network [2].

However, in reality it is impossible to realize RF choke with infinite impedance at the fundamental and any harmonics. Moreover, using a finite DC feed inductance has an advantage of minimizing size, cost and complexity of the overall circuit. Several approaches were proposed to analyze the effect of a finite DC feed inductance on the Class E mode with shunt capacitance. Some of them based on Laplace transform technique provide only particular solutions with the presentation of the load network parameters in a table format [3-5]. The well-defined analytic solution based on an assumption of the even harmonic resonant conditions when the DC feed inductance and parallel capacitance are tuned on any even harmonic was published in [6]. Unfortunately, in this case, the optimum load resistance is over an order of magnitude smaller than for conventional Class E with shunt capacitance when RF choke is used.

However, the circuit schematic with a shunt capacitance and series inductance that can provide ideally 100-percent collector efficiency is not a unique. The same results can be achieved with parallel-circuit Class E configuration with the parallel inductance, parallel capacitance and fundamentally tuned series *LC*-circuit in the load network [7]. In this parallel-circuit Class E power amplifier, the ideal switching operation conditions can be achieved by an appropriate choice of the values of the reactive elements in its load network, which should be mistuned at the fundamental frequency. The basic advantage of such a load network configuration is that the parallel inductance can be used instead of RF choke and no need to use an additional series phase-shifting element.

In a present paper, the switched-mode second-order Class E configuration with generalized load network including the finite DC feed inductance, shunt capacitance and series bondwire inductance, which is a part of the transistor output circuit, is discussed. The results of Fourier analysis and derivation of the equations governing the operation in an idealized operation mode are presented. Based on these equations, the required voltage and current waveforms and circuit parameters are determined for both general case and particular circuits corresponding to Class E with shunt capacitance, even harmonic Class E and parallel-circuit Class E configurations. The effect of the device output bondwire inductance on the optimum circuit parameters is demonstrated. Also the operating power gain achieved with the parallel-circuit Class E power amplifier is evaluated and compared with the operating power gain of the conventional Class B power amplifier.

II. GENERALIZED LOAD NETWORK

The generalized second-order load network of a switched-mode Class E power amplifier is shown in Figure 1(*a*). The load network consists of a shunt capacitance C, a series inductance L_b, a parallel inductance L, a series reactive element X and a series resonant L_0C_0-circuit tuned on the fundamental and a load R. In a common case, a shunt capacitance C can represent the intrinsic device output capacitance and external circuit capacitance added by the load network, a series inductance L_b can be considered as a bondwire and lead inductance, a parallel inductance L represents the finite DC-feed inductance and a series reactive element X can be positive (inductance) or negative (capacitance) or zero depending on the Class E mode. The active device is considered to be an ideal switch that is driven in such a way in order to provide the device switching between its on-state and off-state operation conditions. As a result, the collector voltage waveform is determined by the transient response of the load network when the switch is off.

In order to simplify an analysis of a general-circuit Class E power amplifier, a simple equivalent circuit of which is shown in Figure 1(*b*), it is advisable to introduce the following several assumptions [2]:

- the transistor has zero saturation voltage, zero saturation resistance, infinite off-state resistance and its switching action is instantaneous and lossless

- the total parallel capacitance is independent of the collector and is assumed to be linear
- the loaded quality factor Q_L of the series resonant L_0C_0-circuit is high enough in order the output current to be sinusoidal at the carrier frequency
- there are no losses in the circuit except only into the load R
- for optimum operation mode a 50% duty cycle is used

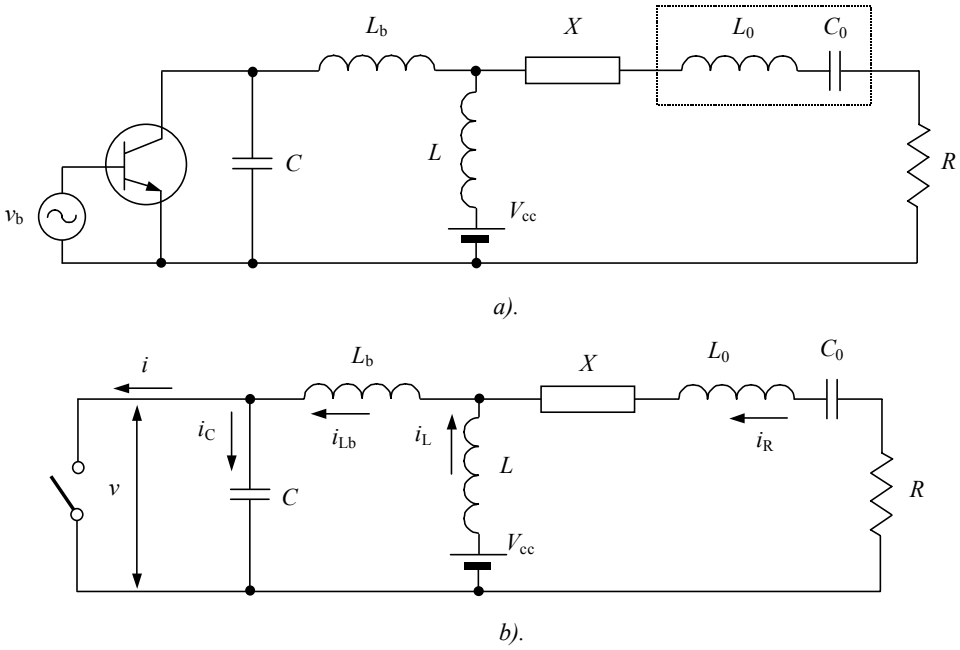


Fig. 1. Equivalent circuits of the Class E power amplifiers with generalized load network

For the idealized theoretical analysis, it is advisable to replace the active device by the ideal switch as it is shown in Figure 1(*b*). Let the moments of switch-on is $t = 0$ and switch-off is $t = \pi/\omega$ with period of repeatability of input driving signal $T = 2\pi$ are determined by the input circuit of the power amplifier. Assume that the losses in the reactive circuit elements are negligible and the quality factor of the loaded L_0C_0-circuit is sufficiently high. For lossless operation mode, it is necessary to provide the following optimum conditions for voltage across the switch just prior to the start of switch on at the moment $t = 2\pi/\omega$, when transistor is saturated:

$$v(\omega t)\big|_{\omega t = 2\pi} = 0 \tag{1}$$

$$\left.\frac{dv(\omega t)}{d(\omega t)}\right|_{\omega t = 2\pi} = 0 \tag{2}$$

where v is the voltage across the switch.

Let the output current flowing through the load is written as sinusoidal by

$$i_R(\omega t) = I_R \sin(\omega t + \varphi) \tag{3}$$

where φ is the initial phase shift.

When switch is on for $0 \le \omega t < \pi$, the voltage $v(\omega t) = V_{cc} - v_{L_b}(\omega t) - v_L(\omega t) = 0$, where $v_{L_b}(\omega t) = \omega L_b \dfrac{di_s(\omega t)}{d(\omega t)}$ and $v_L(\omega t) = \omega L \dfrac{di_L(\omega t)}{d(\omega t)}$. Since the current flowing through the capacitance C is equal to zero, i.e. $i_C(\omega t) = \omega C \dfrac{dv_s(\omega t)}{d(\omega t)} = 0$, and taken into account the boundary conditions $i_s(0) = 0$ and $i_L(0) = -I_R \sin\varphi$, one can obtain

$$i(\omega t) = i_L(\omega t) + i_R(\omega t) = \frac{V_{cc}}{\omega(L + L_b)}\omega t + \frac{\omega L I_R}{\omega(L + L_b)}\left[\sin(\omega t + \varphi) - \sin\varphi\right] \tag{4}$$

When switch is off for $\pi \le \omega t < 2\pi$, the current $i(\omega t) = 0$ and the current $i_C(\omega t) = i_L(\omega t) + i_R(\omega t)$ flowing through the capacitance C can be rewritten as

$$\omega C \frac{dv(\omega t)}{d(\omega t)} = \frac{1}{\omega L}\int_{\pi}^{\omega t}\left[V_{cc} - v(\omega t) - v_{L_b}(\omega t)\right]d(\omega t) + i_L(\pi) + I_R \sin(\omega t + \varphi) \tag{5}$$

under the initial off-state conditions $v(\pi) = 0$ and $i_L(\pi) = \dfrac{V_{cc}\pi - \omega L I_R \sin\varphi}{\omega(L + L_b)}$.

Equation (5) can be represented in the form of the linear nonhomogeneous second-order differential equation given by

$$\omega^2(L + L_b)C\frac{d^2v(\omega t)}{d(\omega t)^2} + v(\omega t) - V_{cc} - \omega L I_R \cos(\omega t + \varphi) = 0 \tag{6}$$

which general normalized solution can be obtained in the form of

$$\frac{v(\omega t)}{V_{cc}} = C_1 \cos(q\omega t) + C_2 \sin(q\omega t) + 1 - \frac{q^2 p}{1 - q^2}\cos(\omega t + \varphi) \tag{7}$$

where

$$q = 1/\omega\sqrt{(L + L_b)C} \tag{8}$$

$$p = \omega L I_R / V_{cc} \tag{9}$$

and the coefficients C_1 and C_2 are determined from the initial off-state conditions by

$$C_1 = -\left(\cos q\pi + q\pi \sin q\pi\right) - \frac{qp}{1 - q^2}\left[q\cos\varphi\cos q\pi - \left(1 - 2q^2\right)\sin\varphi\sin q\pi\right] \tag{10}$$

$$C_2 = \left(q\pi\cos q\pi - \sin q\pi\right) - \frac{qp}{1 - q^2}\left[q\cos\varphi\sin q\pi + \left(1 - 2q^2\right)\sin\varphi\cos q\pi\right] \tag{11}$$

The DC supply current I_0 can be found using Fourier formula and equation (9) by

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\,d(\omega t) = \frac{1}{2\pi}\frac{\omega L I_R}{\omega(L + L_b)}\left(\frac{\pi^2}{2p} + 2\cos\varphi - \pi\sin\varphi\right). \tag{12}$$

In idealized Class E operation mode, there is no nonzero voltage and current simultaneously that means a lack of the power losses and gives an idealized collector efficiency of 100%. This implies that the DC power and fundamental output power are equal, i. e.

$$I_0 V_{cc} = \frac{V_R^2}{2R} \tag{13}$$

where $V_R = I_R R$ is the voltage amplitude across the load resistance R.

As a result, using equation (12) and (13) and taking into account that $R = V_R^2 / 2P_{out}$, the optimum load resistance R for the specified values of supply voltage V_{cc} and output power P_{out} can be obtained by

$$R = \frac{1}{2}\left(\frac{V_R}{V_{cc}}\right)^2 \frac{V_{cc}^2}{P_{out}} \tag{14}$$

where

$$\frac{V_R}{V_{cc}} = \frac{1}{\pi}\left(\frac{\pi^2}{2p} + 2\cos\varphi - \pi\sin\varphi\right) \Big/ \left(1 + \frac{L_b}{L}\right). \tag{15}$$

The normalized load network inductance L and capacitance C as a function of the ratio L_b/L can be respectively defined using equations (8), (9) and (12) by

$$\frac{\omega L}{R} = p\left(1 + \frac{L_b}{L}\right) \Big/ \left(\frac{\pi}{2p} + \frac{2}{\pi}\cos\varphi - \sin\varphi\right) \tag{16}$$

$$\omega C R = 1/q^2 \left(1 + \frac{L_b}{L}\right)\frac{\omega L}{R}. \tag{17}$$

The series load reactance X, which in special particular cases may have an inductive, capacitive or zero reactance depending on the load network parameters can be calculated using two quadrature fundamental Fourier components of the voltage across the combination of capacitance C and bondwire inductance L_b from

$$V_R = \frac{1}{\pi}\int_0^{2\pi} \left[v(\omega t) + v_{L_b}(\omega t)\right] \sin(\omega t + \varphi)\, d(\omega t) \tag{18}$$

$$V_X = \frac{1}{\pi}\int_0^{2\pi} \left[v(\omega t) + v_{L_b}(\omega t)\right] \cos(\omega t + \varphi)\, d(\omega t). \tag{19}$$

III. LOAD NETWORK WITH SHUNT CAPACITANCE

The load network of a class E power amplifier with a shunt capacitance is shown in Figure 2, where the load network consists of a capacitance C shunting the transistor, a series inductance L_X, a series fundamentally tuned L_0C_0-circuit and a load resistance R. The collector of the transistor is connected to the supply voltage by RF choke with high reactance at the fundamental frequency.

Such a simplified load network represents a first-order Class E mode as their electrical behavior in time domain can be analytically described by the first-order differential equations [2].

In this case, when switch is on for $0 \le \omega t < \pi$, the current through the switch is written by

$$i(\omega t) = I_{\mathrm{R}} \left[\sin(\omega t + \varphi) - \sin\varphi\right]. \tag{20}$$

When switch is off for $\pi \le \omega t < 2\pi$, the voltage across the switch is produced by the charging of this capacitance according to

$$v(\omega t) = \frac{1}{\omega C}\int_{\pi}^{\omega t} i_{\mathrm{C}}(\omega t)\, d\omega t = -\frac{I_{\mathrm{R}}}{\omega C}\left[\cos(\omega t + \varphi) + \cos\varphi + (\omega t - \pi)\sin\varphi\right]. \tag{21}$$

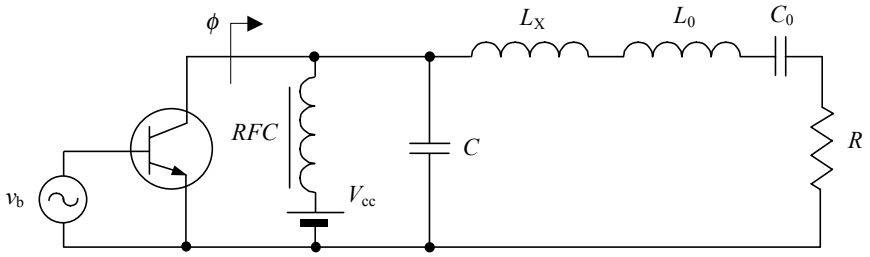


Fig. 2. Equivalent circuit of the Class E power amplifier with shunt capacitance

Applying the first optimum condition given by equation (1) into equation (21) allows defining the phase angle φ as

$$\varphi = \tan^{-1}\left(-\frac{2}{\pi}\right) = -32.482^{\circ} \tag{22}$$

As a result, the normalized steady-state collector voltage waveform for $\pi \le \omega t < 2\pi$ and current waveform for period of $0 \le \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{\mathrm{cc}}} = \pi\left(\omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t\right) \tag{23}$$

$$\frac{i(\omega t)}{I_0} = \omega t - \frac{3\pi}{2} - \frac{\pi}{2}\cos\omega t - \sin\omega t \tag{24}$$

In Figure 3, the normalized (*a*) load current, (*b*) collector voltage waveform and (*c*) collector current waveforms for idealized optimum Class E with shunt capacitance are shown. From collector voltage and current waveforms it follows that, when the transistor is turned on, there is no voltage across the switch and the current $i(\omega t)$ consisting of the load sinusoidal current and DC current flows through the device. However, when the transistor is turned off, this current now flows through the shunt capacitance *C*.

From equations (18) and (19) defining two quadrature fundamental Fourier components, the optimum load resistance *R*, series inductance L_X and shunt capacitance *C* can be found from

$$R = \frac{8}{\pi^2 + 4}\frac{V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} = 0.5768\frac{V_{\mathrm{cc}}^2}{P_{\mathrm{out}}} \tag{25}$$

$$\frac{\omega L_{\mathrm{X}}}{R} = \frac{V_{\mathrm{X}}}{V_{\mathrm{R}}} = 1.1525 \tag{26}$$

$$\omega CR = \frac{\omega C}{I_{\mathrm{R}}} V_{\mathrm{R}} = 0.1836 \tag{27}$$

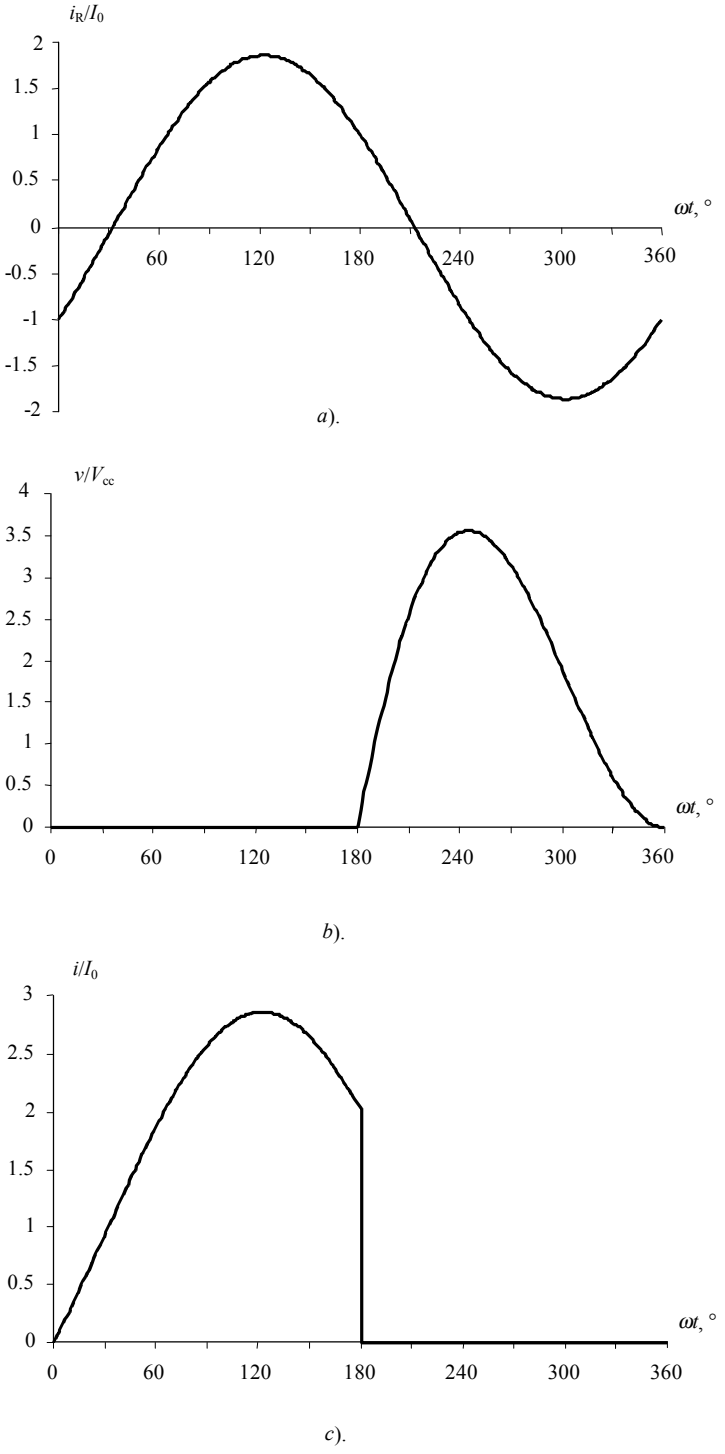


Fig. 3. Normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum Class E with shunt capacitance

Then, the fundamental phase angle of the load network connected to the switch and required for the idealized optimum Class E mode with shunt capacitance can be determined through the circuit parameters by

$$\phi = \tan^{-1}\left(\frac{\omega L_X}{R}\right) - \tan^{-1}\left(\frac{\omega CR}{1 - \frac{\omega L_X}{R}\omega CR}\right) = 35.945° \tag{28}$$

When realizing the optimum Class E operation mode, it is very important to know up to which maximum frequency such an efficient operation mode can be extended. In this case, it is required to establish a relationship between maximum frequency f_{max}, device output capacitance C_{out} and supply voltage V_{cc}. The device output capacitance C_{out} gives the main limitation of the maximum operation frequency. So, using equation (27) when $C = C_{out}$ gives the value of maximum operation frequency of [8]

$$f_{max} = 0.057\frac{P_{out}}{C_{out}V_{cc}^2}. \tag{29}$$

IV. Even Harmonic Resonant Class E Load Network

The second-order Class E load network implies the finite value of DC feed inductance rather than ideal RF choke with infinite reactance at any harmonic components. For even harmonic Class E, the DC feed inductance is restricted to values that satisfy an even harmonic resonance condition and it is assumed that the fundamental voltage across the switch and output voltage across the load have a phase difference of $\pi/2$ [6]. As a result, two unknown parameters of equation (7) can be set in this particular case as

$$q = 2n \tag{30}$$

$$\varphi = 90° \tag{31}$$

where $n = 1, 2, 3, \ldots$.

The third parameter p can be found from optimum condition given by equation (2) as

$$p = \frac{4n^2 - 1}{8n^2}\pi \ . \tag{32}$$

The DC supply current I_0 can be found from equation (12) when $L_b = 0$ by

$$I_0 = \frac{1}{2\pi}\int_0^{2\pi} i(\omega t)\,d(\omega t) = \frac{1}{2(4n^2 - 1)}I_R \ . \tag{33}$$

As a result, the normalized steady-state collector voltage waveform for $\pi \le \omega t < 2\pi$ and current waveform for period of $0 \le \omega t < \pi$ are

$$\frac{v(\omega t)}{V_{cc}} = 1 - \frac{\pi}{2}\sin\omega t + \frac{\pi}{4n}\sin(2n\omega t) - \cos(2n\omega t) \tag{34}$$

$$\frac{i(\omega t)}{I_0} = 2\left[\frac{8n^2}{\pi}\omega t - 4n^2 + 1 + \left(4n^2 - 1\right)\cos\omega t\right]. \tag{35}$$

The load network of even harmonic Class E is shown in Figure 4 where to compensate the required phase shift caused by preliminary chosen particular parameters the series capacitance C_X is needed. The value of this capacitance can be found from the consideration of two fundamental voltage quadrature components across the switch given by equations (18) and (19). In Figure 5, the normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum even harmonic Class E mode are plotted. If the collector voltage waveform of even harmonic Class E is very similar to the collector voltage waveform of Class E with shunt capacitance, then the behavior of the current waveform is substantially different. So, for even harmonic Class E configuration, the collector (drain) current reaches its peak value, which is in four times greater than the DC current, at the end of the conduction interval. Consequently, in the case of the sinusoidal driving signal it is impossible to provide the maximum collector current when the input base current is smoothly reducing to zero.

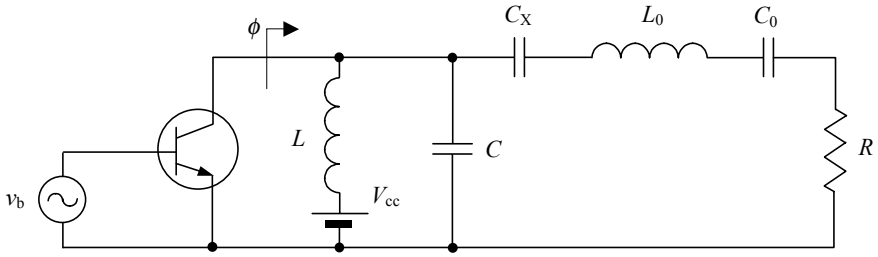


Fig. 4. Equivalent circuit of the even harmonic Class E power amplifier

The optimum load network parameters for the most practical case $n = 1$ can be calculated from

$$R = \frac{1}{18}\frac{V_{cc}^2}{P_{out}} = 0.056\frac{V_{cc}^2}{P_{out}} \tag{36}$$

$$L = \frac{9\pi}{8}\frac{R}{\omega} = 3.534\frac{R}{\omega} \tag{37}$$

$$C = \frac{2}{9\pi}\frac{1}{\omega R} = 0.071\frac{1}{\omega R} \tag{38}$$

$$C_X = \frac{4\pi}{32 + 3\pi^2}\frac{1}{\omega R} = 0.204\frac{1}{\omega R} \tag{39}$$

The phase angle ϕ between the fundamental-frequency voltage $v_1(\omega t)$ $v_{s1}(\omega t)$ and current $i_1(\omega t)$ seen by switch terminal is equal to

$$\phi = \frac{3}{4}\frac{R}{\omega L}\frac{1 + (\omega C_X R)^2}{(\omega C_X R)^2} - \frac{1}{\omega C_X R} = 22.302°. \tag{40}$$

whereas the maximum frequency f_{max} at which optimum even harmonic Class E can be realized is calculated from

$$f_{max} = \frac{2}{\pi^2}\frac{P_{out}}{C_{out}V_{cc}^2} = 0.203\frac{P_{out}}{C_{out}V_{cc}^2} \tag{41}$$

where C_{out} is the device output capacitance.

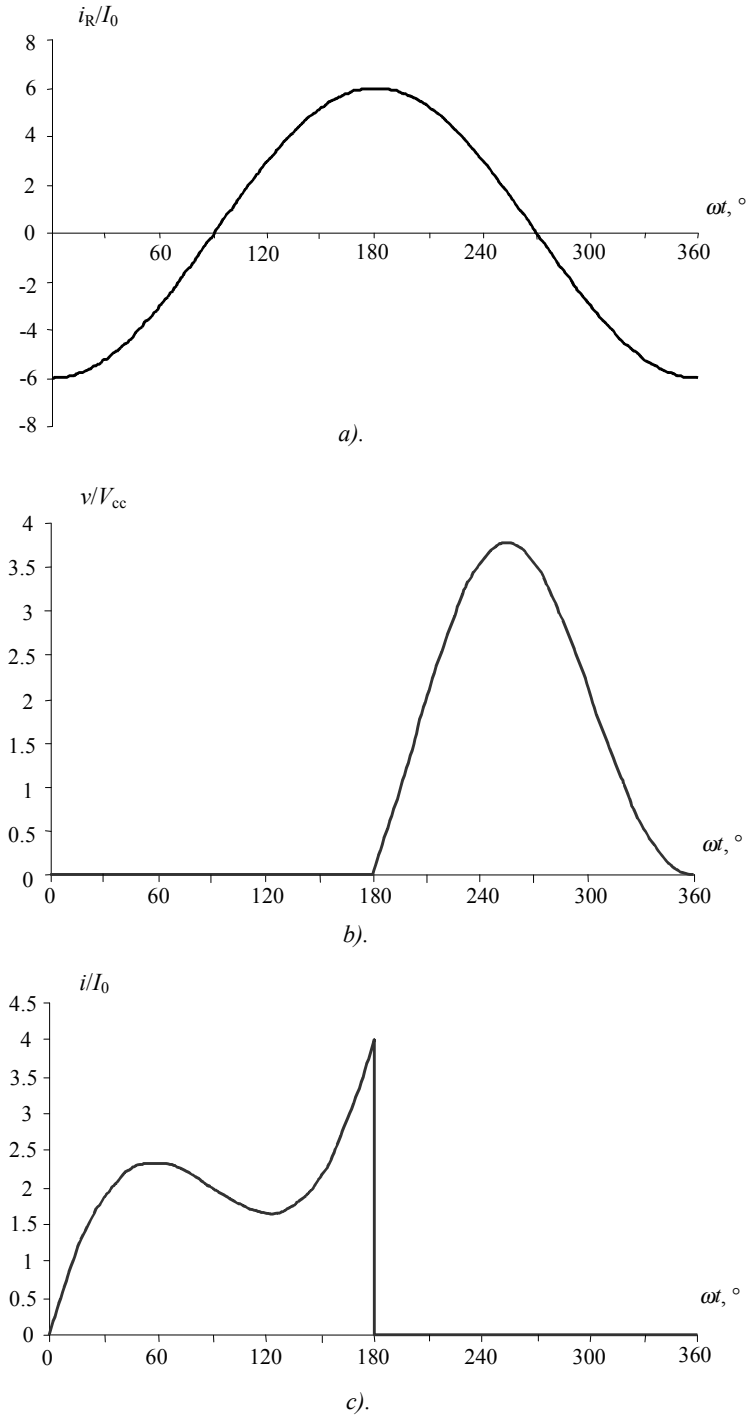


Fig. 5. Normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum even harmonic Class E

V. LOAD NETWORK WITH PARALLEL CIRCUIT

For even harmonic Class E mode, to compensate the resulting phase shift due to the intuitive determination of two initially unknown parameters a priori it is required to include an additional series phase-shifting capacitance C_X. To solve equation (7) in a general case with regard to three unknown parameters ($q = 1/\omega\sqrt{LC}$, p and φ), it is necessary to use two optimum conditions given by equations (1) and (2) and to add an additional equation defining the supply voltage V_{cc} from Fourier series expansion as

$$V_{cc} = \frac{1}{2\pi}\int_0^{2\pi} v(\omega t)\,d(\omega t)$$

$$= \frac{V_{cc}}{\pi}\left[\frac{C_1}{q}(\sin 2q\pi - \sin q\pi) - \frac{C_2}{q}(\cos 2q\pi - \cos q\pi) - \frac{2q^2 p}{1-q^2}\sin\varphi\right] \tag{42}$$

As a result, solving the system of three equations with three unknown parameters numerically gives the following values [7]:

$$q = 1.412 \tag{43}$$

$$p = 1.210 \tag{44}$$

$$\varphi = 15.155°. \tag{45}$$

The load network of parallel-circuit Class E is shown in Figure 6 where the series circuit is tuned on the fundamental and all required phase shifts to realize idealized voltage and current waveforms are determined by the appropriate calculation of the parallel circuit parameters. In Figure 7, the normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum conditions are shown.

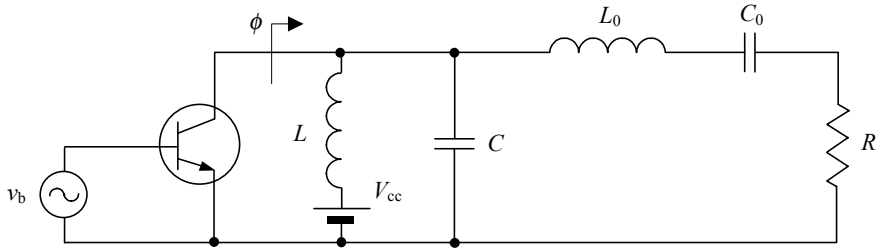


Fig. 6. Equivalent circuit of the parallel-circuit Class E power amplifier

For parallel-circuit Class E mode, the optimum load resistance R, parallel inductance L and parallel capacitance C using equations (14), (16) and (17) can be obtained, respectively, by

$$R = 1.365\frac{V_{cc}^2}{P_{out}} \tag{46}$$

$$L = 0.732\frac{R}{\omega} \tag{47}$$

$$C = \frac{0.685}{\omega R} \tag{48}$$

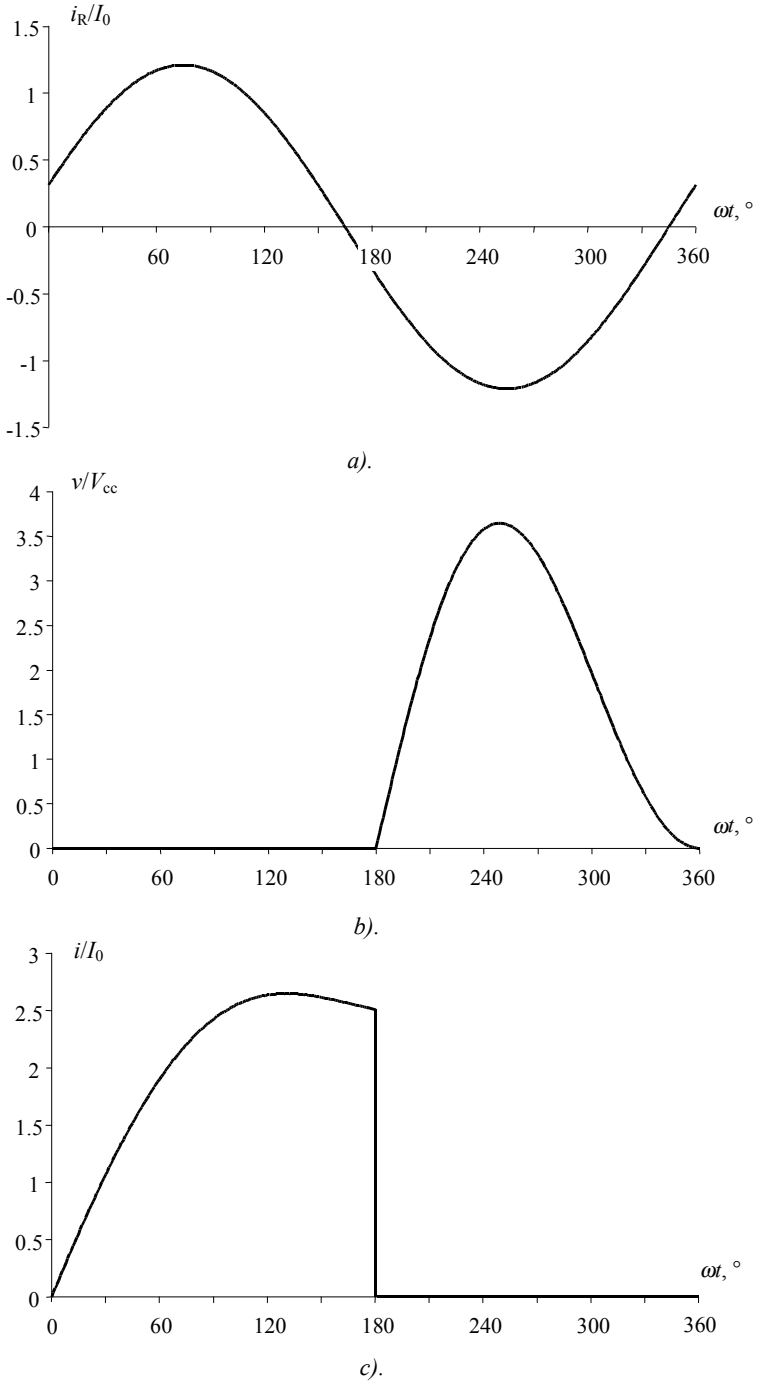


Fig. 7. Normalized (*a*) load current and collector (*b*) voltage and (*c*) current waveforms for idealized optimum parallel-circuit Class E

The fundamental phase angle ϕ and maximum frequency $f_{\max}$ can be represented as the functions of load network elements as

$$\phi = \tan^{-1}\left(\frac{R}{\omega L} - \omega RC\right) = 34.244° \tag{49}$$

$$f_{\max} = 0.0798 \frac{P_{\text{out}}}{C_{\text{out}} V_{\text{cc}}^2}. \qquad (50)$$

From a comparison of equations (29) and (50) it follows that the maximum frequency $f_{\max}$ for optimum parallel-circuit Class E power amplifier in 1.4 times greater than that one for optimum Class E power amplifier with shunt capacitance.

VI. INFLUENCE OF BONDWIRE INDUCTANCE L_b

At higher frequencies when using the discrete power transistors in hybrid power amplifier integrated circuits, it is necessary to take into account the device output bondwire and lead inductance because its influence may be significant especially at high output power level and low supply voltage. The effect of bondwire inductance for even harmonic Class E configuration gives unrealistically small values for optimum load resistance and DC-feed inductance when, for example, in UHF band typical values for the bondwire inductance of approximately 1 nH constitute most, if not all, of the required DC feed inductance [9]. The simplified approach to analyze the parallel-circuit Class E configuration with bondwire inductance based on a simple assumption of the sinusoidal voltage across the infinite DC feed inductance cannot provide an optimum solution [10].

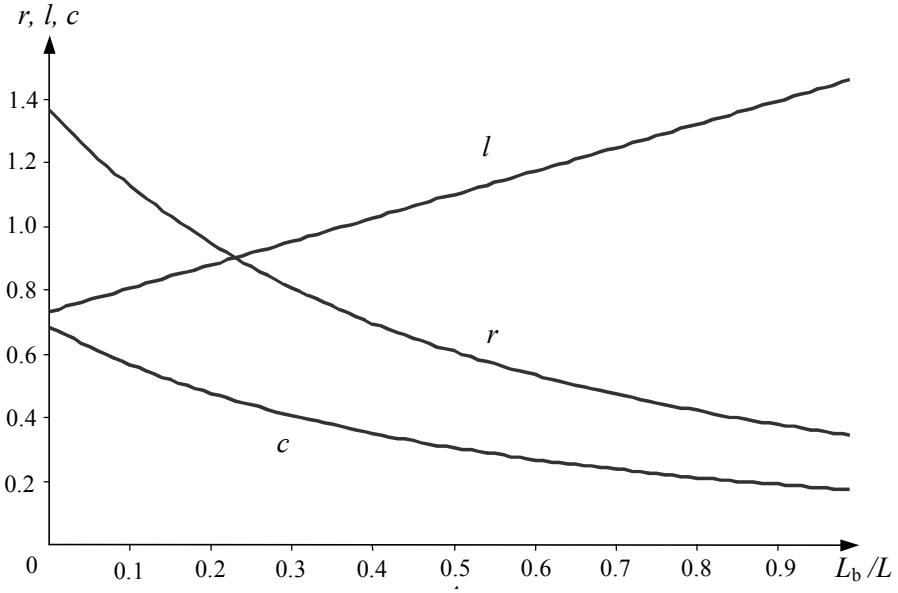


Fig. 8. Normalized optimum load network parameters versus normalized bondwire inductance L_b/L for parallel-circuit Class E

The exact values for the optimum load network parameters can be easily obtained from equations (14)-(17) analytically derived for generalized Class E configuration. In Figure 8, the dependences of the normalized parallel inductance $l = \omega L / R$, parallel capacitance $c = \omega C R$ and load resistance $r = R P_{\text{out}} / V_{\text{cc}}^2$ for parallel-circuit Class E as the functions of the normalized bondwire inductance, L_b/L, are plotted. As it is shown from Figure 8, the increasing effect of the bondwire

inductance L_b leads to the significantly reduced optimum values for the load resistance R and shunt capacitance C and increased optimum value for the finite DC-feed inductance L.

VII. TRANSMISSION-LINE LOAD NETWORK

At microwave frequencies, all inductances in matching circuits of the power amplifier are normally replaced by the transmission lines to minimize power losses. So, the matching circuit can be composed with any types of the transmission lines including open-circuit or short-circuit stubs to provide the required matching and harmonic suppression conditions. However, for compact small-size power amplifier modules developed, for example, for handset transmitters it is advisable to use the series microstrip lines and parallel capacitors. And in order to keep the optimum switching conditions at the fundamental this matching circuit should contain the series transmission line as the first inductive element.

Idealized time-domain calculation of the collector voltage and current waveforms implies the availability of infinite number of the harmonics with their optimum amplitudes and phases in the power amplifier output spectrum. Let us consider what are the real contribution of the first and second harmonics to the above-mentioned waveforms with regard to the parallel-circuit Class E power amplifier using the Fourier series expansion approach. The Fourier series for voltage across the switch $v(\omega t)$ is defined as

$$v(\omega t) = V_{cc} + \sum_{k=1}^{\infty} \left[V_{Rk} \sin k(\omega t + \varphi) + V_{Xk} \cos k(\omega t + \varphi) \right] \tag{51}$$

where the DC supply voltage V_{cc} and the active and reactive harmonic components, V_{Rk} and V_{Xk}, are obtained respectively from

$$V_{cc} = \frac{1}{2\pi} \int_0^{2\pi} v(\omega t) d(\omega t)$$

$$V_{Rk} = \frac{1}{\pi} \int_0^{2\pi} v(\omega t) \sin k(\omega t + \varphi) d(\omega t)$$

$$V_{Xk} = \frac{1}{\pi} \int_0^{2\pi} v(\omega t) \cos k(\omega t + \varphi) d(\omega t) \quad .$$

The same Fourier analysis can be applied to the current flowing through the switch $i(\omega t)$. As it is shown in Figure 9 (dashed lines) from the normalized collector (*a*) voltage and (*b*) current waveforms, where I_0 is the DC current, a good approximation to the parallel-circuit Class E mode can be obtained with only the first and second harmonics accounted for the collector current and voltage waveforms. This situation is similar to that of for the Class E power amplifier with shunt capacitance [11]. Consequently, the high efficiency Class E power amplifier with parallel circuit can be

also effectively used in monolithic microwave design, for example, for cellular mobile phone application provided the optimum conditions for first two harmonics are fulfilled.

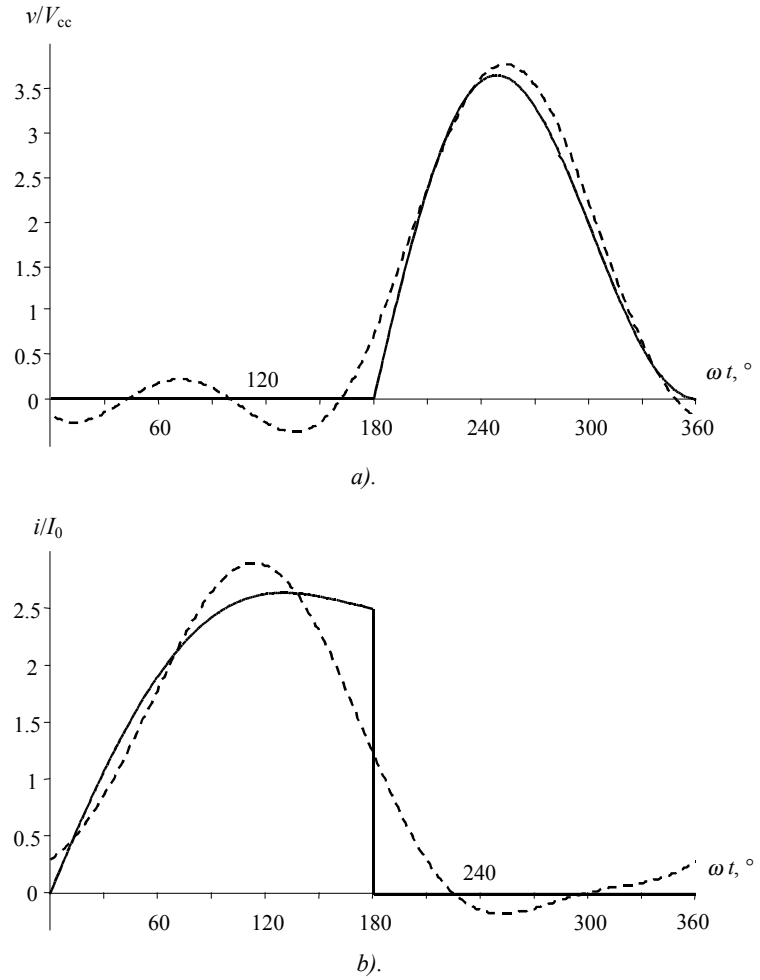


Fig. 9. Two-harmonic approximation to parallel-circuit Class E

As a first step, for parallel-circuit Class E power amplifier shown in Figure 6, the parallel inductance L at microwaves should be replaced by the short-length short-circuited transmission line TL as shown in Figure 10(a) according to

$$Z_0 \tan\theta = \omega L \tag{52}$$

where Z_0 and θ are the characteristic impedance and electrical length of the transmission line TL, respectively. To approximate the idealized parallel-circuit Class E operation conditions for microwave power amplifier, it is necessary to design the transmission-line load network satisfying the required idealized optimum impedance at fundamental given by

$$Z_{\text{net1}} = R / \left(1 - j \tan 34.244^\circ\right) \tag{53}$$

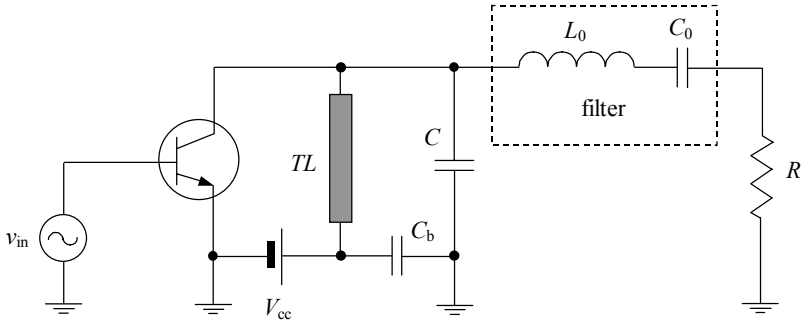
which can be obtained from equations (47)-(49).

By using equation (47), which determines the parallel inductance L for optimum switched-mode operation, the ratio between the transmission line parameters and the load for idealized 50-percent duty cycle switched-mode operation can be obtained as

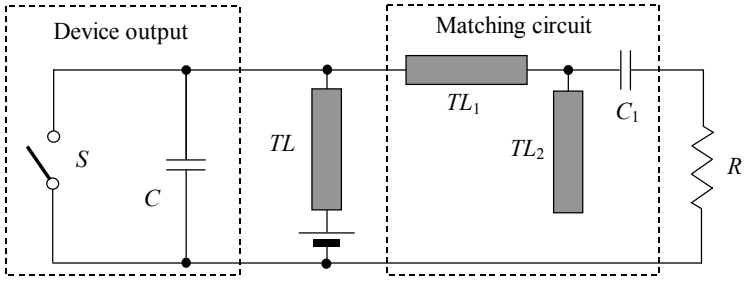
$$\tan\theta = 0.732\frac{R}{Z_0} . \qquad (54)$$

In practical circuit when impedance transformation between the load R and active device is needed, the L_0C_0-filter should be replaced by the output matching circuit, which input impedance needs to be sufficiently high at second and higher-order harmonics. For example, the series L_0C_0-filter can be replaced by T-transformer containing two lumped capacitors and one lumped inductor providing the required harmonic suppression. For transmission-line realization, the output matching circuit can be composed with any types of the transmission lines including open-circuit or short-circuit stubs to provide the required matching and harmonic suppression conditions. However, to maintain the optimum switching conditions at the fundamental this matching circuit should contain the series transmission line as the first element as it is shown in Figure 10(*b*).

One possible transmission-line circuit configuration shown in Figure 11(*a*), which was developed for monolithic cellular handset power amplifier, includes the series transmission line with parallel capacitances. However, because of the finite electrical length of the transmission lines it is impossible to realize simultaneously the required inductive impedance at the fundamental frequency with pure capacitive reactances at higher-order harmonics. Even at the second harmonic the real part of the circuit input impedance is quite high as it is shown in Figure 11(*b*). Nevertheless, such an approach allows designing power amplifiers with extremely high efficiency with a good proximity to parallel-circuit Class E operation mode. In this case, no needs to use an additional RF choke for DC supply current, whose function can be performed by a very short parallel microstrip line.



a).



b).

Fig. 10. Equivalent circuits of transmission-line parallel-circuit Class E power amplifier

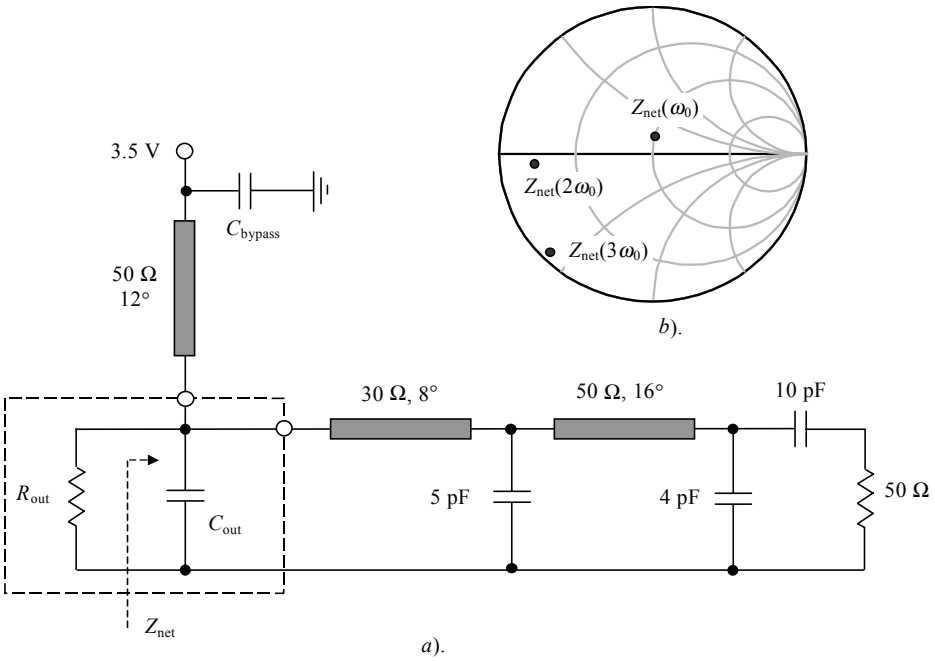


Fig. 11. Output load network of transmission-line parallel-circuit Class E power amplifier for handset application

VIII. POWER GAIN

The load network of any type of Class E mode in order to realize the idealized switching conditions is mistuned at the fundamental frequency, thus violating the conjugate matching conditions required for conventional Class B operation. This means that the output voltage and current waves consist of both incident and reflected components. However, the load impedance conditions for Class E mode is differ from that of for Class B mode. The operating power gain G_P expressed through the active device Y-parameters and load can be obtained by

$$G_P = \frac{|Y_{21}|^2}{\mathrm{Re}Y_{in}} \frac{R}{|Y_{22} + Y_L|^2} \tag{55}$$

where Y_{21}, Y_{22} are the device Y-parameters, Y_{in} is the device input admittance and $Y_L = G + jB$ is the load admittance, $R = 1/G$ is the load resistance [12]. Substituting the real and imaginary parts of the device Y-parameters and load admittance gives

$$G_P = \frac{|Y_{21}|^2}{\mathrm{Re}Y_{in}} \frac{R}{\left(1 + \frac{G_{22}}{G}\right)^2 + \left(\frac{B_{22} + B}{G}\right)^2} \quad . \tag{56}$$

Consequently, the ratio between the operating power gain of the switched-mode parallel-circuit Class E power amplifier $G_{P(E)}$ and the operating power gain of the conventional Class B power amplifier $G_{P(B)}$ with conjugate-matched load can be written by

$$\frac{G_{P(E)}}{G_{P(B)}} = \frac{1}{1 + (B_{22} + B)^2 R_{(E)}^2} \frac{R_{(E)}}{R_{(B)}} \tag{57}$$

where $R_{(E)}$ is the load resistance of the Class E power amplifier and $R_{(B)}$ is the load resistance of the Class B power amplifier. For ideal optimum 100-percent efficiency Class E operation mode it is possible to use equation (13). Therefore, from equation (15) for parallel-circuit Class E configuration it follows

$$V_{R(E)} = 1.652\,V_{cc}\,. \tag{58}$$

For the same output power P_{out} and taking into account that in conventional Class B with zero saturation voltage $V_{R(B)} = V_{cc}$, it can be readily obtained

$$\frac{R_{(E)}}{R_{(B)}} = \frac{V_{R(E)}^2}{V_{R(B)}^2} = 2.729 \tag{59}$$

that shows the significantly higher value for the load resistance in the optimum switched-mode parallel-circuit Class E operation mode.

As a result, the power gain ratio given by equation (57) can be rewritten in the form of

$$\frac{G_{P(E)}}{G_{P(B)}} = \frac{2.729}{1 + \tan^2\phi} = 1.865 \tag{60}$$

where $\phi = 34.244°$ is the phase angle between the fundamental-frequency voltage and current across the switch required for the optimum parallel-circuit Class E mode.

The result given by equation (60) means that ideally the operating power gain for the switched-mode parallel-circuit Class E mode compared with conventional Class B mode is practically the same and even slightly greater despite the mistuning of the output load network. This can be explained by the larger value of the load required for the optimum parallel-circuit Class E operation mode. The idealized conditions for switched-mode operation can be achieved with instant on-to-off active device switching which requires the rectangular input driving signal compared with sinusoidal driving signal for conventional Class B mode. However, the power losses due to the switching time are sufficiently small and, for example, for switching time of $\tau_s = 0.35$ or 20° are only of about 1% [13]. Consequently, it needs to slightly overdrive the active device when the input power should be increased by 1-2 dB to minimize switching time and maximize the collector efficiency of the switched-mode Class E power amplifier. As a result, the resulting power gain becomes approximately equal to the power gain of the conventional Class B power amplifier.

IX. Results

Based on previous theoretical analysis, a comparison of the different Class E circuit configurations shows an obvious advantage of the parallel-circuit Class E mode especially for low supply voltage application with high level of the circuit integration. For such a load network, no need to use an RF choke, the required value of load resistance R for the same output power and supply voltage is greater by approximately 2.4 times and 24 times compared with Class E with

shunt capacitance and even harmonic Class E, respectively. The value of parallel inductance L is not too small as for even harmonic Class E, but is sufficiently small for using in hybrid and monolithic integrated circuits. In addition, the parallel-circuit Class E configuration can be easily implemented in high-efficiency broadband power amplifier design when it is necessary only to satisfy the required phase angle at the fundamental frequency and to choose the proper Q-factor of the series resonant LC-circuit [14, 15].

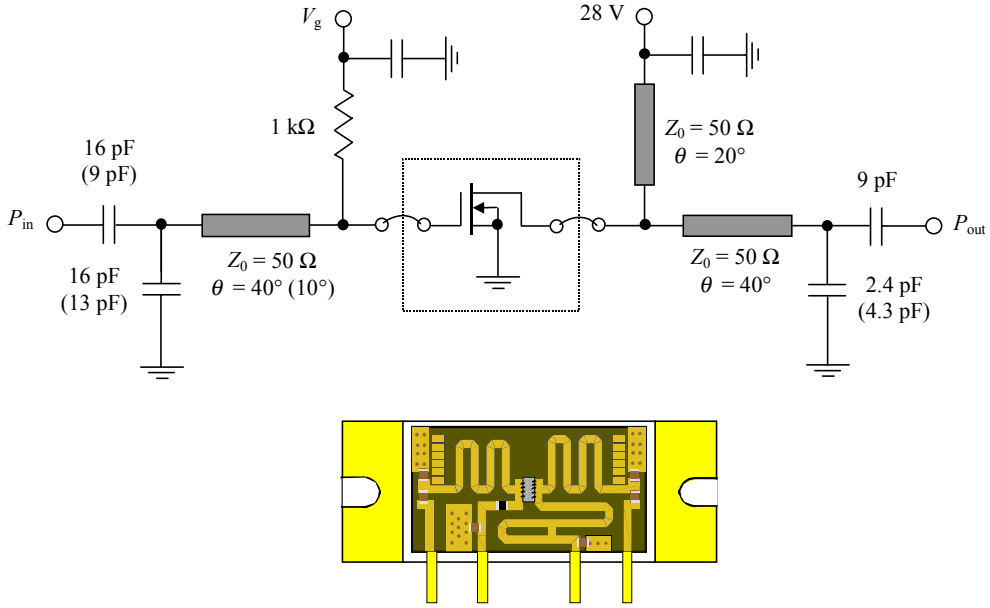


Fig. 12. Circuit schematic and module design of single-stage 500 MHz parallel-circuit Class E high-voltage LDMOSFET power amplifier

In Figure 12, the circuit schematic and module design of the single-stage 500 MHz parallel-circuit Class E high-voltage LDMOSFET power amplifier with supply voltage V_{cc} = 28 V, output power P_{out} = 22 W, linear power gain G_P = 15 dB and power-added efficiency PAE = 67% is shown. The input and output matching circuits represent the T-transformers with series 50-ohm microstrip lines designed using 16-mil FR-4 substrate. The required load network phase angle is provided with the device output capacitance and parallel 50-ohm microstrip line of 25-degree electrical length. Overall size of hybrid module is 45x20 mm^2 with eutectic attached 1.25-µm LDMOSFET die size of 4-cm total gate width, which is connected to the board by four bond wires to the input microstrip line and five bondwires of 1.5-mm length each to the output microstrip line. For the experimental test board fabricated on epoxy glass copper-clad laminate substrate with 50-ohm transmission line of 3-mm width, the same output power was achieved with the increased power-added efficiency of 76%. However, for 900 MHz 28 V LDMOSFET power amplifier module with output power P_{out} = 20 W and linear power gain G_P = 13 dB, the maximum PAE of only 50% was obtained. The matching circuit parameters of this hybrid module is shown in Figure 11 in parenthesis. The lower value of PAE can be explained by an increased inluence of the output

bondwire inductance giving the reduced optimum values of the required output capacitance and load resistance. Besides, according to equation (50) the maximum frequency for parallel-circuit Class E mode with the device output capacitance C_{out} = 15 pF is equal to 136 MHz, which is too low for 900 MHz operating frequency.

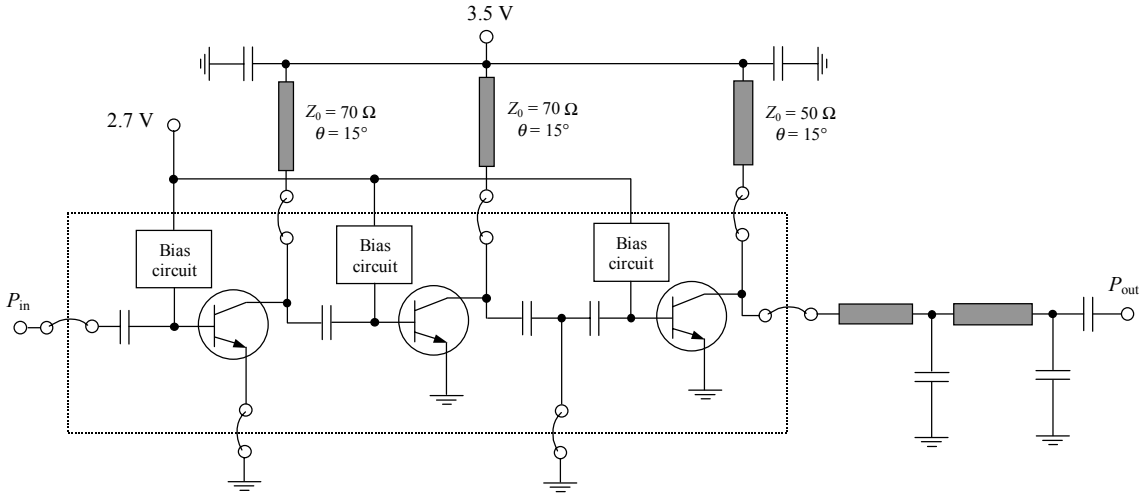


Fig. 13. Circuit schematic of high-efficieny low voltage three-stage dual-band DCS1800/PCS1900 power amplifier

In Figure 13, the circuit schematic of three-stage dual-band DCS1800/PCS1900 power amplifier intended for handset cellular transmitter application is shown. The InGaP/GaAs HBT MMIC (dotted box) contains the RF devices, input matching ciruit, two interstage matching circuits and three bias circuits on a die of 1.1 mm^2 size The emitter areas of the first, second and third devices are 180 μm^2, 900 μm^2 and 5760 μm^2, respectively, corresponding to a median time to failure (MTTF) greater than $8 \cdot 10^5$ hours at the desired power level. The MMIC, packaged in a 3 x 3 mm FQFP package, was mounted on a FR4 substrate, which contains the output matching circuit and microstrip transmission lines connnected to the 3.5 V voltage supply from each device collector. The output matching circuit was built up according to the optimum values from a detailed circuit simulation. Standard ceramic chip capacitors were used, and no more additional tunig was done. As a result, in a frequency range 1.71-1.91 GHz the minimum power gain of 33 dB, output power of minimum 32.5 dBm, collector efficiency of 57% and *PAE* of 47% were obtained. It should be noted that the simulated results with accurate values of the capacitances in the output matching circuit demonstrated the collector efficiency of 68% and *PAE* of 57%, respectively. As an example of close proximity to the idealized switched-mode parallel-circuit Class E mode, the appropriate simulated collector voltage and current waveforms for supply voltage V_{cc} = 5 V are shown in Figure 14(*a*) and Figure 14(*b*), respectively. During off-state operation mode only the current flowing through the device collector capacitance defines the total collector current. The small deviation from the ideal waveforms can be explained by violation of the required optimum impedance

conditions due to the transmission-line effect at the second and higher-order harmonics and device finite switching time and parasitics.

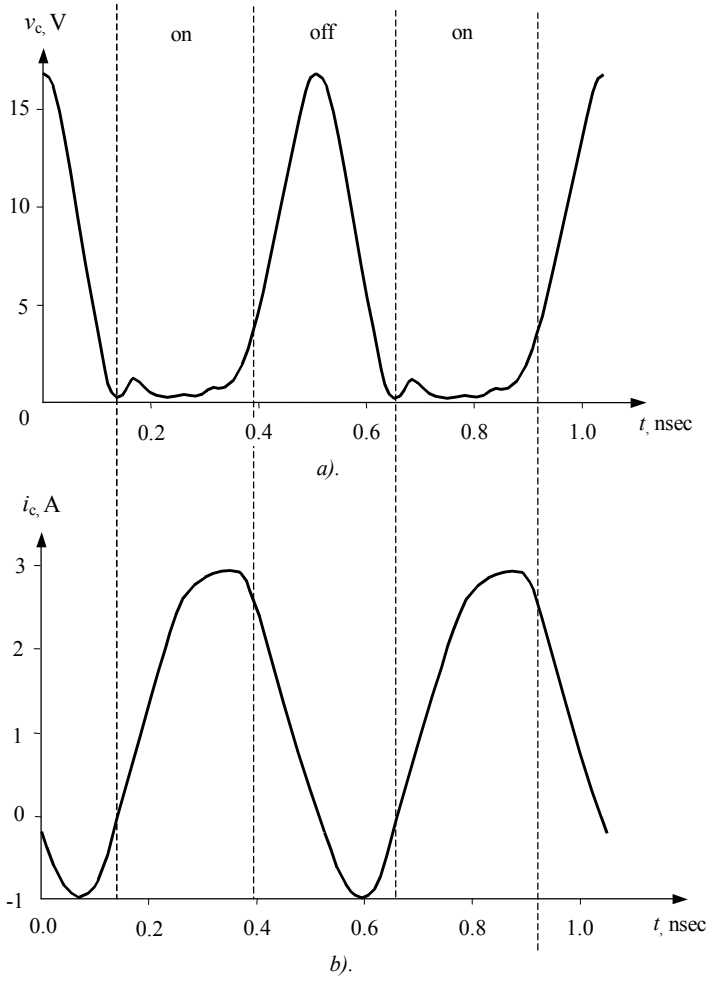


Fig. 14. Simulated (*a*) collector voltage and (*b*) current waveforms of transmission-line parallel-circuit Class E low-voltage InGaP/GaAs HBT power amplifier

X. CONCLUSIONS

The switched-mode second-order Class E configuration with a generalized load network including the shunt capacitance, series bondwire inductance, finite DC feed inductance and series *LC* circuit is analytically defined with a set of the exact design equations. Based on these equations, the required voltage and current waveforms and circuit parameters are determined for both general case and particular circuits corresponding to Class E with shunt capacitance, even harmonic Class E and parallel-circuit Class E configurations. The effect of the device output bondwire inductance on the optimum circuit parameters is demonstrated. The operating power gain achieved with the parallel-circuit Class E power amplifier is evaluated and compared with the operating power gain of the conventional Class B power amplifier. A possibility of the load network implementation at microwaves also is considered. Two examples of high power LDMOSFET and low-voltage HBT power amplifiers, utilizing a transmission-line parallel-circuit Class E circuit configurations, are presented.

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