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Statistical Analysis of Microwave Circuits Predicts Real World Performance

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Manufacturing yield can be improved with statistical analysis at the simulation level, to identify and correct for performance variations due to component and process tolerances.

Obtaining acceptable and predictable circuit performance can be very challenging with all the component tolerances and manufacturing variations involved. The variations can be due to specific processes or discrete components used in circuit design. For robust circuit and system design these variations need to be accounted for and examined during the circuit or system simulation stages to help designers gain confidence in quality of the design. This type of simulation is commonly referred to as *statistical analysis*. This article outlines the intricacies of statistical analysis and makes designers aware of the various types of statistical analyses which can be performed to gain additional confidence during the design process. To illustrate the various statistical simulations, a MIC-based C-band amplifier design is used as an example [1].

Process Variations and Discrete Component Tolerances

There are multiple sources of variations in the real world of microwave design that can be associated with such processes and materials as dielectrics, etching, and discrete components:

1. Dielectrics: Dielectrics can have variations in their height, loss tangent and dielectric constant (ε_r) and this data can be obtained directly from manufacturer's datasheet.

2. Etching: Etching tolerance in the printed circuit process is mainly dependent upon the etching technique used. This tolerance mainly affects the width of the transmission lines:

a. The chemical etching process can have tolerance level of ±Metal Conductor Thickness (max.).

b. Reactive ion etching can produce the excellent tolerances of ±1 μm.

c. Metal deposition techniques can also produce tolerances of ±1-2 μm.

3. Discrete components: Discrete components such as inductors, capacitors, and resistors have their inherent tolerances which could affect circuit performance. Different tolerances for discrete components are summarized in Table 1.

Component Class	Tolerance
B	±0.1 (absolute)
C	±0.25 (absolute)
D	±0.5 (absolute)
F	1%
G	2%
J	5%
K	10%
M	20%

Table 1 · Tolerances for various classes of discrete components.

All of these tolerances should be included into circuit design process as far as possible so that circuit could be analyzed and optimized over these variations. In this article, a typical MIC amplifier circuit is used for statistical simulations and the variations that are considered are the etching tolerances and discrete component's tolerances to keep this article simple. Designers can then take the concepts

Standard Deviation	Confidence Level
1	68.3%
2	95.4%
3	99.7%

Table 2 · Confidence level estimates.

presented here and apply them to each variation (for example, dielectric parameter tolerances, and so on) in their processes.

The substrate which is used for amplifier design in the present text has following specifications:

- Dielectric Height: 25 mils
- Dielectric Constant: 9.9
- Loss Tangent: 7×10^{-4}
- Conductor Thickness: 8 µm
- Conductivity: 4.1×10^{7} (gold conductor)

along with typical discrete component tolerances as listed in Table1

Statistical Design

To perform a simulation that takes into account the real-world tolerance variations that can occur for a variety of reasons, designers need to understand the statistical analysis. Statistical analysis is the process of:

- Accounting for the random (statistical) variations in the parameters of a design.
- Measuring the effects of these variations.
- Modifying the design to minimize these effects.

Yield analysis is the process of varying a set of parameter values, using specified probability distributions, to determine how many possible combinations result in satisfying predetermined performance specifications.

Yield is the unit of measure for statistical design. It is defined as the ratio of the number of designs that pass the performance specifications to the total number of designs that are produced. It also can be thought of as the probability that a given design sample will pass the specifications.

Because the total number of designs produced may be large or unknown, yield is usually measured over a finite number of design samples or trials in the process known as yield estimation. As the number of trials becomes large, the yield estimate approaches the true design yield. Parameter values that have statistical variations are referred to as yield variables.

There are three statistical design options which designers can use to analyze their circuits: *Monte Carlo analysis*, *Yield Analysis* and *Yield Optimization*.

Confidence=68.3%			**Actual Yield=90%**
Error ±%	Estimated % yield		Number of Trials
	Low	High	
1	89	91	900
2	88	92	225
3	87	93	100
4	86	94	56
5	85	95	36
6	84	96	25
7	83	97	18
8	82	98	14
9	81	99	11
10	80	100	9
Confidence=95%			**Actual Yiel**d=90%
Error ±%	Estimated % yield		Number of Trials
	Low	High	
1	89	91	3457
2	88	92	864
3	87	93	384
4	86	94	216
5	85	95	138
6	84	96	96
7	83	97	70
8	82	98	54
9	81	99	42
10	80	100	34
Confidence=99%			**Actual Yield=90%**
Error ±%	Estimated % yield		Number of Trials
	Low	High	
1	89	91	5967
2	88	92	1491
3	87	93	663
4	86	94	372
5	85	95	238
6	84	96	165
7	83	97	121
8	82	98	93
9	81	99	73
10	80	100	59

Table 3 · Confidence tables for yield analysis.

Monte Carlo Analysis

Monte Carlo yield analysis methods have traditionally been widely used and accepted as a means to estimate yield. The method simply consists of performing a series of trials. Each trial results from randomly generating yield variable values according to statistical-distribution specifications, performing a simulation, and evaluating the result against stated performance specifications.

The power of the Monte Carlo method is that the accuracy of the estimate rendered is independent of the number of statistical variables and requires no simplifying assumptions about the probability distribution of either

component parameter values or performance responses.

The weakness of this method is that a full network simulation is required for each trial, and that a large number of trials are required to obtain high confidence in an accurate estimate of yield.

Monte Carlo Trials and Confidence Levels

Here's how to calculate the number of trials necessary for a given confidence and estimate error. The confidence level is the area under a normal (Gaussian) curve over a given number of standard deviations. Common values for confidence level are shown Table 2.

Error is the absolute difference between the actual yield, Y, and the yield estimate, $\tilde{Y}$, given by:

$$E = |Y - \tilde{Y}|$$

where E is the percent error. The low value limit of $\tilde{Y}$ is given by:

$$\tilde{Y} = Y - E$$

The sample or trial size, N, is then calculated from:

$$N = \left(\frac{C_\sigma}{E}\right)^2 Y(1 - Y)$$

where, C_σ is the confidence expressed as a number of standard deviations.

Example

For a 95.4% confidence level, i.e. Standard Deviation = 2, Error = ±2% and a yield of 80%,

$$N = \left(\frac{C_\sigma}{E}\right)^2 Y(1 - Y)$$

N = 1600 trials

Yield Analysis

This process involves simulating the design over a given number of trials in which the yield variables have values that vary randomly about their nominal values with specified probability distribution functions. The numbers of passing and failing trials are recorded, and these numbers are used to compute an estimate of the yield. In a nutshell, yield is the percentage of circuits that meet the desired specifications, set as the Goal.

Yield analysis is based on the Monte Carlo method. A series of trials is run in which random values are assigned to all of design's statistical variables, a simulation is performed, and the yield specifications are checked against the simulated measurement values. The number of passing and failing simulations is accumulated over the set of trials and used to compute the yield estimate.

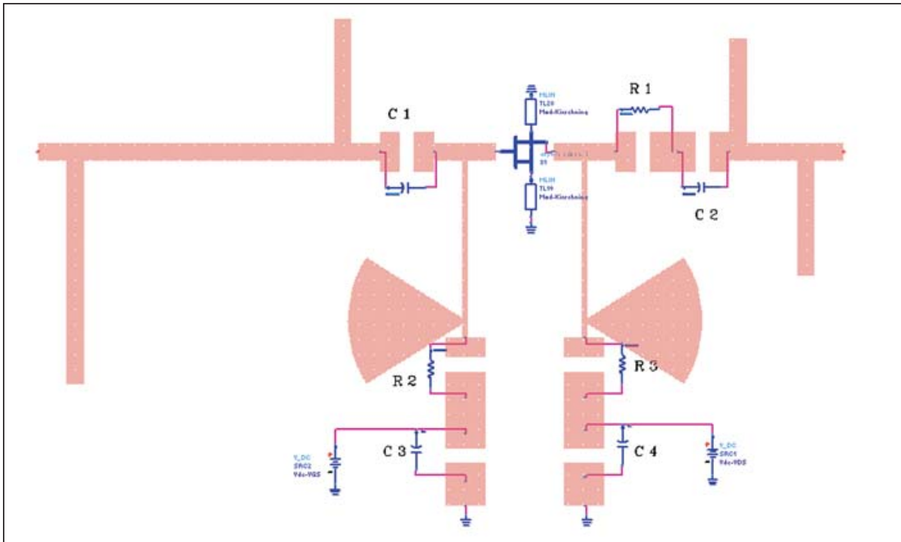

Figure 1(a) · Complete amplifier layout.

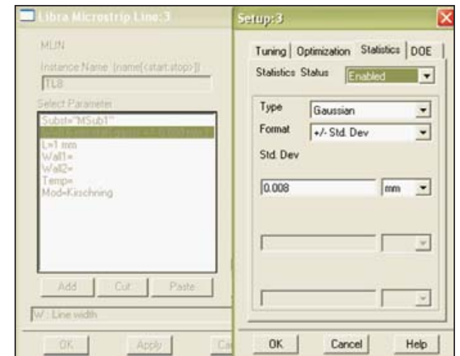

Figure 1(c) · Statistical variation definition setup for transmission lines.

Confidence Tables

The confidence tables that can be followed to determine the number of trials suitable for yield analysis for different confidence levels and yield of 90% are shown in Table 3. For more tables designers can refer to the software documentation [2].

Yield optimization

Yield optimization adjusts nominal values of selected element parameters to maximize yield. Also referred to as *design centering*, yield optimization is the process in which the nominal values of yield variables (component values and process parameters) are adjusted to maximize the yield estimate.

To have control over the confidence level and hence the accuracy of the yield estimate, it is recommended that designer perform a yield analysis after the yield optimization is completed, using the nominal parameter values obtained from the yield optimization. Appropriate number of trials can be chosen based upon the formula mentioned earlier.

It is not possible to perform statistical analysis without a good simulation tool. Without good software statistical analysis can also be time consuming because of the large number of trials involved. The simulation tool should have the capability to perform yield analysis, Monte Carlo analysis, and yield optimization, which designers can use to make sure that the designed circuit can tolerate real-world variations.

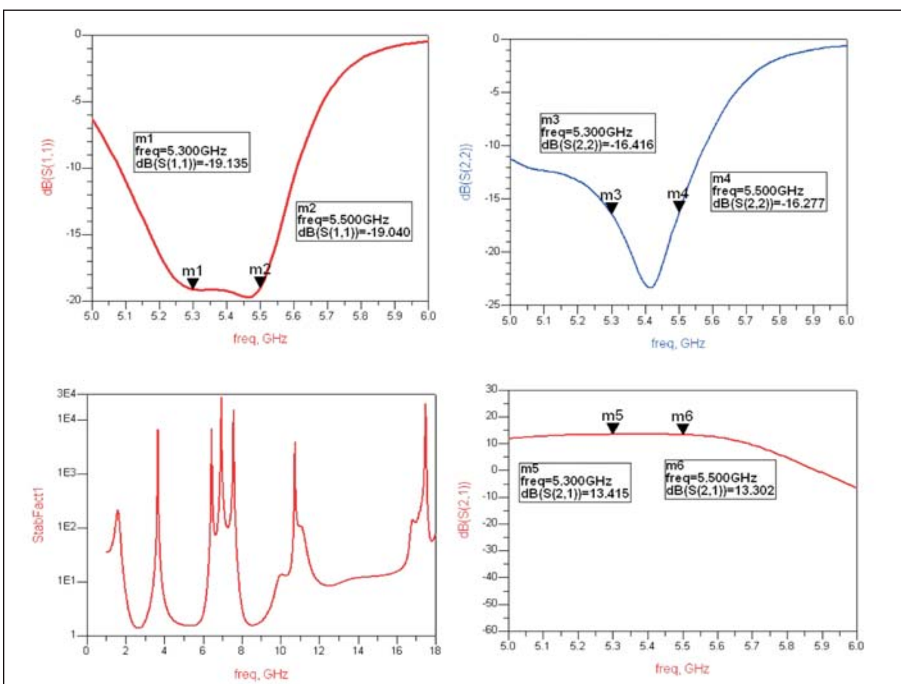

Figure 1(b) · Optimized amplifier performance.

Analysis of a C-band MIC Amplifier

Figure 1(a) shows complete schematic design for C-band MIC amplifier, and Figure 1(b) shows optimized circuit performance. The amplifier specifications are:

- Frequency Band: 5.3 - 5.5 GHz
- Gain: 13 dB (min)
- Input Return Loss: ≤15 dB
- Output Return Loss: <–15 dB

The amplifier is designed over a 25-mil alumina substrate as mentioned previously, and considering the chemical etching process, the maximum etching tolerance would be

Component	Value	Tolerance	Purpose
R1	24 ohm	5%	Stability
R2	300 ohm	5%	Stability (Input Bias Line)
R3	10 ohm	5%	Stability (Output Bias Line)
C1	2 pF	±0.1 pF	Coupling Capacitor (Input)
C2	2 pF	±0.1 pF	Coupling Capacitor (Output)
C3	560 pF	10%	Bypass Capacitor (Input)
C4	560 pF	10%	Bypass Capacitor (Output)

Table 4 · Discrete components tolerance table.

Figure 2 · Yield analysis setup for statistical analysis in simulation.

~±8 µm. It also uses few discrete components, as given in Table 4. Three steps are needed to perform statistical analysis:

a. Define tolerance on the components/transmission lines
b. Set up the performance yardstick to be met
c. Define the number of trials and selection of statistical analysis method (Monte Carlo or yield analysis)

All the transmission line widths were given a statistical variation of ±8 µm using a Gaussian distribution function, and all the discrete components were provided with the tolerances mentioned in Table 4. The performance yardstick is the amplifier specifications, set up as shown in Figure 2.

The number of trials was set at 5000, and the yield analysis method was selected to view the pass percentage after the statistical analysis. The initial results obtained are shown in Figure 3, which depicts the yield percentage to be 81 percent, which is pretty good for a first iteration. Figure 3 also shows number of circuits which passed the required specification and number circuits which failed during the specifications.

Yield	NumFail	NumPass
80.940	953.000	4047.000

Figure 3 · Initial yield analysis results, which do not indicate an acceptable yield.

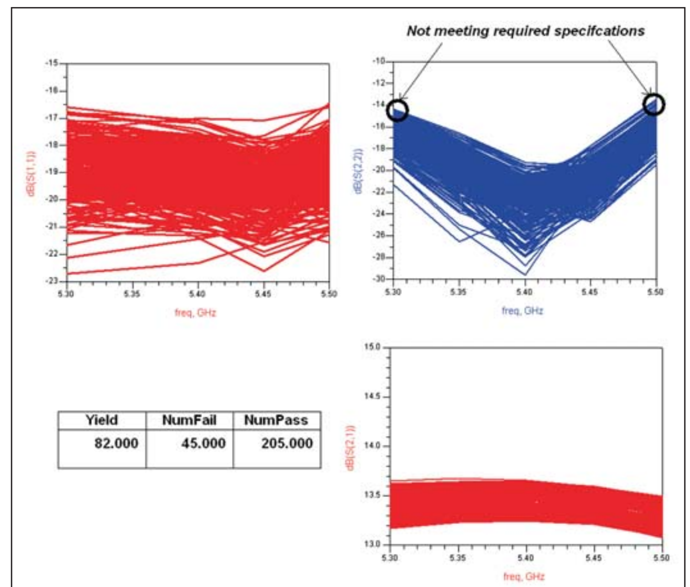

Figure 4 · Yield analysis results (250 iterations).

For production type circuits this yield should be increased to at least 90-95 percent after running the initial yield analysis designer has the choice to perform the yield optimization or sensitivity analysis over the circuit to improve the yield. (This is not discussed in this article.) The designer with a little bit of experience can also take an alternative approach to find the reason for lower yield and once the reason is known the circuit can be modified circuit a bit in order to improve the yield of the circuit.

To determine the reason for lower yield, another yield analysis was performed with 250 iterations. Data for each iteration was saved to take a closer look at the specifications which were not being met, shown in Figure 4.

We can see from Figure 4 that Input Return Loss and

Yield	NumFail	NumPass
98.500	75.000	4925.000

Figure 5 · Yield analysis results with a new S_{22} goal of –14 dB.

Gain specifications did not contribute to lower yield. The main culprit for lower yield is the Output Return Loss, which is slightly below the desired specifications on the lower and upper band edges. Designers can perform yield optimization to center the design to account for these statistical variations.

On the other hand, taking a closer look at the results provided in Figure 4, although the yield percentage figure does not look good as a percentage, the output return loss is just a fraction lower than the required specifications, so another round of yield analysis was performed with target specification for output return loss (S_{22}) relaxed to –14 dB and excellent yield of 98.5 percent was obtained, which is shown in Figure 5.

Conclusion

Performing yield analysis is pretty essential for production type circuits. Sophisticated simulation tools give designers the flexibility to perform complex statistical simulations that allow designers to increase the reliability of their circuits.

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