Broadband SiGe Monolithic Microwave Control Circuits

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A current SiGe process was used to fabricate phase shifter and switch circuits for phased array radar applications, requiring special attention to the characteristics of the PIN diodes

This paper reports the performance of several broadband SiGe monolithic microwave control circuits suitable for phased array radar applications. The amplitude and phase control MMICs are based on an optimized SiGe PIN diode fabricated using the IBM 5-HP SiGe foundry process. Utilizing this diode, several control circuits were designed, including a broadband (1-20 GHz) monolithic SPDT switch, a five port transfer switch, and a 6-bit phase shifter, all operating over 7-11 GHz.

Device Design

The IBM silicon-germanium technology permits the integration of advanced MMICs, low power VLSI digital electronics and low frequency analog circuits in a single high yield process. The availability of several high performance microwave passive and active devices on the same wafer, including SiGe HBTs, PINs and varactors, etc., makes the IBM SiGe technology an exciting paradigm for innovative circuits for RF and microwave communication systems.

Fundamental to the success of any microwave control function is a high performance PIN device. The performance of the PIN is dependent on its material doping profile as well as its layout. In the IBM 5HP SiGe process, the doping profile of the PIN diode is closely linked to that of the HBT through sharing of three HBT material layers, namely, the buried N+ sub-collector layer, the N-collector layer and finally the P+ SiGe base layer.
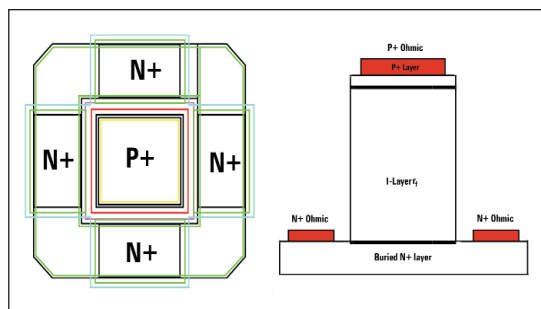

Figure 1 · SiGe vertical PIN diode (dimensions 7 x 7 μm).

These layers have been used to form the cathode, the I-region, and the anode of the PIN diode, respectively. The material profile in IBM 5HP process is optimized for achieving a high F_t HBT performance which somewhat limits its collector thickness and, consequently, the PIN's I-region thickness to approximately one-half micron. Since the material profile of the PIN is rigid due to the HBT's performance requirements, the PIN layout design should be optimized to achieve optimum microwave performance. Figure 1 shows the layout of such a vertical optimized PIN design having a square anode contact that is surrounded by a continuous cathode contact. Such a device has a periphery-to-area ratio of only 0.56, an important design factor for minimizing the device forward bias microwave resistance (R_f).

The forward bias resistance of the PIN diode (R_f) is the sum of the current independent contact resistance (R_c) and current dependent resistance (r_f), caused by the conductivity modulation of the intrinsic region. The current dependent resistance is due to the injection of the holes and electrons into the
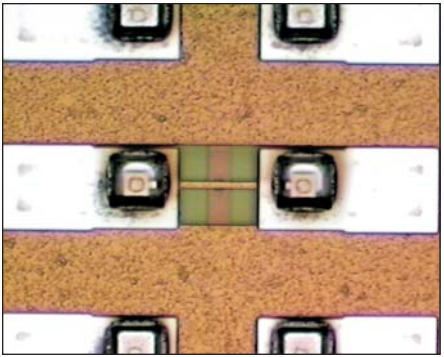
Figure 2(a) · Shunt SiGe PIN diode across 50 ohm CPW lines.
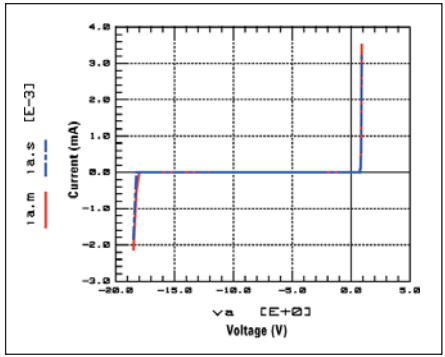

Figure 2(b) · Measured and modeled (using ICCAP) DC-IV characteristics of the shunt diode (80).
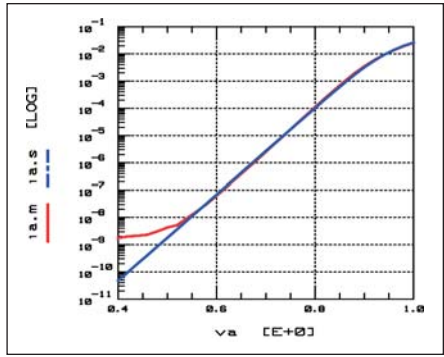

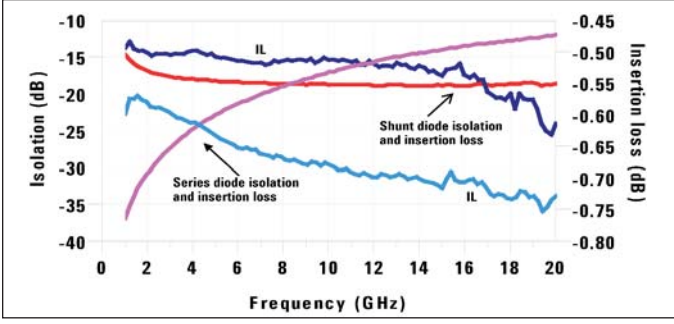Figure 2(c) · Measured and modeled (using ICCAP): log *I* (A) vs. voltage (V).

Figure 2(d) · Microwave performance of series and shunt diodes (I_f = 2 mA, V_f = 1.0V, V_r = –1 V).
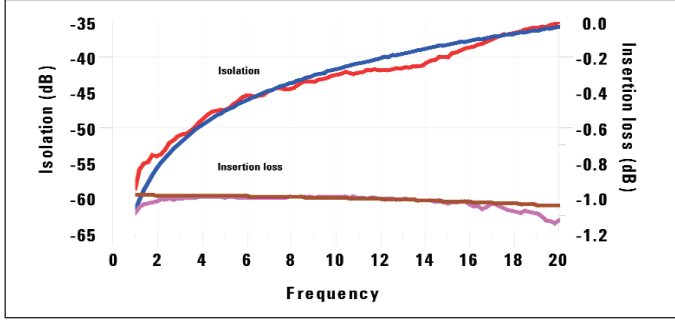

Figure 2(e) · Measured and modeled (using ADS) performance of an integrated series-shunt diode (I_f = 2 mA, V_f = 1.0 V, V_r = –1 V).

PIN Area μm^2	IL (dB) 10 GHz	Iso. (dB) 10 GHz	C_j (fF) –1 V	R_f (W) V_f = 1 V
80 Shunt	0.5	18.0	32	3.5 @ 2 mA
50 Series	0.7	18.0	20	9.0 @ 2 mA

Table 1 · Measured performance and extracted C_j and R_f values.

intrinsic region from the forward biased P^+ and N^+ contact regions. This resistance is given by:

$$r_f = \frac{l_i^2}{2\overline{\mu}\tau I_{DC}} \tag{1}$$

Where l_i is the thickness of the intrinsic region; $\overline{\mu}$ is the average electron and hole mobility; and (τ) is the minority carrier life time.

Device Performance

Figure 2(a) illustrates a fully fabricated 80 μm^2 shunt device in a 50 ohm system. As it can be seen, the buried

PIN is accessed by six vias that connect the device terminals to the input-output launching pads. The transmission lines are formed on a 15-micron thick polyimide layer that is deposited on the surface of the SiGe substrate. Good agreement has been obtained between the modeled and the measured DC current-voltage characteristics of the diode as shown in Figures 2(b) and 2(c). The diode follows a parallel plane diode behavior, given by Eq. (2), over seven orders of magnitudes.

$$I = I_s\left(\exp\left(\frac{qV}{nKT}\right) - 1\right) \tag{2}$$

The measured and modeled data on saturation current (I_s), the ideality factor (n), and the junction revere breakdown voltage (V_b) are found to be: $I_s = 1.2 \times 10^{-17}$, $n = 1.1$ at $T = 300K$, and $V_b = 18$ V. The value of (n) has a significant effect on the performance of the PIN diode [1-3].

Figure 2(d) illustrates the RF performances for typical 50 μm^2 and 80 μm^2 diodes when placed across or in series with 50 ohm CPW input-output transmission lines. As can be seen, good broadband performance has been obtained for both series and shunt devices at a low dissi-
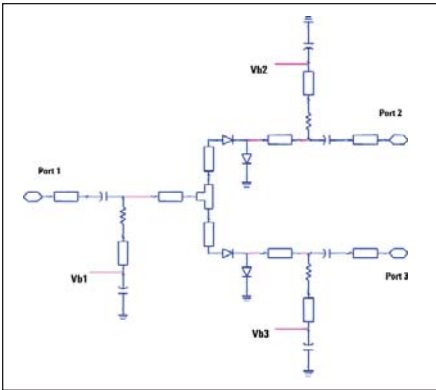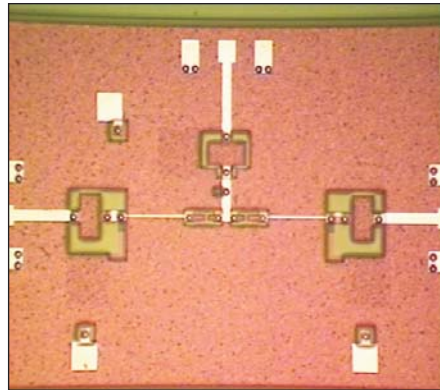
Figure 3(a) · SPDT switch chip schematic.

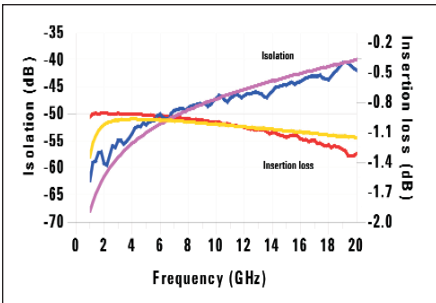Figure 3(b) · SiGe SPDT switch chip (1.0 × 0.42 mm).

Figure 3(c) · Measured and modeled (using ADS) SPDT switch performance.
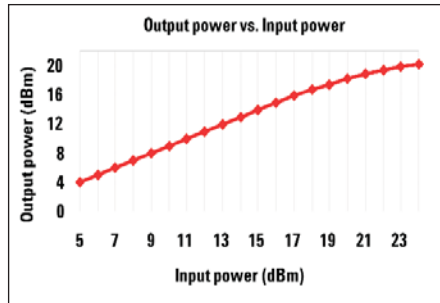

Figure 3(d) · Switch input power at 1-dB compression.

Figure 4(a) · Transfer switch schematic.

Figure 4(b) · Transfer switch chip (3.2 × 1.4 mm).

pation power of 2.0 mW. Table 1 summarizes the extracted values for junction capacitance and the total forward biased resistance (R_f) for both devices.

The measured and modeled performance for a typical integrated series-shunt diode pair (50 series, 80 shunt) is shown in Figure 2(e). To achieve a broadband RF operation for this structure, the distance between the two diodes was set to approximately 10, thereby minimizing its associated parasitics.

Broadband (1 to 20 GHz) SPDT Switch

The series-shunt integrated diode structure described above was used to design a broadband SPDT switch with on-chip resistive biased networks that operates over 1 to 20 GHz bandwidth. All aspects of the circuit design and device modeling were performed using Agilent ADS simulators [4]. Figure 3(a) shows the SPDT switch schematic having a series-shunt diode combination in each arm. This topology was chosen as the best compromise between minimizing the insertion loss and maximizing the switch isolation. On-chip resistive bias networks were also employed to ensure broadband switching performance and smaller chip size as illustrated in Figure 3(b).

The 1500 ohm bias resistors in this design use 340 ohms per square polysilicon thin film resistors and the MIM capacitors are based on 0.7 fF/µm^2 thin dielectric film (SiO$_2$) capacitors. Referring to Figure 3(a), a through-path between ports 1 and 2 exists when V_{b2} = –6.8V and V_{b1} = 0, causing the series diode to become forward biased at 2 mA while the shunt diode is reversed biased. Similarly, an isolation path exists between ports 1 and 3 when V_{b3} is set at (3.8 V, 2 mA). The total DC power consumption for this design is only around 22 mW for a typical switch. As shown in Figure 3(c), a through-path loss of 0.9 to 1.3 dB and an isolation path loss of 60 to 40 dB over a wide frequency range (1 to 20 GHz) have been measured. Also shown is the close agreement obtained between the switch measured and simulated data. A similar chip without the on-chip resistive bias networks was also measured, requiring only 4.0 mW of DC power for maintaining the same switch performance.

The input port power handling capability of the switch is shown in Figure 3(d) indicating the 1-dB insertion loss compression point occurs at around 19 dBm when mea-
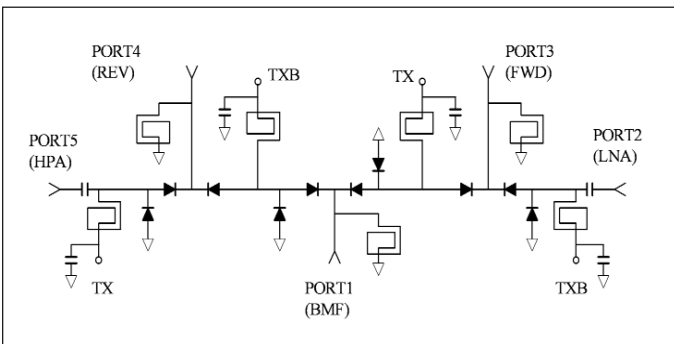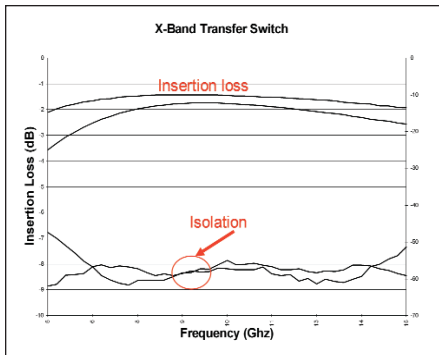
Figure 5(a) · Switch measured insertion loss and isolation.
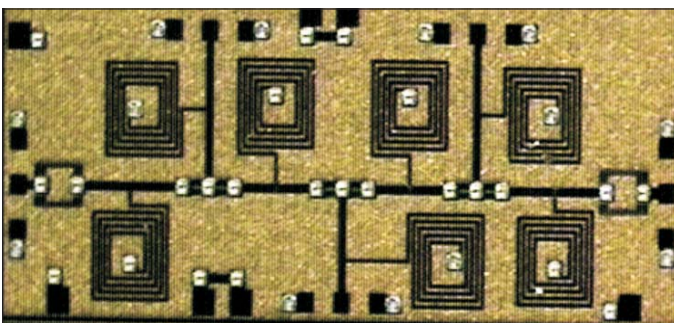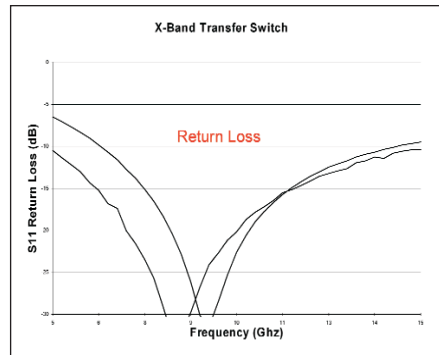

Figure 5(b) · Switch measured return loss.

Figure 6 · 180/90 degrees and 45/22.5 degrees phase 2-bit schematic.

Figure 7 · 11.25/5.625 degrees phase bit schematic.

sured under the nominal bias condition described above. The switching speed and the third order intercept point were both evaluated at 10 GHz. The switching speed was found to be less than one nanosecond and the third order intercept point around 30 dBm at –3 dBm input RF power.

X-band SiGe MMICs

IBM's SiGe BiCMOS 5HP process offers the potential to integrate high levels of microwave circuitry with analog and digital circuits. Microwave functions traditionally performed by gallium arsenide MMICs can now be combined with the analog/digital functions of silicon based ASICs on a single chip. As an example of higher microwave integration levels, several X-band SiGe MMICs, including a transfer switch, a 6-bit phase shifter, a 5-bit attenuator and a variable gain cascode amplifier, is described in this section. The post SiGe topside process is described in details in the section "Topside Polyimide Technology."

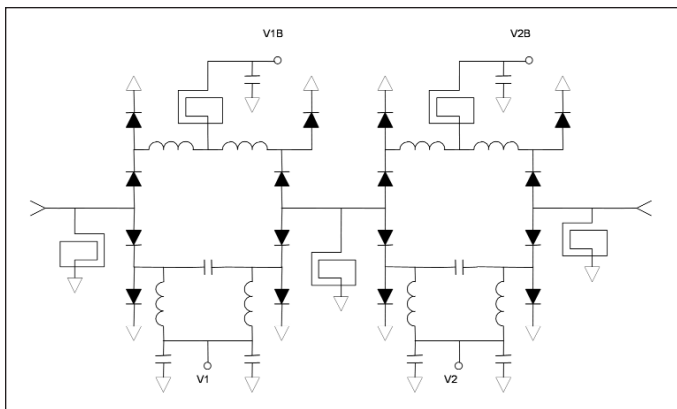*Transfer Switch*—Figure 4(a) shows the circuit schematic of a 5-port transfer switch containing 10 optimized SiGe PIN diodes. The circuit design is suitable for applications where Common Leg Circuit (CLC) architecture [5] is employed for the realization of phased array T/R modules. In the CLC topology, the transfer switch would enable the amplifier gain control and phase control circuitries to be shared by both transmit and receive signal paths. The switch design is based on a series-shunt 50 diode combination as the best compromise between minimizing the insertion loss and maximizing the switch isolation. The simplicity of the circuit design is the result of the low parasitic capacitance and resistance of the SiGe PIN diodes leading to a compact chip size shown in Figure 4(b). The switch measured insertion loss, isolation, and return loss are shown in Figures 5(a) and 5(b). The transfer switch demonstrates a path loss of 1.4 to 2.1 dB and an isolation of >55 dB across 7 to 11 GHz. The measured input and output return losses are better than 10 dB over the same frequency band (Figure 5(b)).
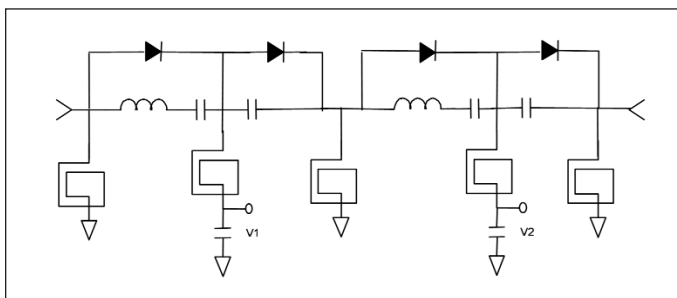
6-bit Phase shifter—The phase shifter design consists of six digital bits (180, 90, 45, 22.5, 11.25 and 5.625 degrees) cascaded in a linear arrangement. This provides 64 phase states between 0 and 360 degrees, in increments of 5.625 degrees. The 180, 90, 45 and 22.5 degree phase bits switch between Pi- and/or T-type high-pass/low-pass phase shift networks using two single pole double throw PIN diode switches. The 11.25 and 5.625 degree phase bits use a simplified topology of capacitive and inductive elements to achieve their phase shifts [6]. These phase bit topologies are selected due to their broad bandwidth performance and relative insensitivity to process variations. The schematics for these phase bit circuits are shown in Figures 6 and 7.

SiGe PIN diodes (7 × 7 mm) are used for switching functions. Diode biasing is provided through spiral inductors in combination with MIM bypass capacitors. The 180, 90, 45 and 22.5 degree phase bits require two complementary bias inputs of ±1 V. The 11.25 and 5.625 degree phase bits use the same voltages but require a single bias input.
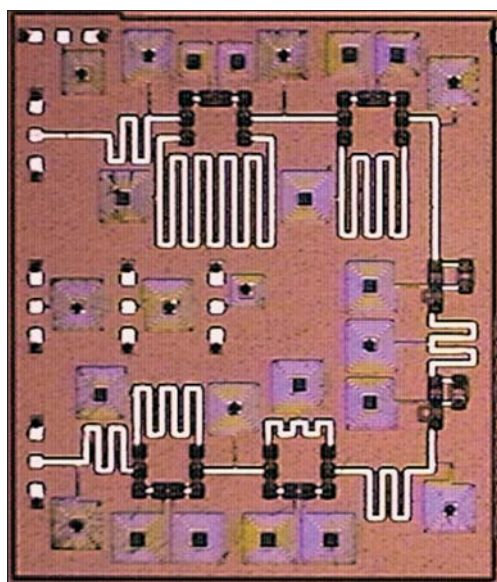
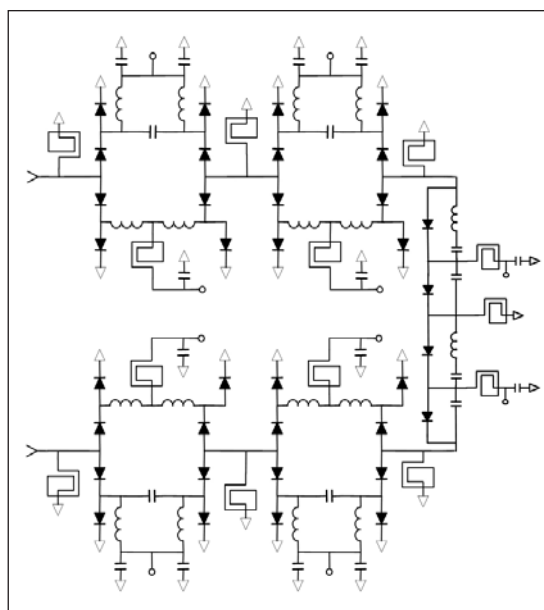**Figure 8(a) · 6-bit phase shifter chip (3.8 × 3.8 mm).**

Figure 8(b) · 6-bit phase shifter circuit.

conductive silicon substrates. Therefore, to realize a low loss medium for transmission lines (TRLs), a topside polyimide process has been developed. In the standard IBM 5HP SiGe process, there are five levels of AlCu interconnect metalization. The top-most layer of this metal system is used as a RF ground-plane for the microstrip transmission lines in a polyimide process. Such a ground-plane must have openings to allow connections between the TRLs above and the active and passive devices below.

The completed 6-bit phase shifter chip and its associated circuit topology are shown in Figures 8(a) and 8(b). Programmable current sources were used to bias each on-state diode at 2.5 mA. Total current for the phase shifter was 45 mA. Figures 9 through 11 summarize the measured performance of the primary phase states over 5 to 15 GHz, where 7 to 11 GHz is the design band. In the reference state, all phase bits were switched to their high-pass state. At 9 GHz, the measured output 1 dB gain compression is 3 dBm with a TOI of 17 dBm. Post measurement simulations indicate that the overall circuit performance can be improved with additional topside technology improvement leading to improved circuit loss for spiral inductors, transmission lines and input/output (I/O) connections of the phase shifter.

Topside Polyimide Technology

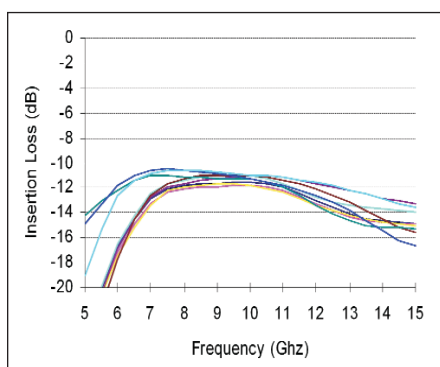The present IBM SiGe BiCMOS IC process is based on

The first step to create MMICs from the completed Si wafers is to deposit a polyimide layer on top of the ground-plane metalization layer (top metal). After polyimide deposition, vias are etched to contact devices below the ground plane. The polyimide thickness is 15 microns. Figure 12 shows the cross-sectional view of the IBM Si based MMICs using microstrip TRLs on polyimide. As shown in Figure 13, the transmission line loss for a typical 50 ohm microstrip line on polyimide is about 1.20 dB/cm at 10 GHz.

Conclusion

The design and measured performance of several broadband SiGe MMICs including a broadband (1 to 20 GHz) monolithic SPDT switch, a five port transfer switch, and a 6-bit phase shifter, all operating over 7 to 11 GHz, are described. The amplitude and phase control MMIC designs are based on an optimized SiGe PIN diode. The broadband
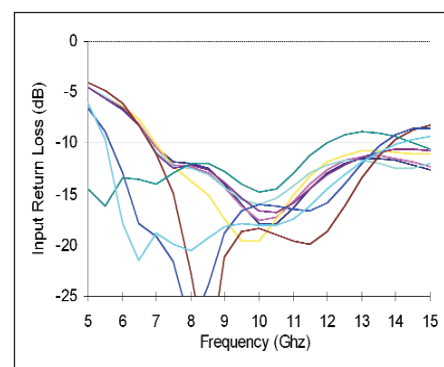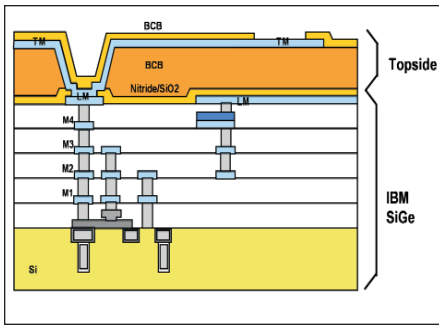

Figure 9 · Measured phase shifter insertion loss.

Figure 10 · Measured phase shifter phase performance.

Figure 11 · Measured phase shifter input return loss.

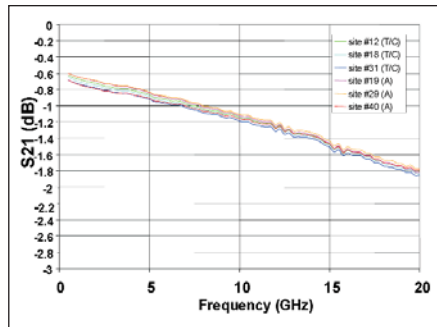Figure 12 · Cross-sectional view of the topside process.

Figure 13 · Loss vs. frequency for 50 ohm, 1 cm TRLs on 15.0 µm polyimide.

(1-20 GHz) resistive bias SPDT switch "ON" arm demonstrates a path-loss of less than 1.3 dB while its "OFF" arm maintains an isolation of greater than 40 dB across 1 to 20 GHz while consuming only 22 mW of DC power. The switching speed, the 1-dB insertion loss compression point and the third order intercept point were found to be <1 ns, 19 dBm and 30.0 dBm, respectively. The transfer switch is a five port design containing 10 PINs and demonstrates a path loss of 1.4 to 2.1 dB across 7 to 11 GHz, the isolation over the same band is >55 dB. The 6-bit phase shifter design successfully demonstrates the feasibility of using SiGe technology for microwave phase control circuit designs. The availability of high performance PIN diodes and other microwave devices including SiGe HBTs, varactors, etc., renders the IBM SiGe technology a new and exciting paradigm for innovative circuit designs suitable for RF and microwave communication systems.

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Author Information

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