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Building a Microwave Frequency Synthesizer—Part 4: Improving Performance

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In this article, the author examines design alternatives to achieve different performance objectives such as fast switching speed or fine resolution

This series of articles continues with an analysis of PLL synthesizer design trade-offs. The simple single-loop PLL synthesizer approach exhibits various limitations and trade-offs. Thus, achieving a good performance combination (e.g., small step size and low phase noise) usually requires more sophisticated solutions. The common design trade-offs as well as various methods to improve synthesizer characteristics are discussed.

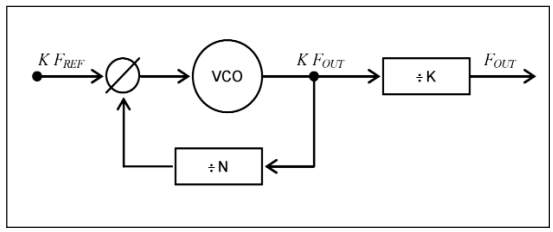

Figure 37 · A simple way to improve single-loop PLL performance.

PLL Design Trade-offs

The main PLL synthesizer parameters, such as output frequency range, step size, switching speed, spurious, and phase noise heavily depend on each other. First of all, the synthesizer switching speed is a function of its loop bandwidth, which is, in turn, defined by the phase detector comparison frequency or the step size. Thus, the smaller the step size, the slower the switching speed. Trying to increase the loop bandwidth may lead to higher reference spurs due to insufficient loop filter rejection. Clearly, increasing the phase detector comparison frequency will benefit the switching speed and spurious performance. On the other hand, for a simple single-loop PLL the phase detector frequency equals to the frequency step size and, therefore, can not be arbitrarily increased.

A simple solution to overcome this problem is presented in Figure 37. The idea is to increase both phase detector input and VCO output frequencies by K times, and then bring the synthesizer output frequency and step size down to desired numbers with an additional divider. This scheme allows higher phase detector comparison frequencies that lead to improved performance, e.g., faster tuning speed or better spur rejection. Besides, it can potentially provide better phase noise characteristics too. Although the phase detector noise normally exhibits 10log$K$ degradation with the phase detector comparison frequency increase, this degradation will be offset by a factor of 20log$K$ by the output frequency divider. Assuming that the phase detector noise dominates (in certain cases) and the loop division coefficient N remains unchanged, the scheme will demonstrate 10log$K$ overall noise improvement.

Let's step back to the general single-loop PLL case (Fig. 15). The main impact on the synthesizer performance is posted by large division ratios required to provide a high-frequency output with a fine resolution. For example, in order to get 10 GHz output with 1 MHz step size, the feedback divider ratio has to be 10000 that corresponds to 80 dB phase noise degradation. Moreover, programmable dividers are usually not available at high frequencies, thus an additional fixed divider (prescaler) is required. In this case the total

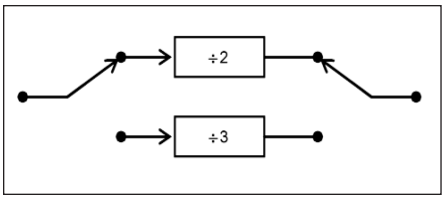

Figure 38 · The fractional division concept.

division ratio will increase by the prescaler division coefficient resulting in further phase noise degradation. Furthermore, the discrete spurs at multiples of the reference frequency tend to be proportional to the loop division ratio that leads to spurious degradation too. As a result, the simple single-loop schemes are only used in low-performance applications.

Fractional-N Techniques

In the PLL example above we assumed that the RF signal was divided by integer numbers only. Let's come back to our example where we need to synthesize some frequencies around 10 GHz with 1 MHz step size, i.e., 10.000, 10.001, 10.002, etc. Note, that we could get these numbers using 10 MHz reference if we could set the loop division coefficient to fractional numbers, i.e., 1000+0/10, 1000+1/10, 1000+2/10, etc. Thus, we would be able to reduce the maximum loop division coefficient and use a higher phase detector comparison frequency that would benefit virtually all synthesizer parameters.

How fractional division coefficients can be realized? In general it is possible by alternating two dividers (Fig. 38) and averaging the output frequency over a certain period of time. Another way to look at this process is to calculate the number of pulses delivered by this circuit for a given time interval, let's say 1 sec. Obviously, the total number of pulses depends how the processing time is split between these two dividers. Thus, the average division coefficient will be between 2 and 3 depending on how many pulses are processed by each divider.

There are a number of fractional divider implementation techniques, which are well described in [16-17]. However, for practical purpose, the fractional dividers are usually purchased parts, which are also integrated with phase detector, reference divider and other circuitry. A good example is a family of fractional-N PLL ICs from Analog Devices, which are pin-to-pin compatible with integer PLL ICs discussed in the previous part.

The main disadvantage of the fractional-N technique is excessive spurious levels due to phase errors inherent to the fractional division mechanism. Nevertheless, it is a simple and elegant solution for many applications where spurious performance is not the main concern.

Using a DDS

The DDS is another very effective solution to provide a very fine frequency resolution without a common penalty of the phase detector frequency reduction. The DDS is essentially a fractional divider that can be inserted into the reference or RF feedback path as shown in Figure 39 and Figure 40, respectively. In the first case, the DDS provides a fine-resolution and relatively high-frequency reference signal that allows reducing the loop division coefficient for a given step size. Moreover, since the DDS output can be programmed in wide limits, the loop division coefficient can be kept unchanged. Thus, a programmable divider is not required. The configuration shown in Figure 40 employs DDS as a fractional divider, whose division coefficient is set by DDS tuning command. An additional divider may be required in front of the DDS to keep its input clock frequency within specified limits. In both cases, the overall loop division coefficient is defined by the ratio between the VCO output and phase detector input frequencies.

Special attention should be paid to the DDS spurious signals, which are degraded by the loop division ratio for both configurations. A number of solutions (both hardware and software based) can be utilized to reduce the DDS spurs. Hardware techniques are usually based on upconversion of the DDS signal followed by a frequency divider as shown in Figure 41. Since the frequency mixing does not affect DDS spurs (assuming that undesired mixer products are properly filtered), the circuit reduces the DDS spurious content at 20 dB/decade rate inherent to the frequency division process. Unfortunately, it also reduces the output bandwidth, which may be a limiting factor in certain cases. The DDS bandwidth can be extended by applying more LO frequencies and filters as depicted in Figure 42 that, however, results in a higher component count similar to the direct ana-

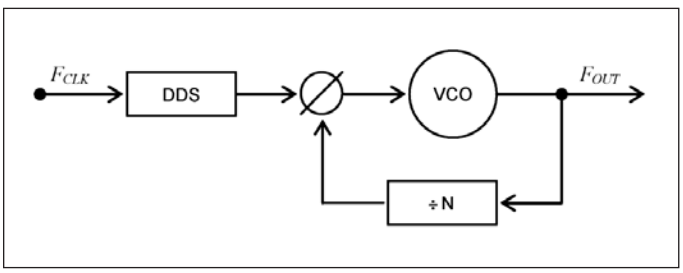

Figure 39 · Using DDS as a reference.

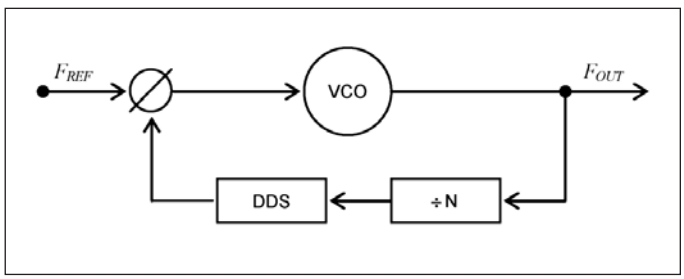

Figure 40 · Using DDS as a fractional divider.

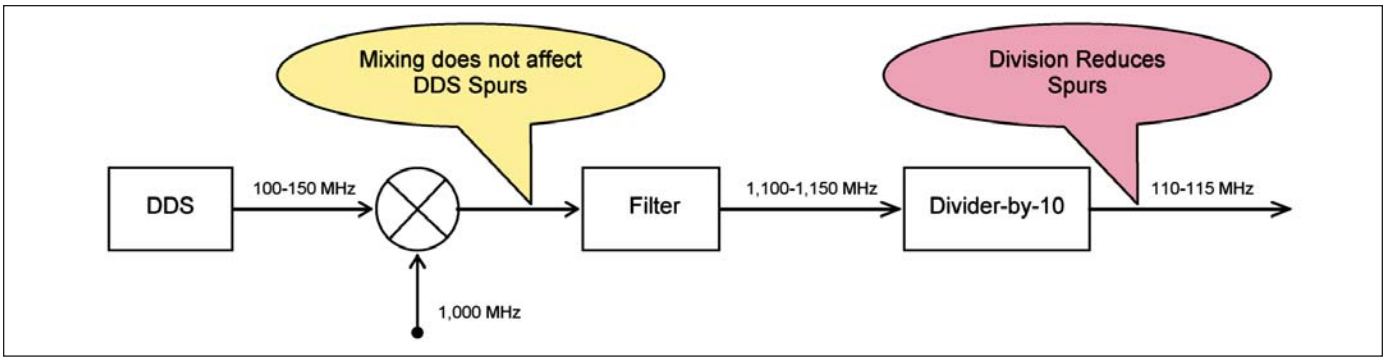

Figure 41 · DDS spur reduction.

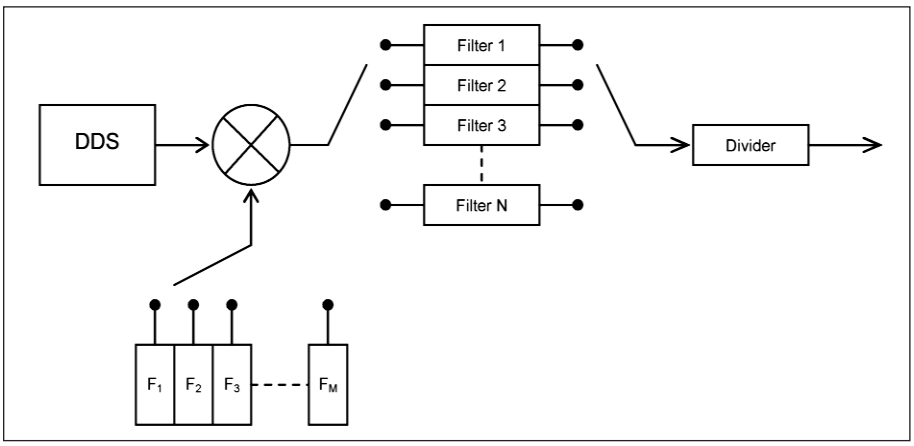

Figure 42 · DDS bandwidth extension.

log schemes.

On the other hand, software techniques involve frequency planning to move DDS spurs in the frequency domain. These techniques are based on the fact that DDS spur location is a function of its output and clock frequencies. Therefore, for a given output frequency one can move and then filter out an undesired spur by adjusting the DDS input clock frequency and frequency tuning command as shown in Figure 43. This technique can be easily combined with PLL architectures, which provide a variable clock source as well as very efficient PLL-based filtering.

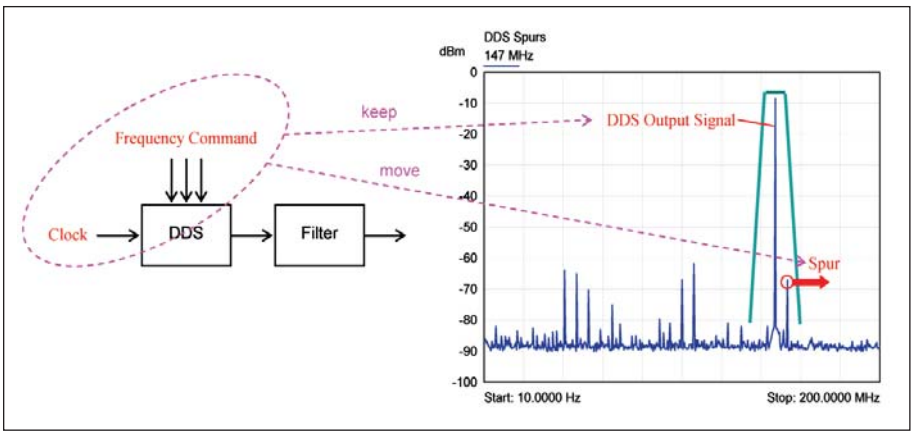

Figure 43 · DDS spur filtering.

Frequency Mixing

The synthesizer's main characteristics can be dramatically improved by employing a frequency conversion (mixing) within the synthesizer feedback path [44] as shown in Figure 44. The VCO output frequency is converted to a much lower frequency with the aid of an offset frequency source in order to minimize the maximum frequency division ratio. The offset signal can be produced using an additional PLL or a chain of frequency multipliers. An attractive solution is a harmonic mixer that utilizes multiple harmonics created by a built-in step recovery diode. This approach usually leads to a shorter bill of materials in comparison with fundamental mixing schemes; however, it is more sensitive to circuit parameters.

The offset signal can be generated within the same PLL (Fig. 45) by adding two programmable dividers at the mixer terminals as suggested in [45]. This scheme allows fractional division coefficients that can lead to the overall performance improvement.

One of the problems associated with any frequency-mixing scheme is a possible false lock due to undesired mixing products. This type of failure requires a sufficiently accurate coarse-tuning mechanism. A digital-to-analog converter (DAC) may be included to coarse-tune the VCO to approximately the correct frequency as shown in Figure 46. This acquisition aid requires linear (and repeat-

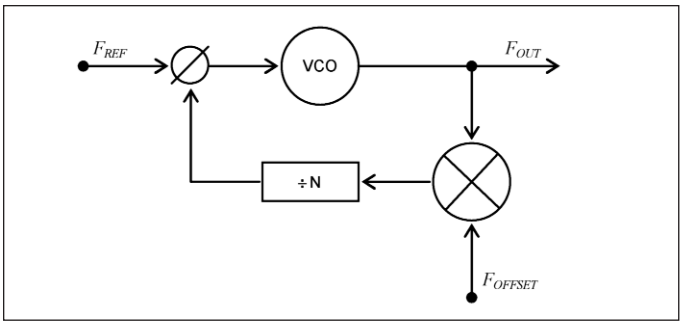

Figure 44 · Frequency mixing within RF feedback path.

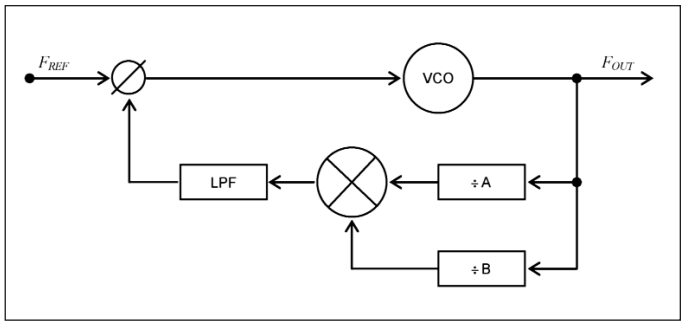

Figure 45 · Self-offset loop.

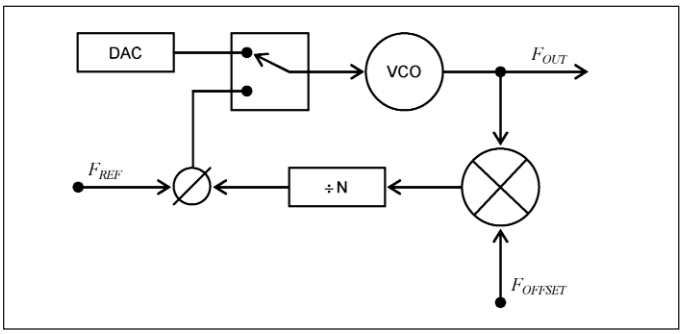

Figure 46 · Initial frequency acquisition.

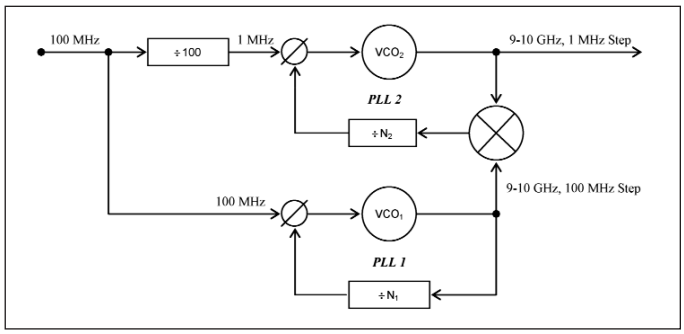

Figure 47 · Dual-loop synthesizer example.

able) VCO tuning characteristics over operating temperature range as well as precise frequency calibration to compensate the VCO temperature drift. Moreover, DACs are usually too noisy, adversely affecting the synthesizer phase noise performance if they are not properly removed after the initial frequency acquisition. Another potential problem is due to undesired mixer signals (e.g., LO leakage, intermodulation products), which can leak to the synthesizer output. Thus, a certain effort is required to provide required isolation between the mixer ports and the synthesizer output.

Multiloop Synthesizers

The main disadvantage of the simple frequency offset schemes is limited frequency coverage. Increasing the output frequency range for a fixed offset signal leads to a higher IF at the mixer output. This requires a divider with a larger division coefficient that defeats the idea of this method. The offset frequency signal should preferably be as close as possible to the VCO output frequency in order to keep the division ratio at minimum. Thus, a variable frequency offset signal is desired.

The variable offset signal can be generated with another PLL as depicted in Figure 47. What do we gain with this approach? Let's revise again our need for a 1 MHz-step synthesizer operating between 9 and 10 GHz. The first PLL provides 9 to 10 GHz frequency coverage with a 100 MHz step size by varying the division ratio N_1 between 90 and 100. The output of the first PLL is used as an offset signal for the second loop to keep the mixer output below 100 MHz. Thus, for the desired 1 MHz step size, the maximum division ratio for the second loop does not exceed 100 as well. The phase noise degradation for both loops (set by the maximum division ratio) does not exceed 40 dB versus 80 dB for the single-loop alternative. Therefore, splitting the design in two loops can potentially result in overall 40 dB phase noise improvement compared to the single-loop approach.

Greater phase noise improvement (or smaller step sizes) can be achieved using a larger number of PLLs as shown in Figure 48. The number of loops and frequency plan depend on particular synthesizer requirements (step size, phase noise, etc.). Since there are a number of choices for managing the individual loop characteristics, the frequency planning is not trivial; some scenarios are discussed in [10-22]. An original mathematical algorithm based on Diophantine equations is described in [47]. It worth mentioning, however, that in many cases the synthesizer architecture is also governed by available components and their cost. Thus, the designer's experience and intuition are probably the most important factors in the synthesizer development equation.

This series of articles will conclude next month reviewing advanced synthesizer solution. It will discuss how to remove the YIG oscillator still preserving good phase noise characteristics. Complex multiloop synthesizers, modulation

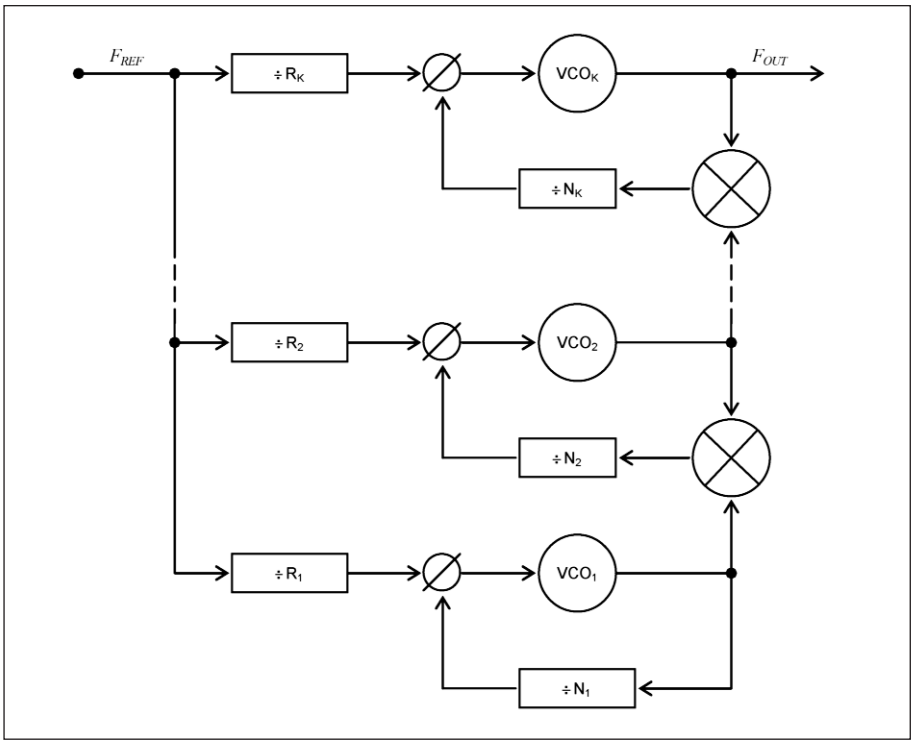

Figure 48 · Multiloop synthesizer concept.

options, various platforms and interfaces will be also discussed.

References

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