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Load Transient Response of a DC/DC Converter in GSM/ EDGE Handset Applications

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Understanding and specifying load transient response during the design of a handset is necessary to avoid errors in high data rate wireless transmission

The DC/DC converter in GSM/EDGE (Global System for Mobile communications/ Enhanced Data rates for GSM Evolution) applications must have the capability to handle both the high currents and non-constant envelopes of EDGE transmit bursts. This requirement leads to one of the key specifications of the DC/DC converter: *load transient response*. In this article, a system modeling technique and analysis flow are presented to derive load transient response requirements from top level system specifications. For this paper, the load transient response of a DC/DC converter has been studied with a large signal polar transmitter architecture, which is a widely adopted architecture for GSM/EDGE handsets in today's market.

Load Transient vs. Load Regulation

DC/DC converters have certain characteristics when responding to abrupt current or load changes. The output voltage of the DC/DC converter deviates from its desired nominal value when the load or current changes from one value to another. This phenomenon usually is characterized as load regulation, which is a traditional parameter to define the load response ability, or, how much the output voltage changes over a range of load current changes. The load regulation is measured by comparing the change in output voltage to the current change at the two loading extremes. One of the typical formulas for calculating load regulation in percentage is described in Equation 1:

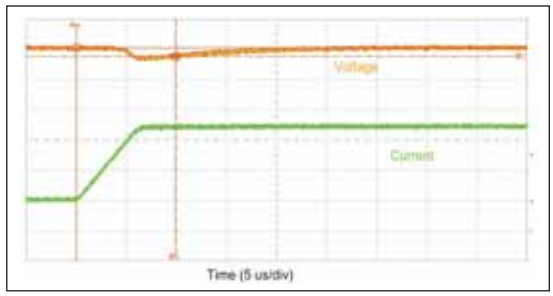

Figure 1 · Undershoot with current ramping up from 0 A to 1.5 A within 5 µs.

$$\frac{V_0(Full\ Load) - V_0(Min\ Load)}{I(Full\ Load) - I(Min\ Load)} * 100\% \qquad (1)$$

where $V_o(Full\ Load) - V_o(Min\ Load)$ is the output voltage variation, and $I(Full\ Load) - I(Min\ Load)$ is the current change from specified minimum load to maximum load.

Obviously, two measurements taken at maximum and minimum loads are static measurements. A key parameter, slew rate, which defines how fast the load current changes, is not taken into account in the load regulation. In general, with faster load current changes, there is more output voltage deviation. Usually, the voltage variations can be alleviated by using large capacitors at output of the DC/DC converter. However, those large capacitors will reduce the loop bandwidth, thus producing longer settling time, which is also a critical parameter defined by timing requirements from burst to burst in a GSM/EDGE system. The design trade-offs are often made by choosing proper values of the capacitors.

When the load current ramps up from a lower value to a higher value, the output volt-

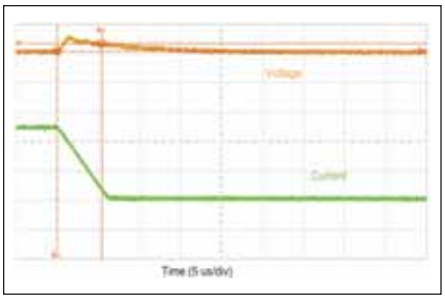

Figure 2 · Overshoot with current ramping down from 1.5 A to 0 A within 5 µs.

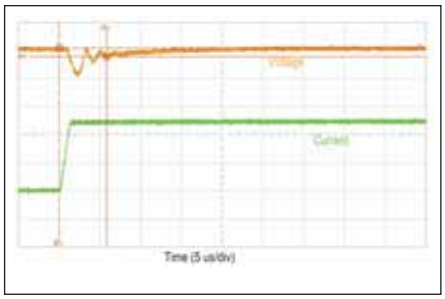

Figure 3 · Undershoot with second current ramping up from 0 A to 1.5 A within 1 µs.

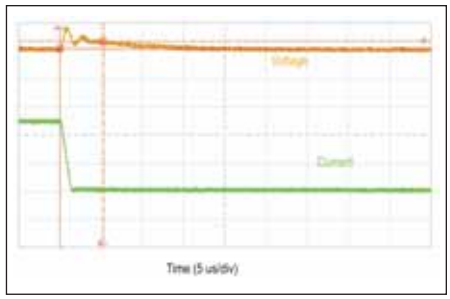

Figure 4 · Overshoot with current ramping down from 1.5 A to 0 A within 1 µs.

age of the DC/DC converter is pulled down and then back to nominal value, it is called voltage undershoot. Similarly, voltage overshoot occurs when current ramps down from a higher value to a lower value, the DC/DC output voltage rises up and then back to the nominal value. Combining undershoot and overshoot, the load transient response can be defined as the magnitudes of the overshoot and undershoot under load current variations.

Faster current changes cause higher load transients. Figures 1 and 2 show measurements of voltage undershoot and overshoot with ramping current up and down within 5 micro-seconds (µs), which is a typical current change rate in EDGE application. The data with faster current changes are shown in Figure 3 and Figure 4, where undershoot and overshoot is measured with current ramping within 1 microsecond. In Figures 1 to 4, all the current steps are from 0 Amp to 1.5 Amps (A). The orange lines are the voltage changes due to current ramping up or down, while the green lines are abrupt current changes.

Clearly the overshoots and undershoots with 1 µs period are significantly larger than ones with 5 µs period. Furthermore, if the currents are controlled by a waveform that continuously drives current up and down, the load transient will consist of a set of voltage overshoots and undershoots, which depend on both the magnitudes and slew rate of the load current changes.

Large Signal Polar Transmitter

The conceptual diagram of the large signal polar modulation is shown in Figure 5. Though the complexity of the large signal polar transmitter is beyond the scope of this article, it is still necessary to have a brief review of how the large signal polar transmitter works, especially when working with a DC/DC converter.

In the large signal polar modulation architecture, the transmitter separates the amplitude component out of the original signal, and only amplifies the remaining phase modulated signal. The signal magnitude of the phase path is intentionally designed to be large enough to drive the power amplifier (PA) into saturation so that the PA is operating in switching mode. The PA stage is then modulated with the amplitude component to recombine amplitude and phase information, restoring the modulation back to original form. The fundamental output RF power is actually proportional to the voltage applied at collector of the PA. By controlling the collector voltage, not only the output power can be controlled precisely but also the envelope of the output signal can be modified.

In Figure 5, several descriptive nodes are defined: V_{bat}, V_{ramp}, V_{cc}, V_{dc_out}, P_{in} and V_{rf_out}. V_{bat} is the connection point between battery module and the input of the DC/DC converter. V_{ramp} is the amplitude of the signal provided by RF transceiver and applied at the input of the PA controller. V_{cc} is the bias node of PA's collectors that actually controls output power delivered by the PA. V_{dc_out} and V_{rf_out} represent the output voltage of the DC/DC converter and RF output voltage of the PA, respectively.

The modulated amplitude signal, V_{ramp}, is applied at V_{cc} through a PA controller that could be simply a low dropout regulator (LDO). Depending on the closed loop gain of LDO, the PA controller accurately amplifies the

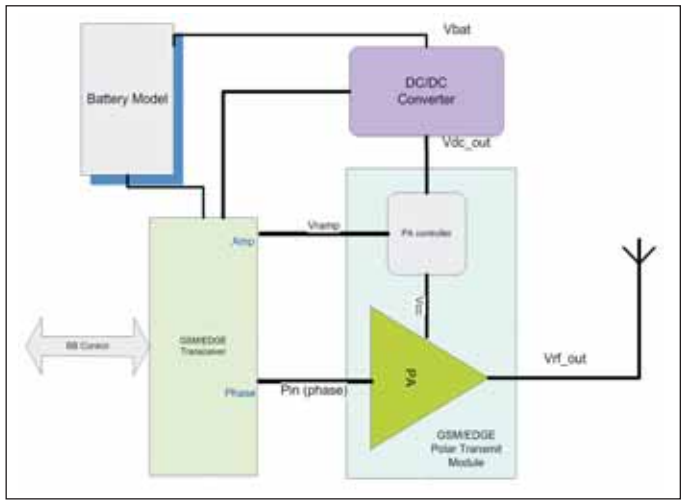

Figure 5 · Block diagram of a large signal polar transmitter with DC/DC converter.

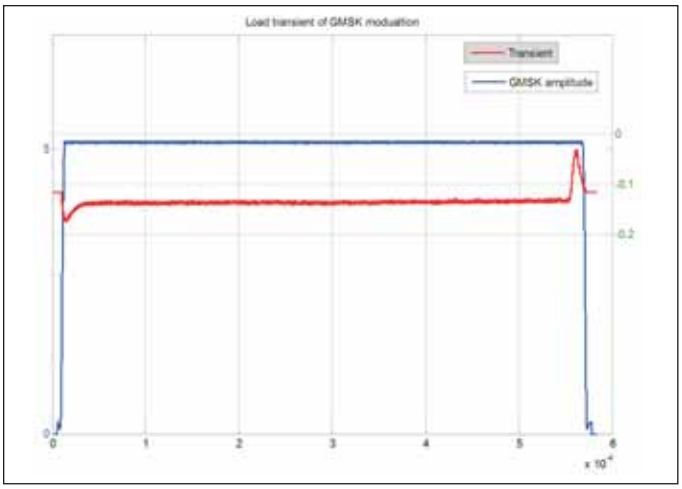

Figure 6 · GMSK amplitude and DC/DC output.

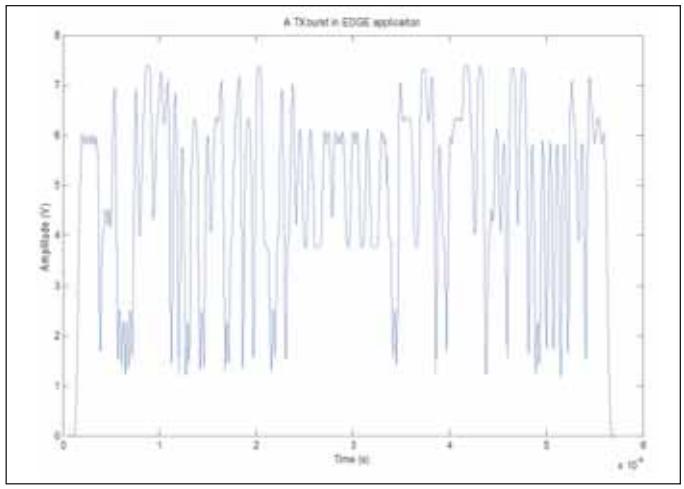

Figure 7 · EDGE envelope of one burst.

V_{ramp} signal, and rejects the noise and spurs coming from V_{ramp} and V_{cc} lines. The collector voltage V_{cc} is then modulated with V_{ramp}. Thus, the amplified signal with original modulation form, V_{rf_out}, can be fully reconstructed from the modulated collector voltage and the phase path waveform.

The DC/DC converter is inserted between battery module and the PA controller. The voltage at the output of the DC/DC converter is computed and set by the system to ensure both maximized efficiency and system performance under all circumstances.

Constant vs. Non-Constant Envelope

It is well known that GMSK (Gaussian Minimum Shift Keying) modulation has constant envelope so that there is no current change during a GMSK burst. The output voltage of the DC/DC converter is consequently constant without any voltage undershoots and overshoots. The GMSK amplitude waveform and the output voltage of the DC/DC converter during a GMSK burst are modeled and shown in Figure 6, where the blue line is the envelope of GMSK signal and the red line is the modeled load transient response.

However, Figure 6 does show that the undershoot and overshoot occur at the beginning and end of the burst. The reason is that current changes only when the burst ramps up and down. Since the load current of the DC/DC converter is constant, it will not affect system performance for GMSK modulation.

Unlike GMSK modulation, the 8PSK (8 Phase Shift Keying) modulation scheme used in EDGE results in a non-constant envelope of the signal, as shown in Figure 7. The large transitions form peaks to valleys that are more than 17 dB.

With these large and fast envelope variations, there is no doubt that many undershoots and overshoots occur during an EDGE burst. The time of transition from valley to peak is typically around 5 µs. Figure 8 illustrates how the amplitude signal invokes the load transient at output of the DC/DC converter.

The non-constant envelope V_{ramp} is actually same as V_{cc} except for a difference in gain factor set by the PA controller. The higher voltage is applied at V_{cc}, the higher current is drawn by the PA, and vice versa. Indeed, currents drawn by the PA are equal to currents pulling from the DC/DC converter, so that the currents of the DC/DC converter will vary with envelope of the signal. As discussed earlier, the output voltage of the DC/DC converter has overshoots and undershoots due to these current changes. Typically during an EDGE burst at maximum PCL with Class E2 in the GSM 850 MHz band, currents of the DC/DC converter might ramp up and down in a range from a few hundreds milliamps up to 2 amps.

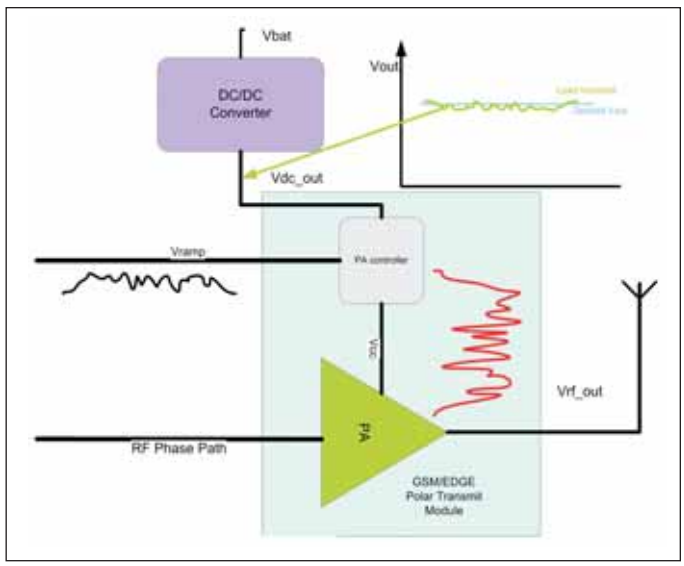

Figure 8 · Load transient formation.

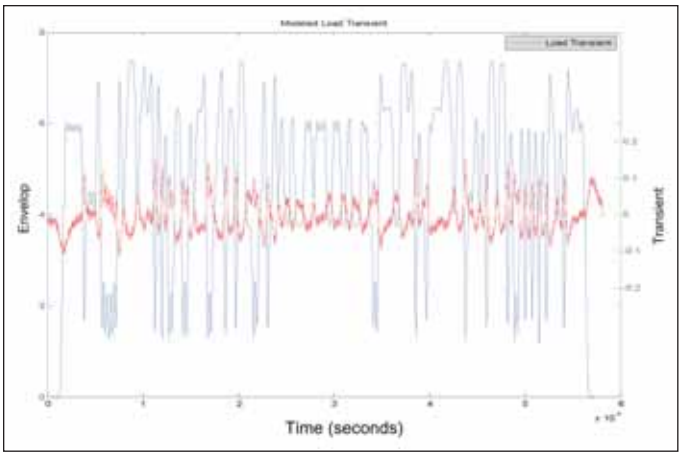

Figure 9 · Load transient during an EDGE burst.

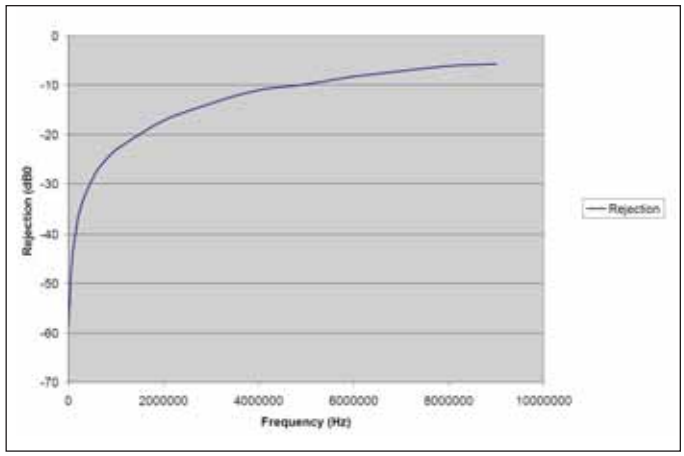

Figure 10 · PSRR of the PA controller.

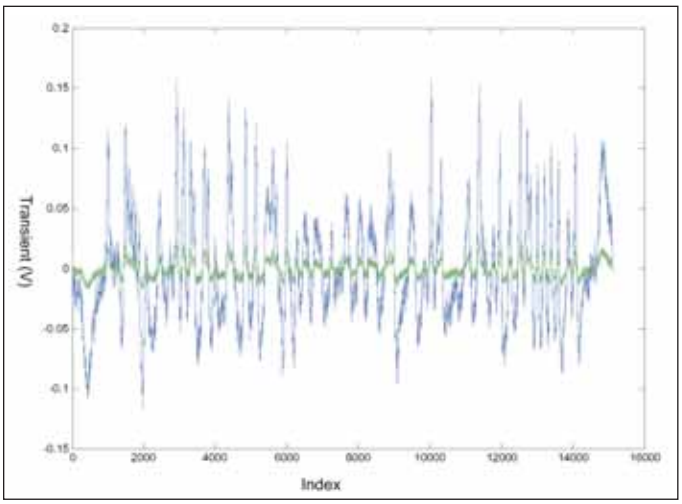

Figure 11 · Load transient before and after PA controller.

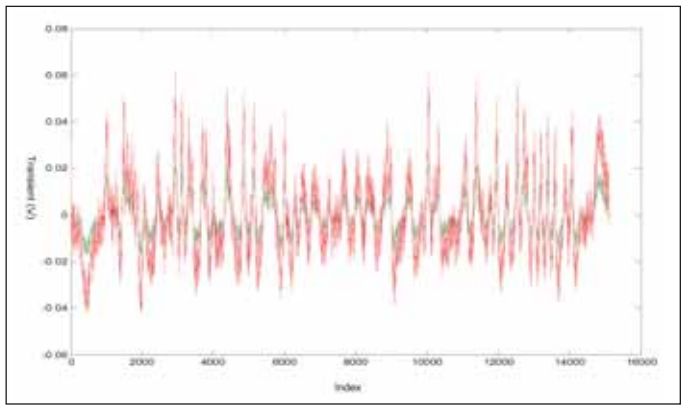

Figure 12 · Transient amplified by gain factor.

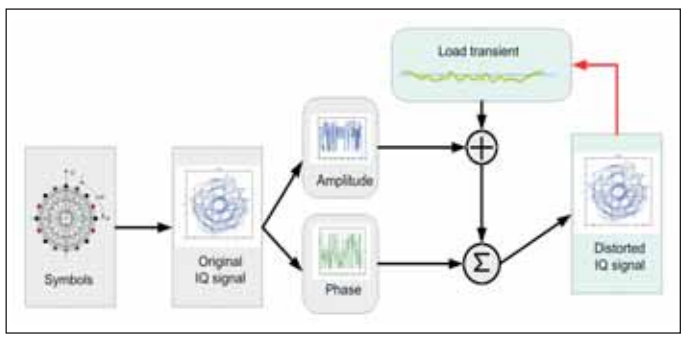

Figure 13 · System model.

Modeled Load Transient in EDGE

The modeled EDGE envelope and the load transient of the DC/DC converter output are both shown in Figure 9. The blue line is signal envelope, while the red line is the modeled load transient. The transient ripple will be superimposed on the top of the envelope or amplitude waveform at V_{cc}. At the output of the PA, the amplitude path will consist of an amplified original amplitude component and amplified load transient ripples, which cause distortions of the amplitude signal. The lower the magnitude of the load transient, the better system performance will be achieved.

PSRR of PA Controller

Though the load transient of DC/DC converter seems quite significant, a certain amount of load transient ripples will be rejected by the PA controller, which usually is designed with very good Power Supply Rejection Ratio (PSRR) up to certain frequency. Typically the PA controller has significant ripple rejection at low frequency but less at high frequency. An example of modeled PSRR of the PA controller is shown in Figure 10.

With finite PSRR, some load transient ripples still penetrate into V_{cc} and are eventually amplified by PA. The transient ripples which pass through the PA controller are simulated and shown in Figure 11. The blue

trace is the load transient at output of the DC/DC converter, and the green trace is the load transient that has passed through the PA controller. Figure 11 clearly shows that the magnitude of the transients is significantly reduced.

Gain Factor

From V_{cc} to V_{rf_out}, there is also a gain factor that needs to be taken into account in the model. The gain factor can be obtained by simulating or measuring AM/AM of the PA module and removing the PA controller gain from V_{ramp} to V_{cc}. Since the gain factor varies from part to part, a gain of 2.5 dB is assumed in this work. The red waveform in Figure 12 is the transient ripple amplified by the gain factor and then presented at V_{rf_out}, and the green line is the load transient ripple at V_{cc}. The load transient ripples finally show up at the output of the system (V_{rf_out}) and are used for further system simulation.

System Model

The system level model, shown in Figure 13, is designed to evaluate the degradation of the system performance due to the load transient. The original I/Q EDGE signal is created from symbols and conditioned close to practical system performance, which is very well specified in 3GPP standards. The amplitude and phase components are extracted from the original I/Q EDGE signal. The load transient model of the DC/DC converter is connected to the amplitude path only. The distorted signal is then reconstructed by combining the amplitude, transient and the phase waveforms.

The spectrum of the load transient at system output is computed and shown in Figure 14. The spectrum up to 800 kHz is significant and need to be considered. In fact the spectrums at 400 kHz and 600 kHz are more sensitive and usually have lower system margin so they need to be carefully budgeted.

Modulated spectrum, switching spectrum and EVM are simulated for evaluating system performance in the model. Based on system performance, the budgets of load transient of the DC/DC converter can be optimized.

Simulation Results

The system level simulations have been done by sweeping the magnitude of the load transient. The EVM results are shown in Figure 15 and little degradations on EVM have been observed. Therefore the load transient impacts should be focused on spectrum performance.

Modulated spectrum at 400 kHz and 600 kHz offsets are simulated and shown in Figure 16. To keep the spectrum degradation below 1 dB at

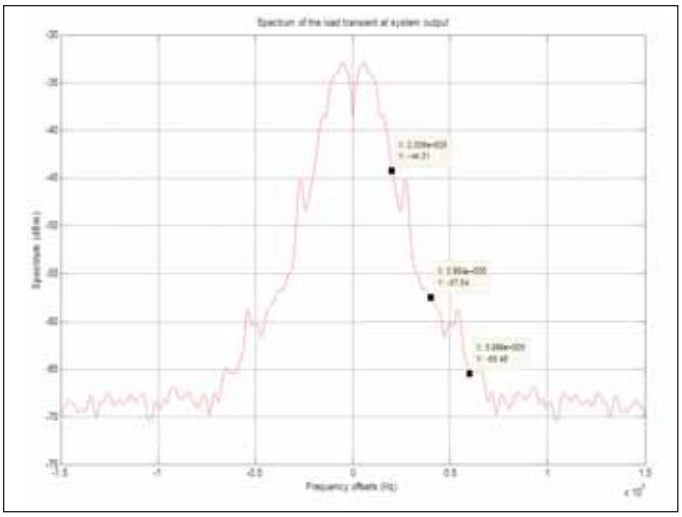

Figure 14 · Spectrum of load transient.

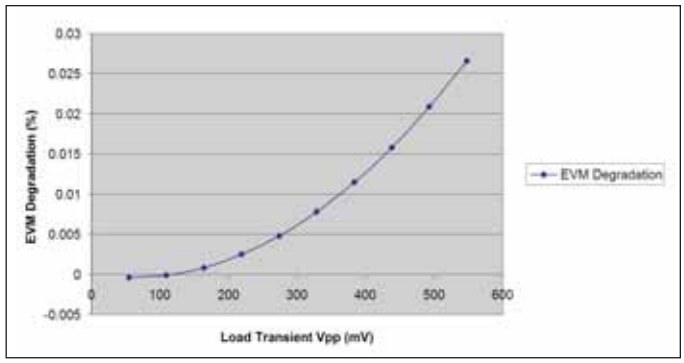

Figure 15 · EVM vs. load transient.

400 kHz, and 0.8 dB at 600 kHz, the load transient ripples shall be smaller than 495 mV peak to peak.

For switching spectrum, simulation results of 400 kHz and 600 kHz offsets are simulated and illustrated in Figure 17. In order to have degradation less than 1 dB, the transient shall be smaller than 250 mV_{pp}.

The allocated budget of load transient varies from system to system, which has different implementations. One system may have greater margin on the modulated spectrum, while the others may have more margin on the switching spectrum. Assuming the system has fewer margins on the switching spectrum, the load transient ripples being less than 250 mV_{pp} might be acceptable. Note that other distortion factors, such as input noise and output noise of the DC/DC converter, also need to be considered for overall budgets.

Summary

The methodology for the allocation of a budget for load transient response of a DC/DC converter in a GSM/EDGE handset is presented in this paper. Though the work has been done with a large signal polar transmitter, it can definitely be applied with a linear transmitter as well. The simulation results show that it is critical to have the load transient ripples optimized so that it has minimum impact on system performance.

Acknowledgement

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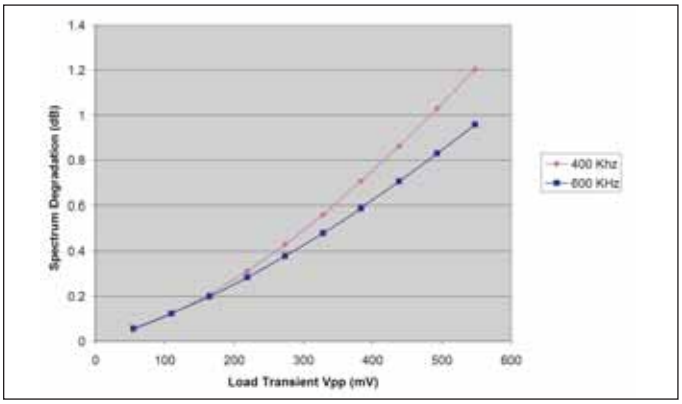

Figure 16 · Degradation of modulated spectrum due to load transient.

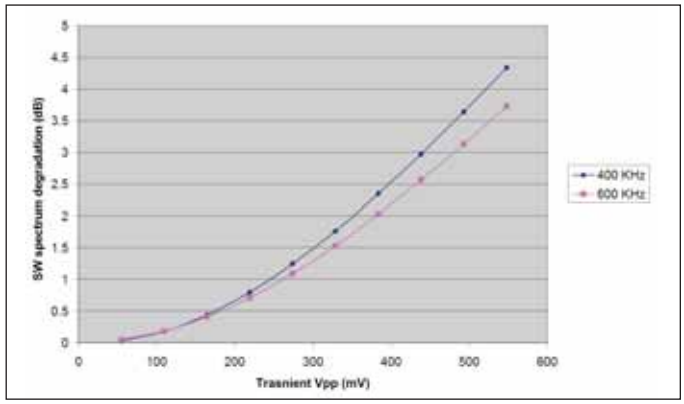

Figure 17 · Degradation of switching spectrum due to load transient.