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Characterization of RF Transmission Lines on Ion-Implanted CMOS Wafers

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This article reports on experiments with transmission lines on silicon that has been modified to improve its dielectric properties

In spite of rapid technology evolution for the use of silicon in RF applications, the main technology challenge to realize high RF performance in silicon to overcome the high substrate losses and cross-talk associated with the CMOS grade silicon. Further, technology advancement demands on-chip integration of transformers, baluns, filters, and the co-integration of digital and RF systems on a single silicon chip. But this is hampered due to low-resistivity of CMOS grade Si (typically 3-5 Ω-cm) wafer, resulting in substantial energy losses and dielectric attenuation. [1]

One of the most common solutions is to utilize VLSI back-end dielectric layers on top of Si wafer to reduce lossy effects. However, large losses from Si substrate are still unavoidable because of limited oxide thickness provided by current VLSI technology. The stack of oxide-nitride-oxide has been reported by Ng et al [2] as having good linearity, absence of dispersion behavior and low leakage. Still, this technique has the limitation of an interfacial layer thickness constraint and cannot be used at higher frequencies. Other options employed are the thicker polyimide or selective removal of the underlying substrate, but this increases complexity due to process intensive steps, along with the risk of contamination of the foundry machinery. Even the use of SOI (silicon-on-insulator) shows little improvement in substrate losses and cross-talk because thicker isolation is required for RF performance improvement. This article details a simple CMOS grade compatible process to develop high-resistivity wafers using ion-implantation with a low energy dose. The process reported in the literature utilizes proton and arsenic implantation at an energy dose in MeV range [3-6].

In this article, the novel concept of poly-silicon deposition over oxide has been implemented. This technique, along with controlled dose of implantation, gives high resistivity at low energy levels (KeV range). The proton implantation has little effect on oxide integrity that can be integrated into VLSI back-end processes. Further, 50 ohm transmission lines have been fabricated both on an ion-implanted silicon wafer and standard alumina substrate. The performance of the ion-implanted wafer has shown to be at par with the standard substrate, thus paving the way for RF-CMOS integration.

Resistivity Effects on Transmission Lines

Transmission lines are of great importance in any RF design and their performance represents one of the key issues in RF-CMOS integration, especially for higher operating frequencies. Two types of modes generally propagate on silicon substrate, known as *slow wave* and *quasi-TEM mode*, corresponding to lossy silicon substrate and lossless (dielectric) silicon substrate. The substrate losses depend on frequency and surface resistivity [7]. At higher frequencies, the dielectric behavior of the silicon substrate cannot be neglected at frequencies approaching or exceeding the dielectric relaxation (cut-off) frequency f_c defined as

$$f_C = \frac{1}{2\pi R_{si} C_{si}} = \frac{1}{2\pi \rho_{si} \varepsilon_{si}}$$

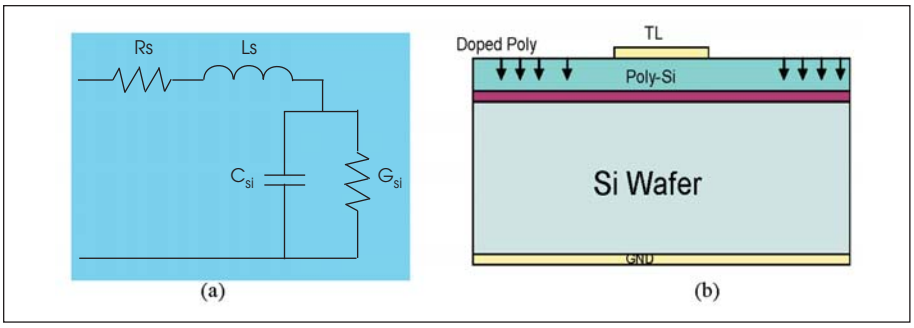

Figure 1 · Transmission line. (a) Lumped physical model; (b) Cross-section view of line on the silicon wafer.

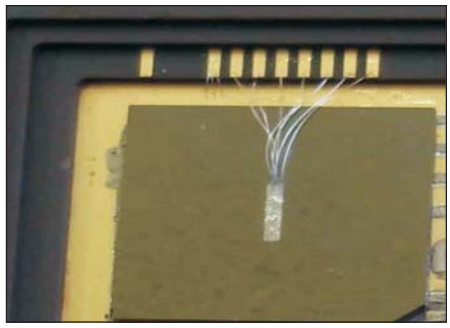

Figure 2 · Fabricated transmission line on ion-implanted wafer

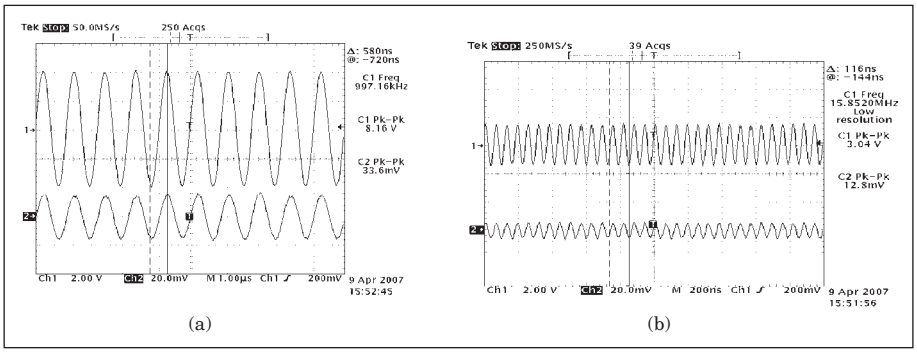

Figure 3 · Measured output performance with sinusoidal wave. (a) 1 MHz; (b) 16 MHz.

where R_{si} and C_{si} are the resistance and capacitance of the substrate and ρ_{si} and ε_{si} are the resistivity and permittivity of the substrate respectively. This relation shows the effect of resistivity on the cut off frequency. The equivalent lumped physical model can be represented as shown in Figure 1.

The substrate losses represented by G_{si} and metallization losses can be represented as R_{si} as shown above. For low and medium resistivity (ρ < 60 ohm-cm), the losses are mainly due to shunt conductance, G_{si}. At high resistivity, substrate behaves purely as capacitive and contribution of G_{si} is negligible so it exhibits lowest losses.

Concept of Ion Implantation

The concept of high resistivity is shown as a cross section view in Figure 1(b). This technique makes a high resistivity wafer compatible with the CMOS process. The oxide is deposited on the silicon wafer to increase substrate isolation over which ion implantation of poly-silicon has been carried out. This technique has been used for RF applications and in authors view still not reported elsewhere. The resistivity of heavily doped poly-Si is about ten times higher than that of diffusion doped poly-Si [Ref. 9, pp. 181-182]. A subsequent annealing step redistributes and activates the implanted dopant.

The Experiment

A standard 6-in Si wafer of 675 µm height, with resistivity of 3-5 Ω-cm is used in this study. Further oxidation of 250 Å followed by poly deposition of 5000 Å has been done. Ion-implantation of the proton (dose of $8.0e^{15}$ cm^{-3}) at 75 KeV has been carried out. The wafer is then annealed

at 1000°C to redistribute the implanted dopants. The metallization of aluminum is carried out using E-beam and patterned using lift-off to have transmission line of dimension 0.5×2.7 mm. Backside metallization is carried out as required for microstrip configuration. The complete topology is shown in Figure 2. Standard MIC fabrication of 50-ohm line is also carried out on alumina (25 mils) substrate having width of 0.25 mm. The measurement of resistivity is carried out using I-V measurement. The AC characterization has been carried out using function generator (Tektronix, AFG 310) and output is measured using oscilloscope (Tektronix, T5540D).

The structure is mounted in the standard COB package with leads thermo-bonded to the output terminals. Multiple leads have been bonded to minimize interconnection inductance.

Results and Discussions

The resistivity of proton-implanted Si comes out around 24 kΩ which is much higher than the standard CMOS grade silicon wafer value of ~300Ω. The performance of the transmission line on ion-implanted Si wafer has been compared with the transmission line fabricated on the standard alumina substrate. Both sinusoidal as well as square wave has been given at different frequencies ranging from 1 MHz to 16 MHz. Figure 3 shows the measured performance of the standard alumina substrate at two different frequencies. The output voltage comes out in the range of 50 mV. It has been observed that square wave got distorted after 8 MHz due to the inherent property of the dielectric (Figure 4).

The same experiment has been carried out using ion-implanted wafer (Figures 5 and 6). The output voltage comes out around in the range of 100 mV and same phenomena have been observed with the square wave.

This result shows good agreement with the standard alumina dielectric, indicating the high resistivity achieved in the Si process. The high resistivity after ion-implantation may be due to implantation-created high defect densities that effectively trap free carriers. The trend of the output voltage variation also shows creation of high resistivity on the wafer.

Conclusion

Simple ion-implantation methodology has been demonstrated for RF circuits applications using a standard CMOS foundry process. The comparison with the standard alumina substrate has also been made. The results show the effectiveness of the desired process topology for changing the resistivity. The process enables easier integration into current technology paving way for RF-CMOS to become a reality on a single chip. It is hoped that this development will lead to practical high integrity and low cost topologies.

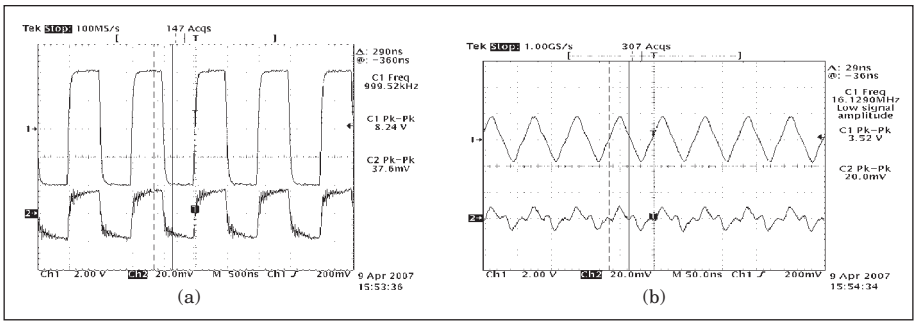

Figure 4 · Measured output performance on alumina substrate with square wave. (a) 1 MHz; (b) 16 MHz.

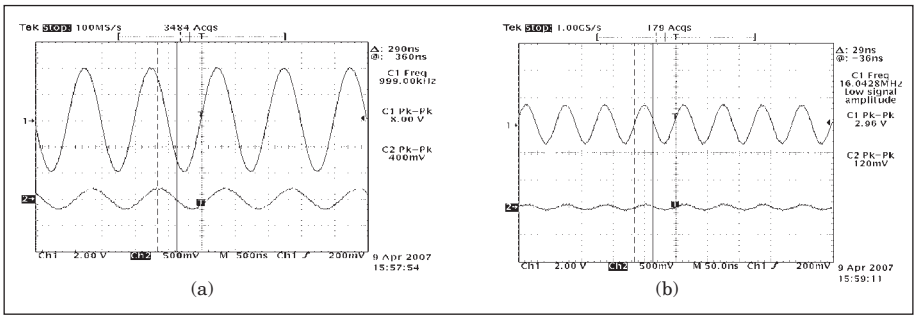

Figure 5 · Measured output performance on ion-implanted wafer with sinusoidal wave. (a) 1 MHz; (b) 16 MHz.

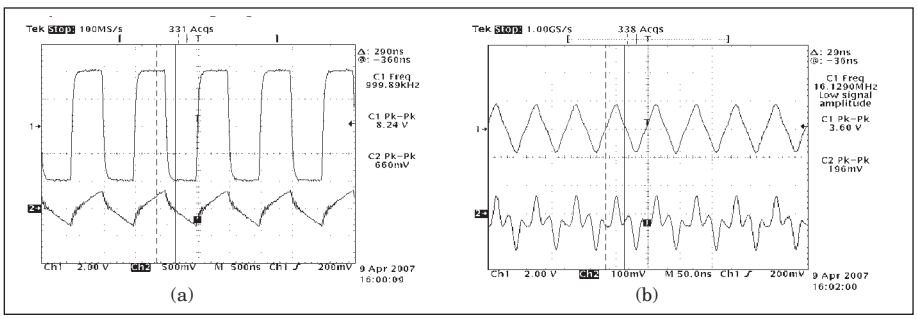

Figure 6 · Measured output performance on ion-implanted wafer with square wave. (a) 1 MHz; (b) 16 MHz.

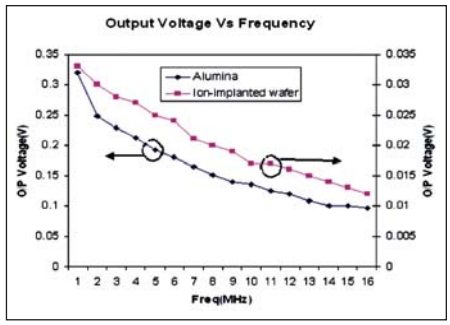

Figure 7 · Comparison of the output voltage with frequency.

References

1. Claus Schollhorn,Weimei Zhao et al, "Attenuation Mechanism of aluminum millimeter-wave coplanar waveguides on silicon," *IEEE Trans. On Electron Devices,* Vol. 50., No. 3, pp 740-746, March 2003.

2. C.H. Ng, K.W. Chew, and S.F. Chu, "Characterization and comparison of PECVD silicon nitride and silicon Oxynitride dielectric for MIM capacitors," *IEEE Electron Device Letters,* Vol. 24, No. 8, pp. 506-508, August 2003.

3. R. Yuang Yang, Cheng-Yuan Hung, et al., "Loss characteristics of silicon substrate with different resistivities," *Microwave and Optical Technology Letters,* Vol. 48, No. 9, pp. 1773-1776, Sept. 2006.

4. Y.H. Wu, Albert Chin et al., "Fabrication of Very High Resistivity Si with Low-loss and Cross-talk," *IEEE Electron Device Letters,* Vol. 21, No. 9, pp. 394-396, Sept. 2000.

5. K.T. Chan, C.Y. Chen et al., "40 GHz Coplanar Waveguide Band pass Filters on Silicon substrate," *IEEE Microwave and Wireless Components Letters,* Vol. 12, No. 11, pp. 429-431, Nov. 2002.

6. K.T. Chan, Albert Chin et al., "Low RF noise and power loss for Ion-implanted Si having an improved Implantation process," *IEEE Electron Device Letters,* Vol. 24, No. 1, pp. 28-30, Jan. 2003.

7. Yong-Zhong Xiong et al., "Substrate effects on Resonant Frequency of Silicon-Based RF on-chip MIM capacitor," *IEEE Transactions on Electrons Devices,* Vol. 53, No. 11, pp. 2839-2845, Nov. 2006

8. G. Cellere, M.G. Valentini et al., "Different Nature of Process -Induced and stress-induced defects on thin SiO_2 Layers," *IEEE Electron Device Letters,* Vol. 24, No. 6, pp. 393-395, June 2003.

9. Stanley Wolf and Richard N. Tauber, *Silicon Processing for The VLSI Era*. Lattice Press, Sunset Beach, California, 1986.

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