How Match Affects Power Measurements

Designing Power Amplifiers Using Maximum-Efficiency Lines and Constant Power Contours

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How Does Match Affect My Power Measurement?

By Orwill Hawkins

When power sensors are designed, attempts are made to produce the lowest VSWR (SWR) so that the user will have the best match when using it. However, match is never perfect because no device, including any power sensor, has a perfect SWR. For this reason, two power sensors of equal quality and calibration will read differently in a user’s system. In this brief, we’ll take a look at the reasons for this along with ways to achieve the best power measurements.

As a result of manufacturing limits, part and component variations, line lengths and detector properties, the VSWR of any power sensor is not perfect and varies dramatically over frequency. Two high quality, high performance power sensors will exhibit different VSWR characteristics at different frequencies. Figure 1, a chart from a LadyBug LB5940A Power Sensor data sheet, shows the specifications and typical data for a production run of power sensors. In the data sheet, the company also provides a table with limit (red line in Figure 1) and typical data for several frequency ranges to make uncertainty calculations easier for users. It is also apparent that as the frequency increases, VSWR increases making it very important to understand match when working with higher frequencies.

When comparing first-quality power sensors, you might notice that each one could exhibit a better VSWR than the other at some frequencies, even though in total they are similar. For example, at 1 GHz, the LadyBug LB5918A sensor has a limit specification of 1.13, while the Keysight™ U2000 is 1.15; at 15 GHz, both limit specifications are identical. Each one will have a frequency where it has a slightly better match. You can expect an accurate measurement from either of these sensors; however, you can be sure that the actual VSWR of each sensor will not be the same. The different VSWR results in different sensor-to-DUT mismatch and slightly different power readings. Further, when phase is considered, power reading variations can exceed 0.1 to 0.2 dB. This sometimes leads to confusion. Next, we will look at it in more detail.
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2: Feature Article
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10: Feature Article
Designing Power Amplifiers Using Maximum-Efficiency Lines and Constant Power Contours
By Ivan Boshnakov, Teledyne Defence & Space, Pieter Abrie, Ampsa Inc.; and Malcolm Edwards, AWR Group, NI.

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Max RF Power 20˚C at Sea Level

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IMS2019 General Chairs’ Welcome

Boston and the local steering committee are pleased to welcome the microwave world to the 2019 International Microwave Week, featuring the Radio Frequency Integrated Circuit (RFIC) Symposium, the International Microwave Symposium (IMS), the 5G Summit, and the ARFTG Microwave Measurements Conference. The technical presentations and industry exhibits will be held at the Boston Convention and Exhibition Center (BCEC). The social and networking events and opportunities will take place throughout the revitalized Seaport District, home to many museums, shops, restaurants, and nightclubs.

Boston has a rich microwave heritage that continues through today. The Radiation Laboratory run by the Massachusetts Institute of Technology (MIT) during the 1940s made seminal contributions to the emerging microwave engineering field. Much of this knowledge was transferred to surrounding industry and universities in the 1950s. More recently, the local steering committee takes pride in balancing the traditions of the IMS with innovative twists to create a great experience for the technical and industry exhibition attendees. This year’s symposium continues this philosophy with new features that include:

A **significantly enhanced mobile app** with the goal of making this the primary interface to the International Microwave Week.

**Focus on start-ups and young professionals** through the introduction of a Start-up Pavilion in the Industry Exhibition along with an IP 101 information session, start-up panel session, and Next Top Start-up contest. Young professionals will have a lounge specifically to meet and exchange ideas and experiences and a reception at Coppersmith on Tuesday evening.

**Sixty Second Presentations** where interactive forum authors can pre-record an overview of their papers, allowing attendees to get a preview of the paper’s content and target the papers of most interest to their work.

**Interactive Panel Sessions** with real-time audience participation via the Slido App

**Sweet Treats Tuesday** to welcome the attendees to the industry exhibit. Dessert items will be provided during the lunch break, encouraging everyone to come to the exhibit floor for a treat and begin interactions with the industry exhibitors.

The overall format of the International Microwave Week remains the same. The RFIC Symposium begins on Sunday with workshops and concludes Tuesday morning. The 5G Summit, again co-sponsored by MTT-S and ComSoc, picks up on Tuesday afternoon and concludes Tuesday evening with a panel session. The IMS will run Sunday through Friday with the Industry Exhibition taking place Tuesday through Thursday. The ARFTG
Microwave Measurements Conference will also begin on Sunday with jointly sponsored workshops on Sunday and Monday, and the technical sessions on Thursday and Friday. In all, there will be over 9,000 attendees from around the world participating in the technical sessions, workshops, and the Industry Exhibition. There will be more than 900 exhibitor booths showcasing the latest developments in microwave hardware, software, components, and systems.

The International Microwave Symposium will begin with workshops and short courses on Sunday and Monday. The opening plenary session will be held Monday evening featuring a presentation on “The Mind-Body Problem for Intelligent RF,” by Dr. William Chappell, the Director of the Microsystems Technology Office at the Defense Advanced Research Projects Agency (DARPA). This will be followed by the Welcome Reception at the Seaport World Trade Center. The IMS technical sessions will run Tuesday through Thursday, with the closing session on Thursday afternoon featuring Dr. Dina Katabi from MIT describing her work at the intersection of wireless microwave systems and machine learning focused on biological applications. The closing celebration reception will be held immediately after. The symposium will conclude with additional workshops held on Friday.

The Industry Exhibition is another center piece of the International Microwave Week and will take place on Tuesday through Thursday. In addition to the Sweet Treats Tuesday, the Industry-hosted reception will be held Wednesday late afternoon. The exhibition floor will be home to the MicroApps Theater, the Societies’ Pavilion, and the new Start-up Pavilion. The IMS schedule again will include exhibition-only time on Wednesday afternoon to ensure all attendees have an opportunity to interact with and learn about the latest products from the microwave industry exhibitors.

The evenings throughout the week will be filled with social and networking opportunities, both organized and informal, so that you can catch-up with your colleagues from across the globe. The RFIC and IMS Plenary Sessions and Welcome Receptions will be held on their respective Sunday and Monday evenings. Tuesday evening will have the young professionals’ social event and the amateur radio social. Wednesday evening will have the Women in Microwaves Reception and the Awards Banquet.

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Consider a microwave source set to 1.00 dBm, connected to a power sensor. If the calibration and match of the source and sensor were perfect, you would set and read 1.00 dBm. In reality, sources are calibrated with a 50 ohm load, however the actual output impedance is not 50 ohms. This is due to the source’s broad driver requirements, driver technology limitations, and part variations. In fact the VSWR is probably very different than 50 ohms, resulting in a high VSWR. A review of the published VSWR specifications for 4 different current model, top-brand sources was 1.5, 1.6, 1.9 and 1.6 at 3 GHz.

Even though a power sensor’s typical VSWR is much lower than that of a source, the significant source reflection can result in an error that should be accounted for. This error is a result of a small portion of the power being reflected back from the sensor to the source, a portion of which is then re-reflected by the source and combined into the measurement (See Figure 2). In addition to the amplitude, it is important to understand how the reflections’ phase can affect your measurement. If the reflected portion is in phase with the incident power, the measurement will be increased; if the reflected portion is 180 degrees out of phase, the measurement will be reduced; there will be frequencies at which the phase is just right and a perfect result will be produced. The reflection repeats, becoming smaller each time. The total mismatch determines the magnitude of reflected power. In this case it is nice to think of reflection coefficient rather than VSWR, even though they are functionally equivalent. The source could be any device generating power for measurement and it is important to know its VSWR.

To calculate the potential error, you must know the reflection coefficient (ρ) of the sensor and the source (DUT - device under test). The sensor’s ρ can easily be calculated from its specifications. All calculations are done with linear data. We’ll calculate here based on a VSWR of 1.10 to keep things simple. For this example, we will consider these to be limit specifications (worst case numbers).

\[ ρ_{\text{sens}} = \frac{(\text{VSWR}-1)}{(\text{VSWR}+1)} \]
\[ ρ_{\text{sens}} = \frac{(1.10-1)}{(1.10+1)} = 0.048 = 4.8\% \]

This worst case number indicates that 4.8% of the power could be reflected back. During calibration, match is mitigated in the applied power system so that the sensor can be calibrated correctly. All power is measured, including that which was reflected back.

Now let’s do the same for a source. Here we will use 1.3 VSWR which is something that we might expect to see.

\[ ρ_{\text{DUT}} = \frac{(\text{VSWR}-1)}{(\text{VSWR}+1)} \]
\[ ρ_{\text{DUT}} = \frac{(1.3-1)}{(1.3+1)} = 0.1304 = 1.304\% \]

If the above described source and sensor are directly connected there will be interaction due to the reflected power. Let’s calculate the mismatch interaction and total potential error due to mismatch using the formula:

\[ M_m = \left(1 + (ρ_{\text{sens}} \cdot ρ_{\text{DUT}})^2\right) - 1 \]
\[ M_m = \left(1 + (0.048 \cdot 0.1304)^2\right) - 1 = 0.0126 = 1.26\% \]

The potential error in measurement due to mismatch is 1.26%. Since limit values (worst case specifications) were used, the error would be something less than this. If we had located and used typical numbers, we would have had a smaller number that was probably more accurate instead of this worst case result.

If we now consider a different power sensor which has a similar but not exact VSWR we will see slightly different results even if the calibrations are both perfect. This second sensor has a VSWR of 1.11, just slightly different than the first.

\[ ρ_{\text{sens}} = \frac{(\text{VSWR}-1)}{(\text{VSWR}+1)} \]
\[ ρ_{\text{sens}} = \frac{(1.11-1)}{(1.11+1)} = 0.052 = 5.2\% \]

The worst case number for the second sensor shows that 5.2% of the power could be reflected back from the sensor.

Since there is no change in the source, we can use \( ρ_{\text{DUT}} \) of 0.1304 and calculate the combined result as:

\[ M_m = \left(1 + (ρ_{\text{sens}} \cdot ρ_{\text{DUT}})^2\right) - 1 \]
\[ M_m = \left(1 + (0.052 \cdot 0.1304)^2\right) - 1 = 0.0136 = 1.36\% \]

The potential error in this measurement due to mismatch is 1.36%, very close to the former 1.26%. However you cannot expect both sensors to measure exactly the same even though both are good measurements.

As can be seen, even if you have the very highest level of calibration, match can cause significant measurement uncertainty. Mismatch is generally considered the most significant part of total measurement uncertainty.

In cases where high source mismatch is present, uncertainty can be reduced by adding an attenuator to the system. If, for example, a 3 dB attenuator is inserted between the source and sensor, the returned power from the sensor to the DUT is reduced, then the resultant reflection back from the DUT is again reduced, minimizing the error. Additional reflections are added on each
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US patents #9,793,904 B1, #9,734,099 B1
Designing Power Amplifiers Using Maximum-Efficiency Lines and Constant Power Contours

By Ivan Boshnakov, Teledyne Defence & Space, Pieter Abrie, Ampsa Inc.; and Malcolm Edwards, AWR Group, NI.

Introduction

This article presents an effective design approach for high-power and high-efficiency RF and microwave power amplifiers (PAs) based on a novel design method using the concept of maximum-efficiency lines, combined with control of the harmonic load impedances.

The concept springs from first examining two previously reported design methods in which compact nonlinear transistor models were used to perform simulated load pull for the fundamental, second, and third harmonics. This evolves into investigating load-pull results when the harmonics impedances at the intrinsic generator of the transistor model are pre-defined and from there to the concept of maximum-efficiency lines and how to define them using nonlinear simulated load pull.

The Cripps method, extended by Abrie’s “power parameters,” which provides the load-pull power contours and the maximum efficiency lines, is also discussed.

Designing Exclusively From Load-Pull Data

The initial compact nonlinear model used in [1] did not have the intrinsic channel model exposed. Therefore, the intrinsic voltages and currents could not be observed directly. Without this capability it was impossible to establish the fundamental-frequency and harmonic impedances required for the power and efficiency targeted over the bandwidth of interest in a straightforward manner [3, 4, 5, 6]. Load-pull simulations were therefore required in order to obtain the optimum load impedances (at the available device model’s reference plane) at a number of passband frequencies.

The selected target areas in Figure 1 were used to synthesize the output matching network. The input matching network was designed to match the input impedance of the transistor as calculated by using the S-parameters of the transistor with the load network in place.

The matching circuit synthesis was performed using a real-frequency synthesis technique to synthesize matching networks to solve the fundamental-frequency, second, and third-harmonic problems defined [9].

Figure 2 compares the simulated performance and the measured performance of the designed amplifier. The simulated and measured performances are in good agreement.

Model With Intrinsic Current Generator

A different design approach was presented in [2] to design a 1.8 – 2-GHz amplifier stage. The nonlinear transistor model developed by Modelithics for the 30 W T2G6003028-FL Qorvo gallium nitride (GaN) high-electron-mobility transistor (HEMT) was used to demonstrate this...
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new approach. Unlike the model used in the first design approach, this model enables access to the intrinsic device-channel voltage and current, crucial in this second design methodology.

Figure 3 shows the internal schematic of the nonlinear transistor model. The voltages and currents are measured across the intrinsic current generator and the impedance can be calculated and is plotted in the graph on the right. The output tuner of the load-pull setup controls the fundamental-frequency terminations along with the second- and third-harmonic terminations.

The second- and third-harmonic load reflection coefficients are pre-tuned for the selected class of operation (Class F in this case), before performing the fundamental-frequency load-pull simulations using Microwave Office circuit simulation software. A near short for the second harmonic and near open for the third harmonic are required for Class-F operation.

The fundamental-frequency reflection coefficient at the output was tuned for maximum power, Figure 3. The input tuner is used to achieve maximum gain at the fundamental frequency. The harmonics impedances at the input were set to 50 ohms in this design.

With the second- and third-harmonic load impedances pre-set for Class-F operation, the fundamental-frequency contours for maximum power and maximum efficiency were generated, as shown in Figure 4 (left graph). These contours were used to define a circular target area (green circle) for the fundamental-frequency load terminations.

The fundamental-frequency termination was set at the center of the circle targeted and load-pull contours (constant power and constant efficiency) for the second and third harmonics were then generated. The second-harmonic contours were generated with the third-har-
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monic impedance fixed to an open circuit, while the second-harmonic impedance was fixed to be a short circuit when the third-harmonic contours were generated. Useful areas of the Smith chart were then selected for the two harmonics. The second-harmonic load-pull contours are shown to the right in Figure 4.

The matching networks were synthesized as before [2]. The manufactured amplifier (1.8 - 2.2 GHz) with
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measured results is shown in Figure 5, indicating good agreement to simulation. The matching networks were synthesized as before [2]. The manufactured amplifier (1.8 - 2.2 GHz) with measured results is shown in Figure 5, indicating good agreement to simulation.

**Load Pull With Pre-Defined Harmonic Impedances**

Based on these results, load-pull analysis with pre-defined harmonic impedances was explored further. The first design method using the Wolfspeed 25-W GaN CGH40025F was used again for this investigation. Figure 6 shows a schematic with a load tuner and a new nonlinear model for the transistor, which provides the ability to measure the voltages and currents across the intrinsic generator. Load-pull simulations were performed with the harmonic impedances (reactances) pre-tuned for Class-B, Class-F, and inverse Class-F operation.

Figure 7 shows the 2.5-GHz power contours obtained at 5-dB gain compression. The maximum output power at the same compression depth are similar for the three classes of operation (44.7 dBm, 45 dBm, 45.3 dBm). The differences in the efficiency are significant (57.7%, 67.7%, 75.2%). The efficiency is the lowest for Class-B and the highest for inverse Class-F. The intrinsic fundamental-frequency impedance terminations for maximum power for each class are close to the values predicted by the theoretical expressions for the pre-hard-clipped situation where the RF current and voltage just touch the limiting boundaries of the I/V-curves (knee voltage, maximum current and breakdown voltage) [3, 4, 5].

The drain efficiency load-pull contours for the three classes of operation were also generated, Figure 8. The efficiency is again increasing from Class-B to Class-F to inverse Class-F. In the graph on the right, power and efficiency contours are superimposed.

Figure 8: Drain efficiency contours for class-B, class-F and inverse class-F operation (left) and superimposed output power and drain efficiency contours are shown.

**Impact of Harmonic Terminations**

Figure 8 shows a wide area where acceptable tradeoffs between power and efficiency could be achieved, but the area is strongly dependent on the harmonic impedances.

Two additional power contours are shown in Figure 9. The associated second-harmonic and third-harmonic reflection coefficients were intentionally de-tuned to -90° (green trace) and +90° (pink trace), thereby stretching the useful area further.

The peak-power point for Class-B is close to one of the contours added. Comparing the performance with the
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same fundamental-frequency termination, but different harmonic terminations, shows the power and efficiency for Class-B operation is 44.7 dBm and 57.7% and degraded to 44.2 dBm and 49% if the harmonics are de-tuned to 90°. This extreme case illustrates that the performance can degrade substantially if the harmonic impedances are off-target.

3D Load-Pull Simulations

The importance of the effect of the harmonics terminations is illustrated well in [3] and the graphs in Figure 10. 3D and 2D plots of the output power and drain efficiency as a function of second- and third- harmonic reactance values depicts the design sensitivity to harmonic loads based on how the drain-source capacitance is modelled (linear vs. nonlinear). The fundamental-frequency termination, but different harmonic terminations, shows the power and efficiency for Class-B operation is 44.7 dBm and 57.7% and degraded to 44.2 dBm and 49% if the harmonics are de-tuned to 90°. This extreme case illustrates that the performance can degrade substantially if the harmonic impedances are off-target.

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<td>3.5” x 1.5” x 0.5”</td>
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<tr>
<td>HADA-D2001</td>
<td>500 - 2000</td>
<td>-44 dBm</td>
<td>50</td>
<td>-40 to 0</td>
<td>2.5” x 1.5” x 0.44”</td>
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<tr>
<td>SDLVA-0R5G4G-70dB-100R</td>
<td>500 - 4000</td>
<td>-73 dBm</td>
<td>25</td>
<td>-70 to 0</td>
<td>3.2” x 1.8” x 0.4”</td>
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<tr>
<td>SDLVA-0R71R3-75-CD-1</td>
<td>700 - 1300</td>
<td>-70 dBm</td>
<td>40</td>
<td>-70 to 0</td>
<td>3.75” x 1.5” x 0.5”</td>
</tr>
</tbody>
</table>
Figure 6 • A new model for the 25 W GaN transistor with access to intrinsic generator is embedded in a load-pull simulation setup.
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RoHS compliant

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### Electrical Specifications (-55 to +85°C base plate temperature)

<table>
<thead>
<tr>
<th>Model</th>
<th>Frequency (GHz)</th>
<th>Gain (dB)</th>
<th>P1dB (dBm)</th>
<th>IP3 (dBm)</th>
<th>NF (dB)</th>
<th>Price $ (Qty. 1-9)</th>
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<tbody>
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<td>ZVA-183WX+</td>
<td>0.1-18</td>
<td>28±2</td>
<td>27</td>
<td>35</td>
<td>3.0</td>
<td>1479.95</td>
</tr>
<tr>
<td>ZVA-183GX+</td>
<td>0.5-18</td>
<td>27±2</td>
<td>27</td>
<td>36</td>
<td>3.0</td>
<td>1479.95</td>
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<td>3.0</td>
<td>935.00</td>
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<tr>
<td><strong>NEW!</strong> ZVA-203GX+</td>
<td>2.0-20</td>
<td>29±1</td>
<td>17</td>
<td>27.5</td>
<td>3.0</td>
<td>1295.00</td>
</tr>
<tr>
<td>ZVA-213X+</td>
<td>0.8-21</td>
<td>26±2</td>
<td>24</td>
<td>33</td>
<td>3.0</td>
<td>1039.95</td>
</tr>
<tr>
<td>ZVA-213UWX+</td>
<td>0.1-20</td>
<td>15±1</td>
<td>15</td>
<td>30</td>
<td>3.0</td>
<td>1795.00</td>
</tr>
<tr>
<td><strong>NEW!</strong> ZVA-403GX+</td>
<td>0.005-40</td>
<td>11±1.5</td>
<td>11</td>
<td>23</td>
<td>4.0</td>
<td>1995.00</td>
</tr>
</tbody>
</table>

*Heat sink must be provided to limit base plate temperature. To order with heat sink, remove “X” from model number and add $50 to price.

### Wideband Performance

- ZVA-183WX+
- ZVA-183GX+
- ZVA-183X+
- ZVA-203GX+
- ZVA-213X+
- ZVA-213UWX+
- ZVA-403GX+
The fundamental-frequency impedance is pre-defined for maximum power from a 10-W GaN HEMT device operating at 2.45 GHz, while the reactance values at the second- and the third-harmonic frequencies are swept. The graphs on the left and in the center show power and efficiency versus the second- and third-harmonic reflection-coefficient angle, while the graph to the right shows merged two-dimensional cross-sections for a chosen performance target (power higher than 10-W power and efficiency higher than 80%).
These graphs show a very wide area of acceptable reactance values for the harmonic terminations and very deep poor-performance valleys, which should be avoided.

The nonlinear transistor models used in some scientific papers are more advanced than the models provided by many transistor manufacturers. In [3] the output capacitor \((C_{ds})\) of the transistor is modelled as nonlinear and it is shown that this substantially widens the useful impedance area for high-power and high-efficiency performance. The nonlinear models provided by most transistor manufacturers are, however, simplified and the output capacitors have fixed values.

Furthermore, commercial models are sometimes not validated even up to the third harmonic of the upper end of the useful fundamental-frequency range. To emphasize the importance of modelling \(C_{ds}\) as nonlinear, the two graphs shown in Figure 11 [3] compare the results of load-pull simulations with \(C_{ds}\) constant and \(C_{ds}\) nonlinear. Modeling \(C_{ds}\) as constant leads to more restrictive requirements for the harmonics impedances.

Using Power Parameters, Matching Networks Synthesis, and Maximum-Efficiency Lines

Steve Cripps published a method of plotting load-pull power contours for a transistor stage operated in Class-A mode [6, 7]. The simple closed-form equations and a cascade LC model for the output of the transistor enabled reasonably accurate plotting of the constant-power contours. Cripps also showed that the elliptical shape of the constant-power contours was caused by the hard clipping of the intrinsic voltage and/or current at the I/V-plane boundaries and that they are derived by intersecting constant resistance and constant admittance circles. The constant resistance circle segment is where the intrinsic current clips, while the voltage clips on the constant admittance circle segment.

The Cripps load-line concepts were adopted and extended in the specialized commercially available software tool Amplifier Design Wizard (ADW) [9]. The first extension was to use four arbitrary lines to define the load-line boundaries instead of assuming a rectangular load-line area. The problem of finding the external load line associated with the required intrinsic load line was solved by using the power parameters introduced by Abrie [8]. The intrinsic voltages and the intrinsic output current were mapped to the external voltages for any arbitrary linear network. This network usually consists of the full linear model for the transistor (package included) and any network elements (arbitrary) between the transistor and the matching network. The reverse feedback of the transistor is also accounted for in this approach and external feedback is also permitted. Losses (resistors) are allowed in the transistor model, as well as the external network.

Using the complete linear transistor model and the mapping functions of the power parameters, intrinsic load
lines can be mapped directly to external load lines at any frequency of interest, with no restrictions on the transistor configuration, feedback, resistive losses, transmission lines, grounding node position, etc. The power generated by the transistor is determined by the intrinsic load line and the load-line boundaries. Constant-power contours can be generated for Class-A, Class-B, Class-AB, Class-F, and inverse Class-F operation.

Load-pull results from a harmonic-balance simulator and the ADW validate the accuracy of this method. The graph on the left in Figure 13 represents the simulated constant-power contours of an amplifier stage in Class-B operation (5 dB into gain compression). The center graph is the load-pull contours produced in the ADW for Class-B operation with pre-hard-clipped load lines. The graph on the right shows the excellent agreement between measurements.

All the points of maximum power and maximum efficiency of the load-pull contours (Figure 14), starting with the peak-power point for
25

Class-B operation, are lined up on a reasonably smooth curve. This curve will be referred to as the maximum-efficiency line. For a given class of operation, the efficiency will increase initially along the maximum-efficiency line as the power is decreased from its peak value. The class of operation can be changed when the peak-power point for that class is reached, at which point the efficiency will jump to correspond to the new class.

The maximum-efficiency points are positioned on the voltage-clipping side, which at the intrinsic generator is on the constant admittance circle segment and is the side with higher intrinsic load resistance. They are also purely resistive and hence lie on the central horizontal line of the Smith Chart. At the intrinsic reference plane, the power contours are perpendicular (vertical) to the central horizontal line of the Smith chart (contours not rotated).

When the contours are mapped from the intrinsic generator plane to the output of the transistor using the power parameters, the contours shift and tilt, as shown in Figure 15, and some dispersion is in effect, depending on the complexity of the transistor model. By plotting the maximum-efficiency points on any power contour, the designer is able to set and visualize the desired compromise point for achieving the optimum tradeoff between power and efficiency.

If a Class-B, Class-F or inverted Class-F stage is to be designed with harmonic control, the fundamental-frequency load line at each passband frequency can be set to the peak-power termination (or a scaled version of it) or can be chosen to be the optimum point on the power contour targeted, or a circular area around it.

The second- and third-harmonic impedances can be specified to be low or high, relative to the fundamental-frequency impedance (near short or near open), depending on the desired class of operation. Exact shorts, opens or harmonic reflection coefficients (continuous modes)

Figure 12 • The intrinsic load lines from the I/V plane can be mapped directly into external load lines. The power parameters are used to create constant-power contours for the external load line on the Smith chart.

Figure 13 • Comparison of constant-power contours generated using load-pull analysis of nonlinear model (left) to the output power contours generated using the linear model and power parameters (center).
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PAs

will place very stringent demands on the external harmonic impedances and are not required.

**Design Demonstration and Validation**

After extracting a linear model for the transistor, the fundamental-frequency impedances were selected to be the maximum-efficiency points on the power contours targeted (points on the maximum-efficiency lines) at a number of frequencies across the bandwidth. Power levels below the peak were targeted in seeking the optimum trade-off between power and efficiency (Figure 16).

Lumped-component load networks were synthesized for different power levels and different combinations of low and high harmonic impedances. These networks were then imported into the simulator for nonlinear simulation and verification. After a few iterations the desired amplifier response was obtained and a final network of mixed microstrip transmission lines and surface-mount compo-

![Figure 13](image1.png) • The graph shows the superimposed constant-power and constant-drain efficiency contours generated in Microwave Office software.

![Figure 14](image2.png) • The ADW-derived constant-power contours at four frequencies across the passband are shown with the maximum-efficiency lines.

![Figure 15](image3.png) • ADW constant-power contours with the markers placed on the maximum drain efficiency points of the power contours.
Figure 16: Artwork view of the synthesized output impedance matching network.

Figure 17 • Comparison of amplifier maximum power, power gain, PAE, and input return loss for the initial design method (faded traces) and the new design approach.
nents was synthesized. The parasitic elements and the pads of the lumped components and discontinuities of the microstrip network are accounted for automatically during synthesis.

The final version of the synthesized network, Figure 17, was imported into the general simulator design environment for further layout detailing, along with the nonlinear model and its artwork information. Sections of the design were set up for EM simulation and harmonic-balance was used to verify the design.

The simulation results for the new design method are compared with those of the previous design method (faded traces) in Figure 18.

The new design method provides wider bandwidth (~100 MHz to both the upper and lower edges of the bandwidth) with negligible reduction of output power and efficiency.

Conclusion

The design approach in this article is based on selecting the fundamental frequency impedances on the maximum efficiency lines of the load-pull power contours. The desired harmonics impedances are also defined. Combined with the extended Cripps load pull method and real-frequency matching networks synthesis technique the approach provides an efficient (fast) design method that is no less accurate than methods that only use nonlinear transistor models and harmonic-balance simulated load-pull data.

References

1. Ivan Boshnakov, “Practical design approach of RF PA for high efficiency using simulated Load-Pull and real-world network synthesis with control of the harmonics impedances”, AWR PA Forum at EuMW, October 2014


7. Steve C. Cripps, “GaAs FET Power Amplifier Design”, Matcom, Inc., Technical Note 3.2


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<th>Gain (dB)</th>
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Advanced Materials

We are the world’s technology leaders in innovative solutions for power electronics, advanced foams for cushioning and protective sealing, and high-frequency printed circuit materials. When reliability, efficiency and performance are critical, design engineers partner with Rogers to develop and deliver the material technologies they require. For over 180 years, we have developed new solutions to empower our customers’ breakthroughs and help them create a leaner, safer, and more connected world. Headquartered in Chandler, Arizona, USA, we serve our customers and partners around the globe.

Rogers Corp.
Booth # 448

RF and Microwave Subsystems

Founded in 2009, SignalCore, Inc. is a privately held company based in Austin, Texas. SignalCore designs and manufactures high quality, instrument grade RF and microwave subsystems. We serve customers worldwide in the industries of measurement, communications, aerospace, defense, academia, and electronics manufacturing. Our extensive engineering knowledge and experience in the design and manufacturing of high performance RF and microwave solutions ensures that our products are of the highest quality and reliability in the industry.

SignalCore
Booth # 274

Resistives Expertise

State of the Art, Inc. is the leading supplier of thick and thin film resistive components to the Biomedical, Communications, Aerospace, and Defense industries. We are the industry leader in providing customers with quality, reliability, value, prompt and courteous customer service, and the most advanced technology available. We are dedicated to achieving and maintaining an unsurpassed level of excellence in all aspects of our operations. We are committed to the ethical behavior and the fair treatment of our customers, suppliers, community, and fellow employees.

State of the Art
Booth # 1129
Times Microwave Systems is a subsidiary of Amphenol Corporation (NYSE: APH) and part of the Amphenol Military and Aerospace division. TMS designs and manufactures high performance coaxial cables, connectors and cable assemblies for military, aerospace, telecommunications, industrial RF and microwave applications. For over 70 years Times has been committed to innovation, quality and the development of new products for demanding applications.

### Power Sensor: Advanced Video Filters

LadyBug Technologies’ LB480A and LB680A RF Power Sensors with Option 004 make wide bandwidth time domain trace measurements. The detected video filters include a selection of 9 frequencies between 100 kHz and 10 MHz.

The filters are ideal for honing in on your signal’s modulation. Along with LadyBug’s advanced averaging techniques, the filters can aid in reducing noise that interferes with the desired video information. Signals can be cleaned so that accurate peak and pulse power levels are quickly measurable.

Additionally, the sensors can make statistical pulse measurements programmatically or with LadyBug’s Power Meter Software. This makes them ideal for manufacturing test systems. Filters are provided with option 004 on Ladybug LB480A (50-MHz to 8-GHz) and are included with the LB680A (50-MHz to 20-GHz) power sensors.

Extensive programmatic support is provided for system builders.

LadyBug Technologies
Booth # 1255

### MM-Wave Expertise

Norden Millimeter has extensive experience in product development and manufacturing of millimeter wave amplifier products to specific customer specifications with quality and customer satisfaction the ultimate objective. MMIC technology is used extensively throughout our product base. Extensive qualification is used to insure MIC integrity during our manufacturing process and for our customer’s final application. Waveguide is offered for our millimeter wave products. WR-42, WR-28, WR-22, & WR-19 waveguide connectors can be used on all of our standard housings in lieu of threaded connectors. WR-15, WR-12 and WR-10 housings are split-block designs with waveguide being an integral part of the housing.

Norden Millimeter
Booth # 1306
**Tiny MMIC Gain Slope Equalizers Flatten DC-20 GHz**

Mini-Circuits’ EQY-5-24+ is an absorptive MMIC gain equalizer with a negative 5.1 dB slope versus frequency from DC to 20 GHz. Fixed slope MMIC equalizers are useful for flattening negative gain slope in wideband amplifiers, receivers and transmitters in applications from wireless communications to broadband/optical, satellite, defense and more. This model is capable of handling up to +34 dBm RF input power and provides 20 dB typical return loss across its full bandwidth. Fabricated using highly repetitive GaAs IPD technology, this equalizer provides outstanding repeatability of performance, making it suitable for volume production. It comes housed in a 2 x 2mm 8-lead QFN package, saving board space and minimizing the effect of parasitics. EQY-series MMIC gain slope equalizers are available with a wide range of slope values to meet your needs.

**High Dynamic Range MMIC Amplifier with Shutdown Feature, 1 MHz to 1 GHz**

Mini-Circuits’ TSS-13LN+ ultra-high dynamic range MMIC amplifier provides industry-leading noise figure and IP3 from 1 MHz to 1 GHz. An internal shutdown feature protects the amplifier in the presence of pulsed signals while keeping the power supply at constant voltage to minimize DC power consumption. This model provides 1.1 dB noise figure and +39.2 dBm IP3, making it ideal for maximizing sensitivity and dynamic range in high-performance receiver applications. It delivers 22.8 dB typical gain with ±3.0 dB flatness, and +19 dBm output power at 1 dB compression. The amplifier is fabricated using E-PHEMT technology with excellent repeatability. It operates on a single 8V supply, and comes housed in a tiny 12-pad 3x3mm QFN package.

**Tiny High-Rejection LTCC Low Pass Filter, DC to 530 MHz**

Mini-Circuits’ LFCG-530+ is an LTCC low-pass filter with a passband from DC to 530 MHz. This model provides 1.0 dB typical passband insertion loss and stopband rejection of 30 dB typ. The filter is capable of handling up to 4W RF input power and provides a wide operating temperature range from -40°C to 85°C. Housed in a tiny 0805 ceramic form factor with wraparound terminations, the LFCG-530+ is ideal for dense PCB layouts with minimal performance variation due to parasitics.

**Tiny LTCC Dual/Differential Low Pass Filter, DC to 1600 MHz**

Mini-Circuits’ DLFCV-1600+ is a dual low pass filter with a passband from DC to 1600 MHz designed into a single 1210 ceramic package. This design allows customers to use a single unit in systems where two filters of the same passband are required, saving board space. The dual filter can also be used as a differential filter in differential circuits where interference and noise must be minimized. This model provides 1.5 dB passband insertion loss, 50 dB stopband rejection, and RF input power handling up to 3W (each filter). It supports a wide range of applications and is ideal for minimizing interference at amplifier inputs and ADC outputs.

**Ultra-Low Noise D-PHEMT Transistor, 10 to 4000 MHz**

Mini-Circuits’ TAV1-331+ is a MMIC D-PHEMT transistor with an operating frequency range from 10 to 4000 MHz, supporting a wide range of wireless communications bands. This model provides a unique combination of low noise (0.6 dB) and high gain (24.1 dB), resulting in lower overall system noise. It also provides high IP3 performance of +31.8 dBm, making it ideal for sensitive receiver applications. Manufactured using highly repeatable D-PHEMT technology, the unit comes housed in a tiny 1.4 x 1.2mm MCLP package. This model requires external biasing and matching.

**Coaxial Adapter Mates 1.85mm-F to 2.92mm-F Connectors**

Mini-Circuits’ 185F-KF+ is a coaxial 1.85mm-F to 2.92mm-F adapter, supporting a wide range of applications from DC to 40 GHz. This model provides 1.05:1 VSWR, and 0.13 dB insertion loss with flat response over its full frequency range. The unit features rugged, passivated stainless steel construction and measures 0.82” in length.
24 GHz to 44 GHz Wideband Up & Downconverter

Analog Devices announced the ADMV1013 and ADMV1014, a paired highly integrated microwave upconverter and downconverter, respectively. These ICs operate over a very wide frequency range with 50 Ω-match from 24 GHz up to 44 GHz, facilitating ease of design and reducing the costs of building a single platform that can cover all 5G mm Wave frequency bands including 28 GHz and 39 GHz.

Additionally, the chipset is capable of flat 1 GHz RF instantaneous bandwidth supporting all broadband services as well as other ultra-wide bandwidth transceiver applications. Each upconverter and downconverter is highly integrated, comprising I (in-phase) and Q (quadrature-phase) mixers with on-chip programmable quadrature phase-shifter configurable for direct conversion to/from baseband (operable from DC to 6 GHz) or to an IF (operable from 800 MHz to 6 GHz). Also included on-chip are voltage variable attenuators, transmit PA driver (in the upconverter) and a receive LNA (in the downconverter), LO buffers with x4 frequency multiplier and programmable tracking filters.

Most programmability functions are controlled via an SPI serial interface. Through this port, these chips also provide a unique capability for each upconverter and downconverter to correct its respective quadrature phase imbalance, hence the usually difficult to suppress sideband emission can be improved from a typical value of 32 dBc, by 10 dB or more. This results in an unmatched level of microwave radio performance. The combination of features provides unprecedented flexibility and ease of use while minimizing external components, enabling implementation of small form factor systems such as small cells.

Analog Devices
Booth # 918

Ducommun RF Switching Solutions from DC-110 GHz

PIN diodes from 30MHz to 110 GHz
- SPST, SPDT
- SP4T, SP6T, SP8T
- Broadband, Narrowband
- High-Power

Coax switches from DC to 46 GHz
- SPDT, Transfer
- SP3T-SP10T
- Non-terminated & Terminated
- 50Ω and 75Ω impedances

Ducommun offers Switch Matrix Solutions!

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For additional information contact our sales team at: 310-513-7233 or rfsales@ducommun.com
side of the attenuator; however in cases where large source mismatch presents an issue, these attenuator mismatch errors are generally small in comparison to the larger source mismatch. Users requiring the highest level of accuracy should take all factors into account.

While mismatch is usually the most significant component of a measurement’s uncertainty it is only one of many. Another component is the sensor’s Calibration Factor uncertainty. This important uncertainty represents the accuracy of the sensor’s calibration, and is often stated by manufacturers as the sensor's accuracy because the DUT mismatch is unknown. However sensor-to-DUT mismatch is most often a more significant uncertainty.

An easy way to begin calculating measurement uncertainty and increase your overall measurement accuracy and understanding, is to workup the uncertainty of a measurement using a power sensor manufacturer’s uncertainty worksheet or spreadsheet. For example, the last pages of the above-mentioned LB5940A power sensor’s data sheet includes a worksheet and completed example that covers the most significant factors in a typical power sensor measurement. Most high quality power sensor manufacturers provide similar worksheets.

A power sensor manufacturer can supply specifications. However, it is not possible to determine the accuracy of any measurement without knowing the measurements parameters. Most of the specifications have an associated parameter such as frequency or power level. These will determine which specification from the sensors data sheet is applicable. Once these are all known, they can be included in an RSS calculation to determine the total measurement uncertainty.

In conclusion, for the best accuracy, make the distinction between sensor accuracy and measurement accuracy, then use the sensor’s specifications to develop a full understanding of your measurement’s uncertainty. This will give you confidence in the measurement and allow you to improve the accuracy as needed.

About the Author

Orwill Hawkins serves as VP of Marketing at LadyBug Technologies.
QUALITY, PERFORMANCE AND RELIABILITY IN PRECISION COAXIAL CONNECTORS

Including These Connector Series

<table>
<thead>
<tr>
<th>Connector Size</th>
<th>Frequency Range</th>
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</thead>
<tbody>
<tr>
<td>1.85mm</td>
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<td>DC-34 GHz</td>
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<tr>
<td>7mm</td>
<td>DC-18 GHz</td>
</tr>
</tbody>
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SGMC Microwave
Manufacturer of Precision Coaxial Connectors
620 Atlantis Road, Melbourne, FL 32904
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