RF Component Integration – Saving Space in High Performance Applications

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Significant opportunities exist to make circuits smaller, while still maintaining a high level of performance.

Introduction

A higher level of RF component integration is a trend which is visible across the semiconductor industry. However, the level of integration that has been achieved varies significantly by application, with a tendency to have less integration in applications where higher performance is required. This article will look at the kinds of signal chains and applications that have tended to use discrete high performance RFICs. By looking at recent advancements in component integration we will identify those areas where significant opportunities exist to make circuits smaller, while still maintaining a high level of performance.

In deciding how to approach the design of a wireless transceiver we must decide early whether to build the circuit discretely. To implement popular radio standards such as Bluetooth, Zigbee, or GPS, it makes little sense to attempt a discrete implementation. By the same token these highly integrated chipsets are of little use beyond their native application. In general we can conclude that highly integrated chipsets are optimal from a space perspective, and typically have lower performance compared to circuits implemented using discrete components, but they are also less flexible. This leads to the question of whether or not there is a level of integration that saves board space, but which still affords the designer an appropriate level of flexibility?

Size Matters

Let's start by considering the relative sizes of the typical components in today's RF signal chains. Modern active components such as IQ modulators, IQ demodulators, and mixers are usually available in lead frame chip scale packages (LFCSP) that are typically 16 square millimeters to 36 square millimeters. Voltage controlled oscillators (VCO) and surface acoustic wave (SAW) filters can be relatively large. 100 square millimeters is not an unusual size for a discrete VCO, while SAW filters can easily have a surface area of 35 square millimeters.

VCO Integration

Since VCO's seem to consume significant real estate on a circuit board, and since most RF transceivers require a local oscillator (LO), let's take a look at recent technology developments in this area.

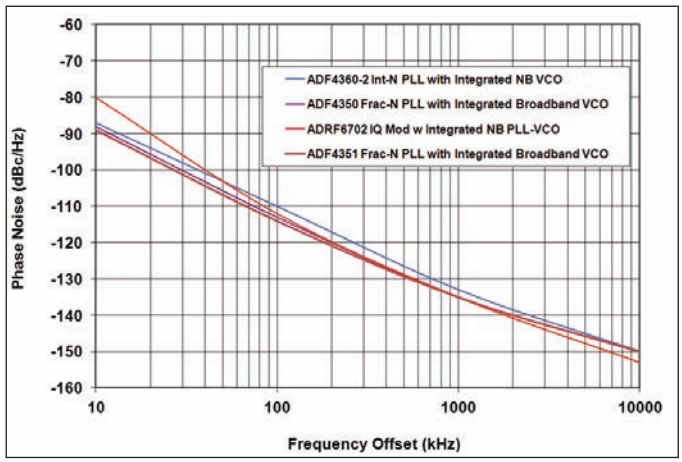


Figure 1 • Integrated PLL/VCO Phase Noise Comparison at 2.2 GHz.

Component Integration

The two primary components in a phase locked loop (PLL) based synthesizer are the PLL itself and the VCO. Because the size, and sometimes also the height, of discrete VCO's are relatively large there has been a focus in the IC design community on integrating VCO's into PLL's. While integrating a VCO into a silicon IC is not particularly difficult, integrating a high quality VCO is not trivial. And when we say high quality, we are referring the phase noise or spectral purity of the signal. Lower VCO phase noise improves receiver sensitivity and error vector magnitude (EVM) of both the transmitted and received signal. Figure 1 compares open-loop phase noise performance of some VCO's which have been integrated into RFIC's.

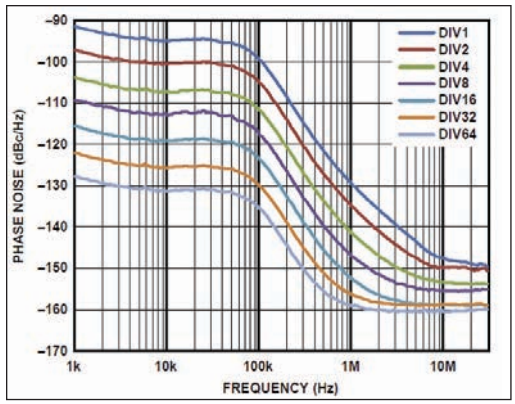


Figure 2 • The Closed-Loop Phase Noise of the ADF4351 PLL, with the VCO Operating at 4.4 GHz.

Two of these plots come from the ADF4350 and ADF4351. These are a family of PLL's with integrated VCO's. In addition to having very low phase noise, the VCO banks in these devices have a full octave of tuning range. Combining this octave of VCO tuning range with a bank of frequency dividers, yields a device in a 5 mm x 5 mm MLF package which can operate continuously from 35 MHz to 4.4 GHz. Figure 2 shows the closed-loop phase noise of the ADF4351 PLL at a series of output frequencies. In this case the VCO is operating at 4.4 GHz.

The closed loop phase noise at 4.4 GHz is indicated by the dark blue curve at the top of the plot. As each frequency divider is engaged, the output frequency halves and the phase noise improves by 6 dB. So with both the VCO and the frequency divider bank on-chip, the only remaining external components are the power supply decoupling capacitors and the external loop filter.

Receiver Architecture Evolution

Next let's take a look at the evolution of receiver architectures and how this is impacting the size of these circuits. If we look back a few years we see that a typical diversity receiver already had a reasonable level of integration (Figure 3). One the RF side of the mixer however, the LNA's and variable attenuators are all discrete, and the LO for the mixer is implemented using an external VCO.

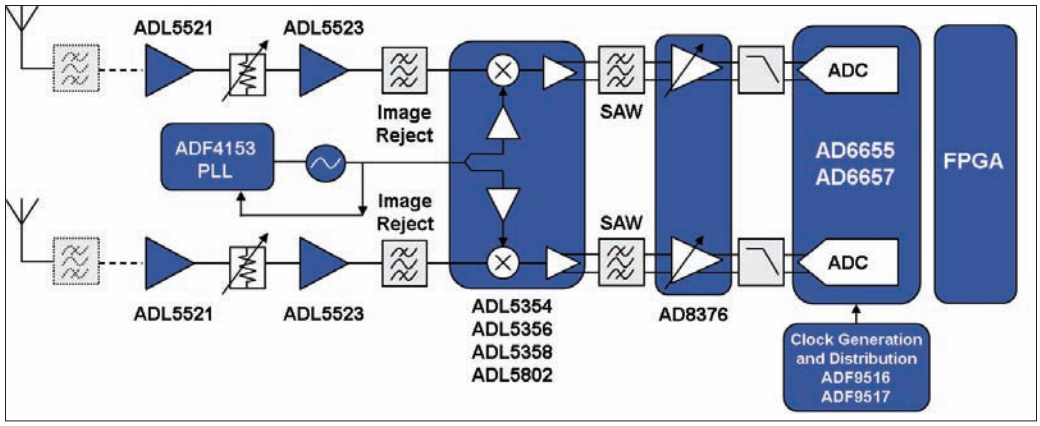
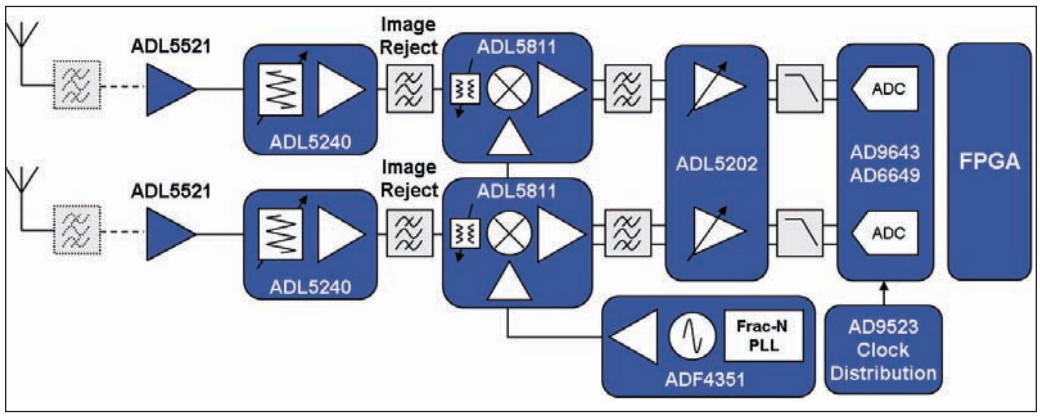


Figure 3 • IF Sampling Receiver Signal Chain, Circa 2009.

Figure 4 • State-of-the-Art IF Sampling Receiver Signal Chain.



Now let's fast-forward a few years. Referring to Figure 4, we see that for most applications the PLL with discrete VCO can be replaced by a single integrated device as already noted. In addition, there is an increased level of integration on the RF side of the mixer. In this case the post-LNA amplifier has been integrated with a variable attenuator. We refer to this as "horizontal integration" where adjacent components in the signal chain are merged into a single package. It is notable however that the front-end LNA is still a stand-alone component. This is primarily due to semiconductor process incompatibilities between LNA's (usually fabricated in GaAs pHEMPT) and the typical down-stream components in a receiver such as digital step attenuators (DSA) and broadband amplifiers.

When we integrate components in a diversity receiver, another option to consider is "vertical integration." In the receiver shown in Figure 4, a dual ADC and a dual ADC driver have been chosen but the mixers and RF VGA's are separate components. One critical factor that must be taken into account when integrating vertically is the parasitic coupling or leakage between devices. Figure 5 shows the channel-to-channel isolation of the ADL5812 dual broadband passive mixer with integrated intermediate frequency (IF) amplifiers. Notice how the level of leakage increases as the RF input frequency increases.

This increase in channel-to-channel leakage is very typical because the impedance of parasitic coupling paths tends to decrease with increasing frequency. As a result, vertical integration is less popular on the RF side of mixers. In the case of mixers single and dual versions are generally offered so that the designer can decide on the level of integration versus the level of isolation required between the devices.

Zero IF Receive – Does it Save Space?

In recent years there has been a renewed interest in replacing the popular IF sampling architecture with a so-called direct conversion, or zero intermediate frequency receiver (ZIF). In a ZIF receiver the RF signal is mixed down to baseband in a single step using an IQ demodulator, as shown in Figure 6. The main appeal of this architecture is that the need for the front-end image-reject filter and IF SAW filter, with its relative large size and insertion loss, are eliminated. This architecture does have size advantages and the approach is also very frequency agile because there is no IF and frequency planning to worry about. The frequency range of the receiver is only limited by the operating range of the synthesizer and the IQ demodulator, as well as by the front-end LNA's. With the wide availability of broadband IQ demodulators and synthesizers, this approach has become quite popular, particularly in frequency-agile reconfigurable radios.

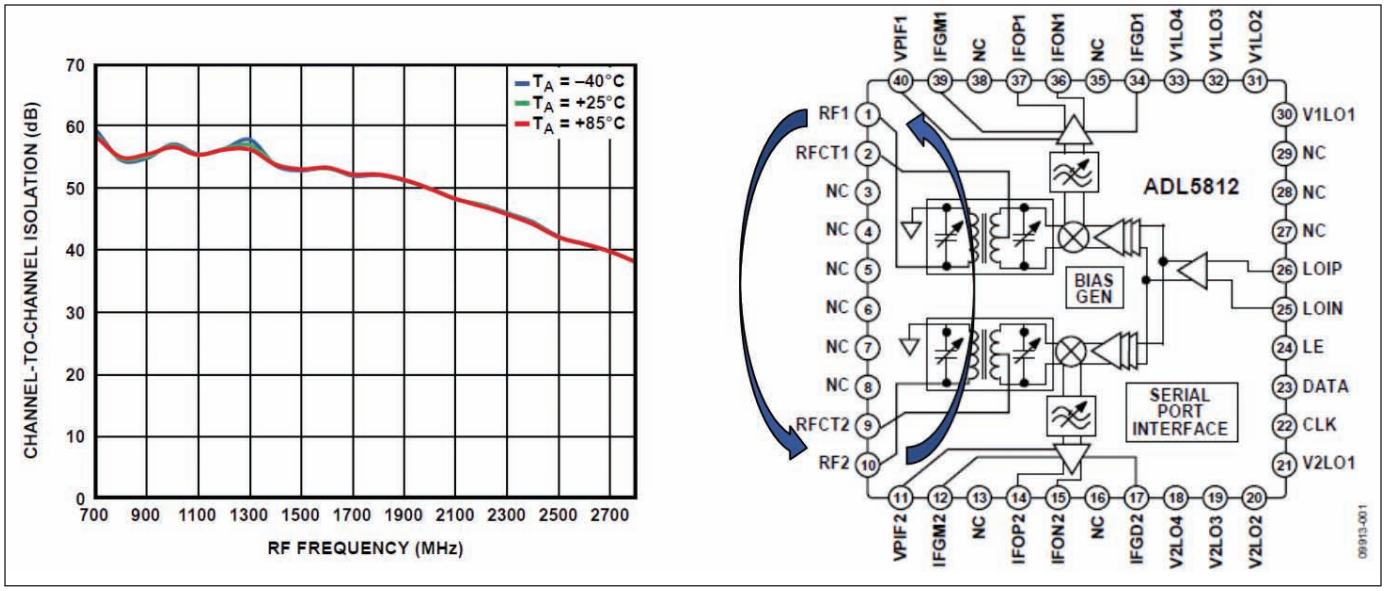


Figure 5 • Channel-to-Channel Isolation of the ADL5812 Dual Passive Mixer.

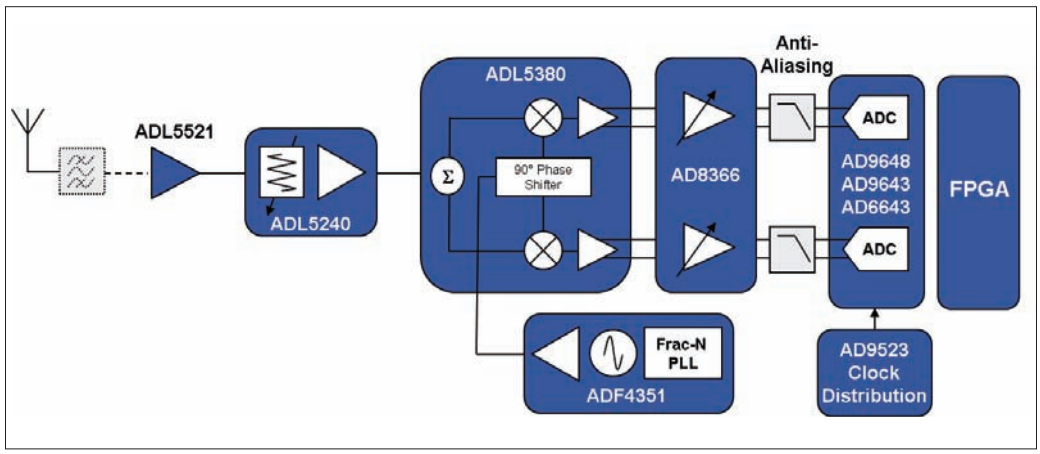


Figure 6 • Zero IF Receiver Block Diagram.

Zero IF receivers eliminate the need for an IF SAW filter, which rejects unwanted in-band and out-of-band signals. While this is a definite advantage, the job of eliminating these signals then falls to the anti-aliasing filter in front of the ADC. The ADRF6516 shown in Figure 7 is an example of a highly integrated device which helps to enable the direct conversion receive architecture. This device provides 50 dB of variable gain along with a programmable filter bandwidth that can be varied between 1 MHz and 30 MHz in 1 dB steps, all in a compact 5 mm x 5 mm LFCSP package.

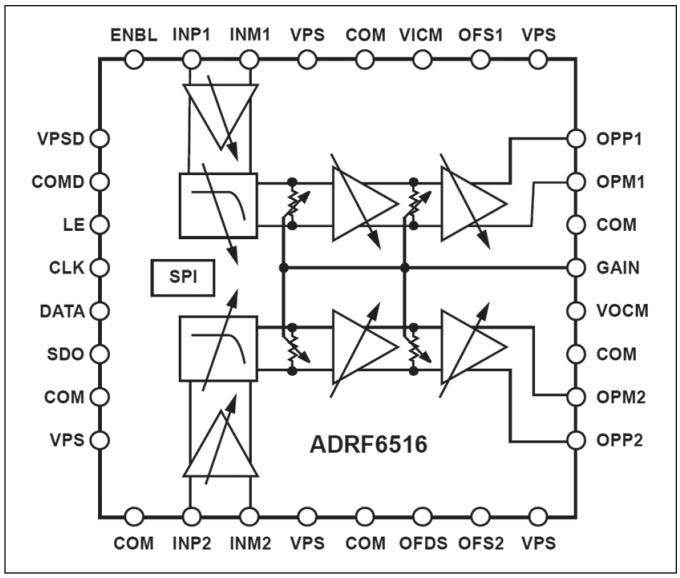


Figure 7 • Block Diagram of the ADRF6516.

Zero IF Versus IF Sampling

Let's now compare these two architectures in terms of performance and power consumption. Figure 8 shows an ADIsimRF signal chain analysis of a typical IF sampling receiver. At this gain setting we achieve an input IP3 of 27.8 dBm and a noise figure of 4.7 dB, while consuming 2.2 Watts.

If we simulate an equivalent zero IF line up in ADIsimRF (Figure 9), we find that it has about the same input IP3 but the noise figure is a fair bit lower at 2.1 dB. This is mainly due to the absence of the high loss SAW filter in the zero IF architecture. The power consumption

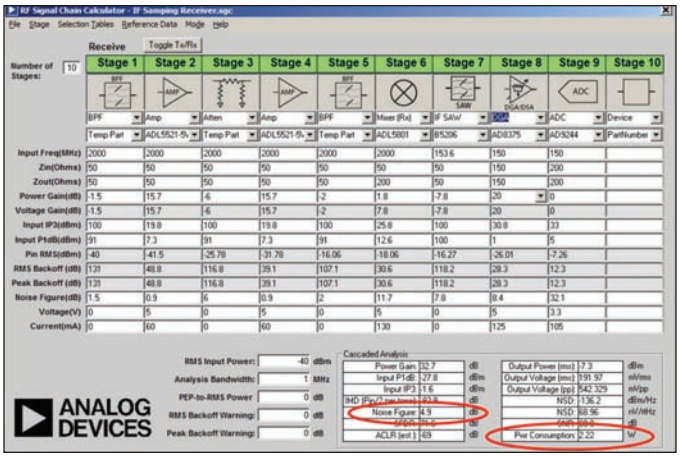


Figure 8 • IF Sampling Receiver Signal Chain Analysis.

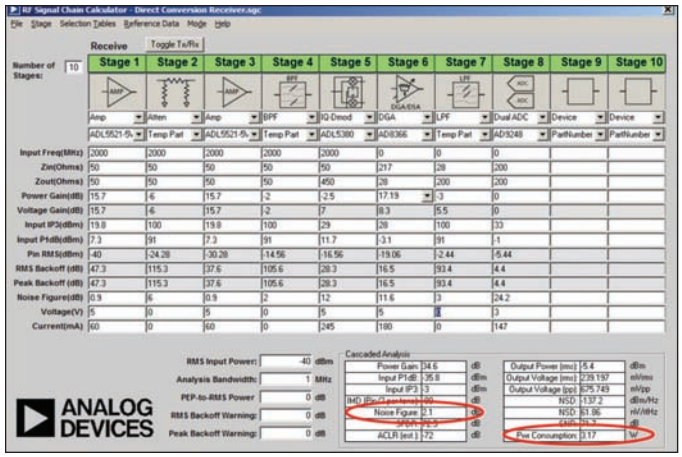


Figure 9 • Zero IF Receiver Signal Chain Analysis.

is higher though at 3.17 Watts. This is attributed to the need for two ADC's and two baseband amplifiers to drive them, compared to just one of each in an IF sampling receiver.

So in this case, even though an IF sampling ADC will typically have higher current than a baseband sampling ADC, the need for the two baseband ADC's, and two ADC drivers, negates this power consumption advantage. However, one factor that is not being considered here is the power consumption of the digital down conversion circuitry that is required in an IF Sampling receiver. This might bring the two approaches more into balance from a power consumption perspective.

Transmitter Evolution

Next let's look at how transmitters are evolving, to see what opportunities exist to save space. For radio frequencies that are in the 500 MHz to 6 GHz range the use of IQ modulators has become quite popular. Indeed, the adoption of direct conversion on the transmit side has been more widespread than on the receive side, where IF sampling or IF-to-baseband conversion using an IQ demodulator are still more popular. In the signal chain example in Figure 10 the transmitter also includes a loopback circuit which monitors the distortion of the power amplifier and provides feedback to the digital pre-distortion (DPD) algorithm which runs in baseband. In this configuration, instead of a true ZIF architecture, the DAC output is at 120 MHz, a so-called complex IF (CIF). This allows the use of a single LO to drive both the IQ modulator and the DPD mixer, as the IF frequency of the loopback circuit is also 120 MHz.

Dual DAC architectures have evolved so that in many cases a single device can support both ZIF and CIF signal chains. That is the device can generate a spectrum centered at baseband (0 Hz) or the device can digitally upconvert the signal to a complex IF. From an integration perspective devices such as the AD9122 (16-Bit, 1.2 GSPS) and AD9125 (16-Bit, 1 GSPS) provide the best of both worlds. They offer smaller package sizes of 10 mm x 10 mm, and additional signal processing functionality, with lower power consumption.

The IQ modulator used here, ADRF6702, is one of a family of four IQ modulators with integrated PLL and VCO that provide frequency coverage from 400 MHz up to 3.0 GHz. These devices conveniently provide an LO output which can drive the DPD mixer directly to facilitate using a single LO to drive both transmitter and loop-back receiver. Analog Devices also offers the ADRF660X family of mixers with integrated PLL and VCO's, as well as the ADRF680X family of demodulators with integrated PLL and VCO. This shows that one of the most common state-of-the-art form factors for highly integrated / high performance RF components consists of a frequency conversion component integrated with a PLL and a VCO.

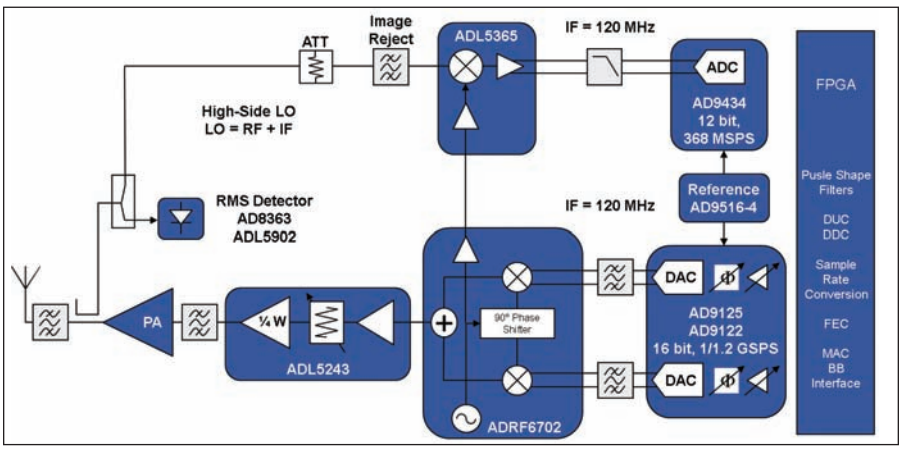


Figure 10 • Complex IF Transmitter Block Diagram with Loopback Circuit at the same IF.

This signal chain also shows a nice example of horizontal integration along the signal chain. The ADL5243 RF/IF VGA monolithically integrates two RF/IF amplifiers along with a digital step attenuator (DSA), all into a small 5 mm x 5mm LFCSP package. The first amplifier is a broadband matched gain block and the second amplifier is an externally matched ¼ Watt driver, along with the DSA being broadband matched supporting 31.5 dB range and a step size of 0.5 dB. The ADL5240 companion part combines the DSA with just the broadband gain block. In both cases, the individual elements are pinned out externally. This provides integration while maintaining maximum flexibility in that any component in the RF/IF VGA can be wired first.

Conclusions

When implementing popular wireless radio standards, particularly on the terminal side where dedicated chipsets are available, there is rarely a good case for implementing a discrete circuit. When a design is made with discrete components there is significant flexibility and higher performance is available, IP3 levels in the 25 dBm to 45 dBm range, but at the cost of higher power consumption. To achieve higher integration, while maintaining higher performance, RFIC's are now widely available that combine the frequency conversion component along with the necessary PLL and VCO. These RFIC's save significant board area when compared to a discrete implementation.

The use of direct conversion transmitters and receivers can save board space through the elimination of IF stages, and the associated filtering, but may not provide significant power savings compared to a conventional super heterodyne transceiver. However, direct conversion architectures do offer significant frequency agility particularly when the synthesizer has a multi-octave output frequency range.

Lastly, when considering a dual channel integrated solution close attention needs to be given to channel-to-channel isolation specifications to ensure system requirements are being met.

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