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Techniques for Low Voltage Power Amplifier Matching

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A straightforward matching technique can solve the problem of low output impedance in IC amplifiers that must produce >1 watt from a 1.8 V supply

There is rapid expansion in the use of short range digital wireless systems [1], using the license-free allocations around 915 MHz in the USA and 869 MHz in Europe that permit up to 1 watt output power. These RF systems now use digital signal processing (DSP) for modulation and demodulation so to get better circuit packing density, and take advantage of finer IC process geometries that generally use low voltage supplies. Of course, lower operating voltages have the further benefit that they reduce the power consumption of the digital circuits, always an important parameter in battery powered products.

However, reduced supply rails result in low impedances at the output of the power amplifier (PA) which can be difficult and inefficient to match. As a result, the power amplifier is often run from a separate, higher voltage, which has to be provided by an additional external regulator. With the constant pressure on commercial products for lower cost, the external parts count must be minimized.

The approach we have taken is to run the PA off the 1.8 V supply hat is already used as a common interface level in many products. This tutorial shows how it is simple to use a balanced amplifier with a low cost balun incorporated into the circuit board, so power outputs of more than 1 W can obtained at 900 MHz, even on a 1.8 V supply, with a minimum of external matching components.

Design Example

In this example we will use the RDS101, which is fabricated using a standard 0.18 µm CMOS process and assembled in a conventional 24 pin QFN package, frequently used for power amplifiers because the exposed die paddle is an effective heat spreader. The RDS101 (Table 1) is a polar modulation PA that is well suited to frequency and phase shift keying (FSK, PSK) often used in license-free data transmission. In addition, it has both analogue and digital amplitude modulation inputs so multi-level quadrature amplitude modulation (QAM) can be generated with no additional external components.

Parameter	Value	Units	Comments
Supply	1.8	V	Tolerance ± 5%
Process	CMOS		Geometry = 0.18 µm
Package	QFN24		
Frequency	850~950	MHz	
Power output	1.0	W	Minimum
RF input	+3	dBm	
Power control	6	bits	
Modulation	10	bits	Also 1V analog input

Table 1 · RDS101 power amplifier key characteristics.

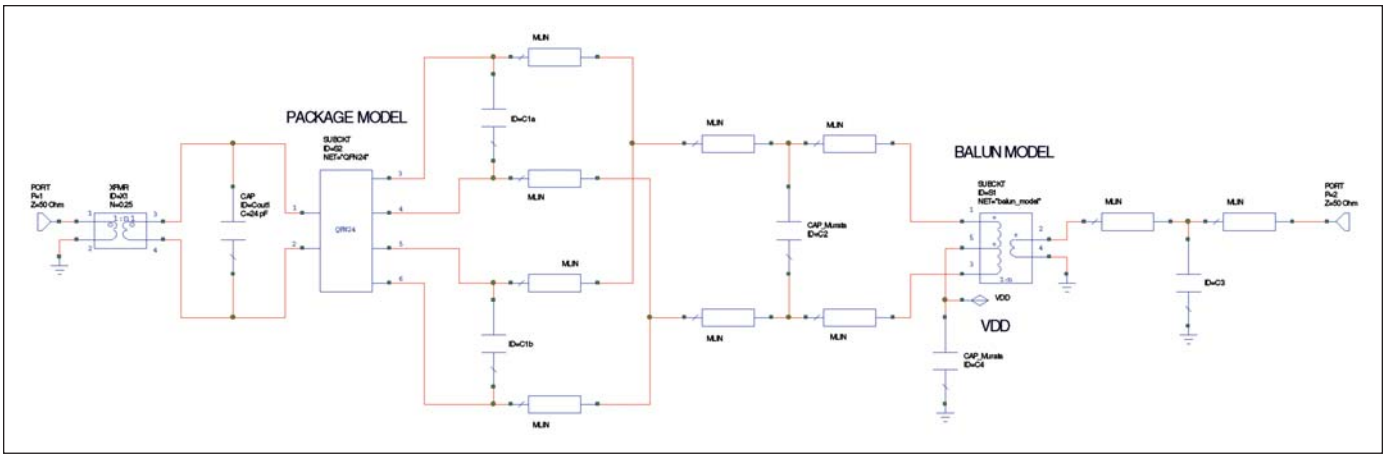

Figure 1 · RDS101 output match block diagram.

The RDS101 amplifier has balanced outputs giving significant advantages for low voltage operation as the output swing is doubled when measured across the differential output pins. The PA outputs are biased through the center tap of the output balun (Figure 1), which not only provides bias to the output, but also impedance transformation, simplifying the output impedance matching network [2] so only four tuning capacitors are needed. The only additional component is the decoupling capacitor on the supply connection.

Balun requirements include low loss and ability to handle the DC current flowing into the PA outputs. A balun printed in the PCB material avoids the cost of an additional component and, with no magnetic material, can easily cope with the DC bias.

The model of the balun is an important design input, but is easily derived as a differential version of a conventional transformer equivalent circuit (Figure 2). The primary winding has the center tap which is used for connecting the supply. The only significant addition to the model is the inter-winding capacitance of the secondary. This is needed because the secondary turns are stacked on two layers to reduce the balun area to 0.04 cm^2. The balun has a 3:1 turns ratio, giving a 9:1 impedance transformation.

The balun model was implemented in Microwave Office from AWR [3] which in common with other microwave simulators allows near real-time tuning of the schematic values to get an adequate fit to the measured *S*-parameters (Figure 3). The traces labelled 'tb_balun' are the measured *S*-parameters. The primary of the balun is connected to port 1, with the green trace as the measured impedance compared to the modeled trace which is colored cyan. The secondary is connected to port 2, with the measured S_{22} in blue while the model result is in grey. The balun measurements were made single ended, with ports 3 and 4 grounded, while port 5 on the primary center tap was left open.

A slight disadvantage of the printed balun is that for low cost it is fabricated in FR4 and this gives noticeable loss of about 0.6 dB, but as the PA easily achieves the required output, this is acceptable. In some applications where loss is more critical, a low loss substrate such as glass reinforced PTFE might be preferred [4].

The balun model is incorporated into the overall model for the amplifier PCB, including a model for the QFN package (Figure 1). The QFN package is a simple construction and when mounted on microstrip the leadframe has been considered to be part of the track, so only the bondwires need to be modeled, using the

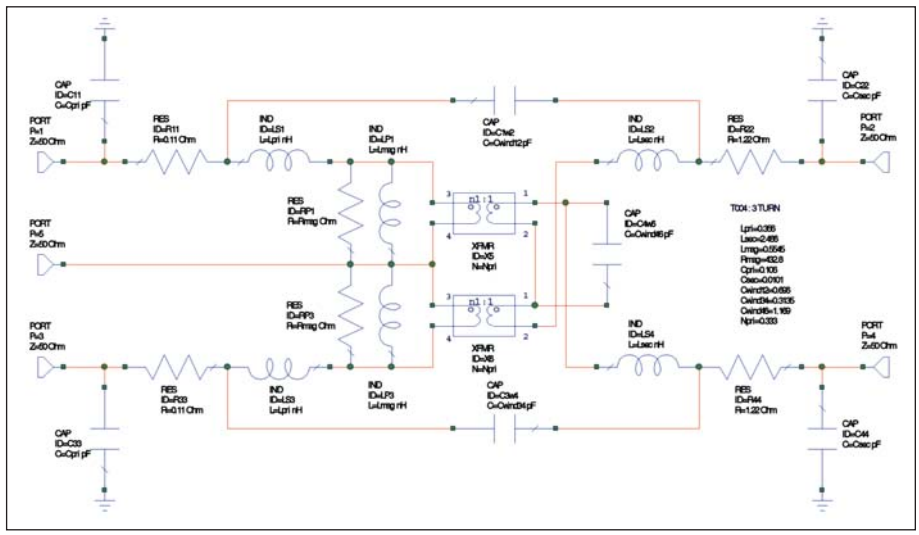

Figure 2 · Balun equivalent circuit.

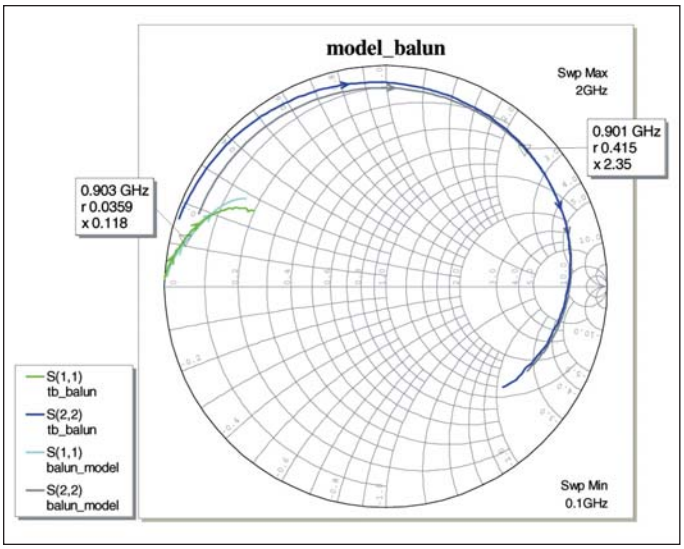

Figure 3 · Comparison of the balun model against measurement.

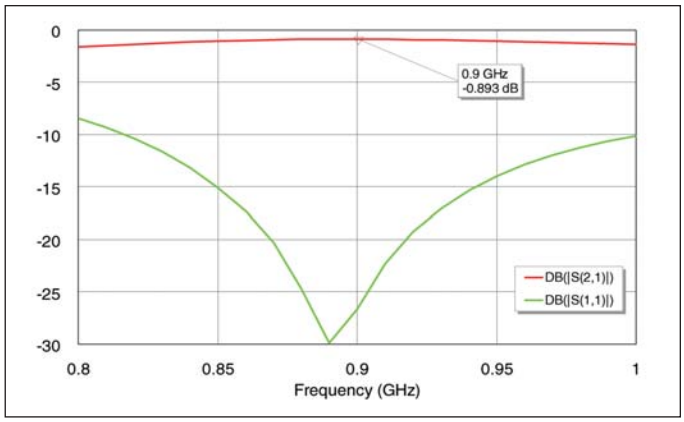

Figure 4 · Simulated output network response.

element available in Microwave Office. The PCB requires only four layers, with layer 2 largely a ground plane for the microstrip tracks on the top layer; while layer 3 is largely a power plane. Some experiments with the printed balun showed that the ground plane needs to be removed below the balun, otherwise there is significant eddy current loss.

Because of the low supply voltage, significant DC current flows through the amplifier output pins (about 2 A total at maximum power), so two pairs of pins are used in parallel for the balanced output. As a result, the first tuning capacitor is split into two components, with one chip capacitor across each pair of outputs. The capacitors need to be low loss so Murata GJM 0402 ceramic chips were used throughout—these are included in the simulation as library models which can be downloaded from Murata [5].

The tuning components are easily derived using the linear simulator. Referring to Figure 1 the amplifier output is represented by its capacitance of 24 pF differentially between the pins. The desired load line, in this case 3.1 Ω, is set by the transformer on port 1 which has a 4:1 turns ratio (hence a 16:1 impedance ratio). The printed balun turns ratio of 3:1 gives an impedance step down of 9:1 with the remainder of the transformation provided by a reactive L-match formed from the shunt capacitors C1 and C2 together with the inductance of the QFN leadframe and bondwires.

The optimizer in Microwave Office is then run with the target of maximising S_{21} to get the correct impedance match. For this design the optimization was carried out over the band 850 - 950 MHz to give adequate margin for covering the license free bands of 915 ±13 MHz in the USA and 869 ±1 MHz in Europe. The simulated S_{21} of the output matching network has a broad maximum (Figure 5) which shows the tuning is not critical. Note that the simulation is just for the output network and does not include the amplifier response—however this varies only slightly over the simulated range. The simulation of S_{11} represents the accuracy of the loadline presented to the amplifier. The network input return loss of better than 14 dB over the 850 - 950 MHz band represents a maximum VSWR of 1.5:1 which means the loadline is close to the desired value.

The broad maximum in the response shows the advantage of using a balun to achieve most of the impedance transformation from 50 Ω. With a 3:1 step down turns ratio the impedance at the balun primary is about 5.6 Ω. For a required loadline of 3.1 Ω, this requires the reactive match to achieve a transformation of less than 2:1, making it easier to achieve a wide bandwidth.

The output network loss is estimated to be about 0.9 dB at 900 MHz. As explained above, this is largely due to the balun printed on FR4. Above the bands of interest the output matching network response is low pass, which is useful in minimizing out-of-band harmonic levels.

The simulator can be used to derive the tuning capacitor values for different loadline impedances by setting the port 1 transformer to different turns ratios and re-running the optimization (Table 2). This shows the flexibility afforded by transforming the impedance with a balun, so the reactive match can then tune over a range of loadlines. The higher loadline impedances are suitable for lower power operation. When checking the PA tuning we found that using two smaller capacitors in parallel for C2 gave slightly better results due to the higher Q and reduced series inductance.

Measurements

The amplifiers were measured into a 50 Ω broadband 20 dB attenuator as the load using a 10% duty cycle, as required by the regulations of some license-free band

operations. Using the match from the linear simulation, the output power is centered around 900 MHz (Figure 5) and achieves 1 W output (30 dBm) with adequate margin. The power is slightly reduced at 869 MHz, but as only 0.5 W output (27 dBm) is permitted in Europe there is more than 3 dB margin available.

The efficiency, measured at the output socket, is better than 40% over the 915 MHz band. Using the matching network loss of about 0.9 dB given by the simulations, we can estimate an amplifier output power of about 1.8 W with an output efficiency of 50%.

As seen in Figure 5, the output is significantly above the permitted 1 W in the 915 MHz band. This is not a problem as the RDS101 output power can be adjusted, using a 6 bit digital control word programmed over a 3-wire bus, giving output power from maximum down to almost zero (Figure 6). A useful feature of the RDS101 is that the output stage is specifically designed for maintaining efficiency at lower power by reducing the current consumption in step with the control setting.

The effect is that the efficiency is still better than 30% at half power (Figure 7), whereas with constant current consumption in the output stage the efficiency would be 21% which is simply half that at the maximum power setting. The effectiveness of this current control technique gives further flexibility in trading power output against battery lifetime in portable products by, for example, reducing power at shorter ranges when the received signals are strong.

Loadline (Ω)	Turns ratio n : 1	C1 (F)	C2 (F)	C3 (F)	Comments
3.1	4.0 : 1	2 × 16p	28p	3.6p	Nominal match
4.5	3.3 : 1	2 × 13p	29p	3.6p	
6.1	2.9 : 1	2 × 12p	30p	3.3p	

Table 2 · Tuning for different loadlines.

Many proprietary data transmission systems in the license-free bands use FSK as it is simple to implement, robust, and can use a limiting IF chain in the receiver (as there is no amplitude information). But if higher data rates are needed, these can be obtained by going to QAM, using the amplitude modulation already included in the RDS101 amplifier. The modulation can either be provided digitally using an on-chip 10 bit digital-to-analogue converter (DAC) or as an analogue input voltage. Using the DAC for modulation gives the opportunity for the modulating waveform to be corrected for compression effects, as seen in Figure 8 by comparing the grey trace, which is the uncorrected characteristic, against the blue trace which is after linearization.

The output power in Figure 8 is plotted on a square law scale because the modulating signal, whether an external analogue signal or from the internal DAC, modulates the amplifier output voltage, which means that the power output is proportional to the square of the modulating signal. By plotting on a square law scale, a straight line is expected, that shows linearity more clearly.

Conclusions

This simple matching technique, based on a low cost balun, meets the needs of licence free data transmission for the 915 MHz band in the USA and the 869 MHz band in Europe. By allowing operation at 1.8 V it can share the supplies of the digital processor circuits but still achieve more than 1 W output with an efficiency which is adequate for commercial applications. This technique can obviously be extended to a power amplifier integrated directly into a wireless system on chip.

Acknowledgements

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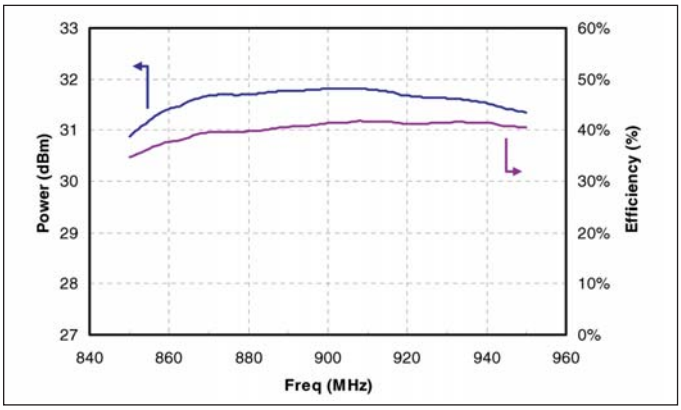

Figure 5 · Measured power and efficiency response.

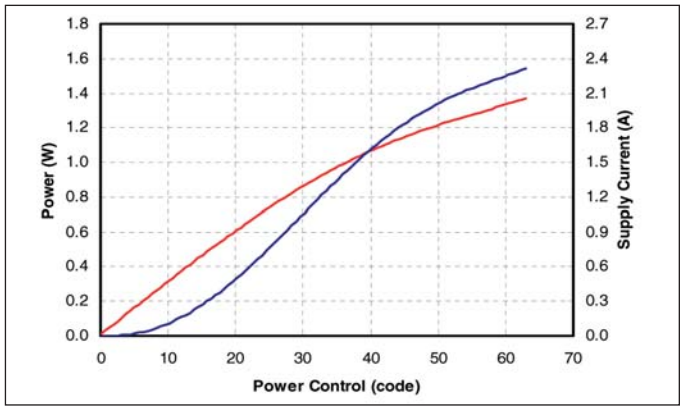

Figure 6 · Digital power output control.

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Author Information

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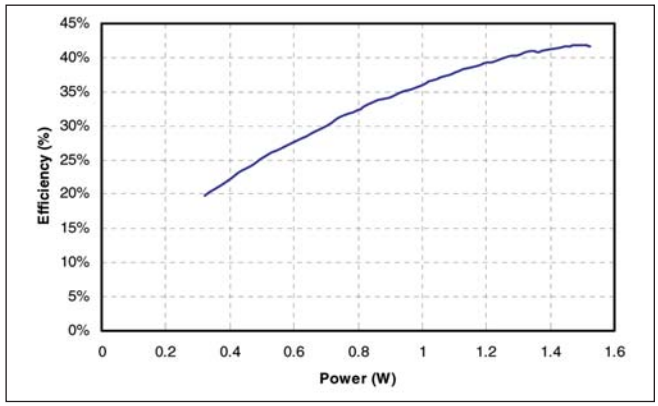

Figure 7 · Effect of power output on efficiency.

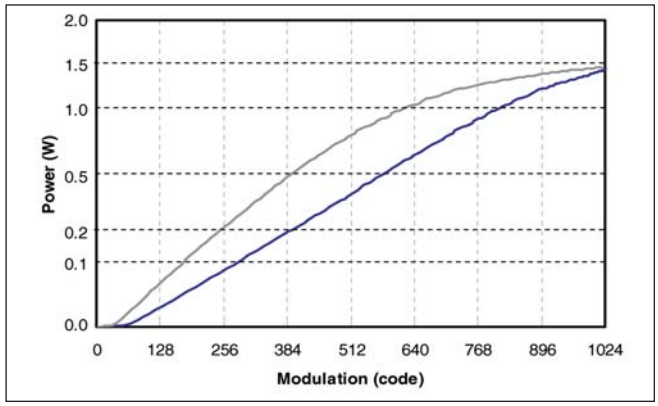

Figure 8 · Measured modulation characteristics.