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Practical Developments Using Today's Fractional Synthesizers

By Jim Carlini

This article reviews the design procedures for fractional-N synthesizers, with examples that demonstrate the performance achievable with currently-available PLL IC products

Integrated fractional PLL solutions have been available since the late 1990s. Over the past decade the in-band phase noise associated with the fractional processes has been greatly reduced. So have the troublesome fractional spurs. The base noise floor in dBc/Hz for some state of the art, low noise fractional PLLs approaches that of the lowest integer devices. Table 1 shows data for the recently released ADF4150 and the LMX2487E, which was recently reevaluated and found to have a lower noise floor then what's on the datasheet.

The table doesn't take into account PLL 1/*f* noise. 1/*f* noise is a phenomena that increases by 3 dB/octave at some break point close to the carrier frequency, i.e. 1 to 10 kHz. For low noise, narrow span applications this may be a concern.

The basic advantage of the fractional PLL is that the value of *N* by which the VCO is divided can be greatly reduced. In theory every time *N* is halved the phase noise goes down by 6 dB. However in reality it's increased 3 dB for every halving of *N* due to the 10Log(PFD) rule. In reality the situation is more complex, but this is the basic premise for choosing fractional synthesis. However for certain application when a low fixed value of *N* is used (i.e. as is often the case for a 2nd LO) an integer PLL could remain the PLL of choice.

Review of PLL Theory

A RF-Microwave PLL is a feedback loop that is defined by the following linear equations: Forward Gain, Open Loop Gain and Closed Loop Gain. This article is centered on modern integrated PLLs that use current source-sink charge pumps. The circuit takes the VCO's output and divides it down by an *N* counter. The reduced frequency is then applied to the negative input of a phase detector. Here it is compared to that of a stable reference clock, whose signal is applied to the positive input of the phase detector. The phase detector acts as a summing circuit and produces a difference that is proportional to the difference between the divided down VCO frequency and reference clock. This phase error drives a charge pump which sources or sinks a difference current to a lowpass filter. The Lowpass filter charges up to a new DC voltage, retuning the VCO. This retuning continues until phase lock is achieved. Once the loop is locked the charge pump is in a high impedance state. The terms used in the loops transfer function are defined as follows. $K\Phi$ represents the phase detector with units in mA/radian. F(s) is the lowpass (loop) filter; the filter design can range from 2nd to 5th order, depending on the spur rejection required. Theoretically each additional pole provides extra 6 dB/octave of spurious attenuation. *Kv* is the VCO's tuning

Fractional PLL(Noise Floor) dBc / Hz	Integer PLL(Noise Floor) dBc / Hz
–219 (ADF4150)	**–219** (ADF4108)
–216 (LMX2487E)	**–219** (LMX2434)

Table 1 · Comparison of the noise floor for extremely low noise PLLs.

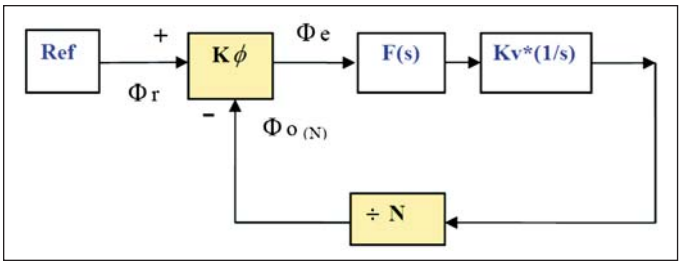


Figure 1 · The PLL block diagram used to derive equations 1-3 and circuit description.

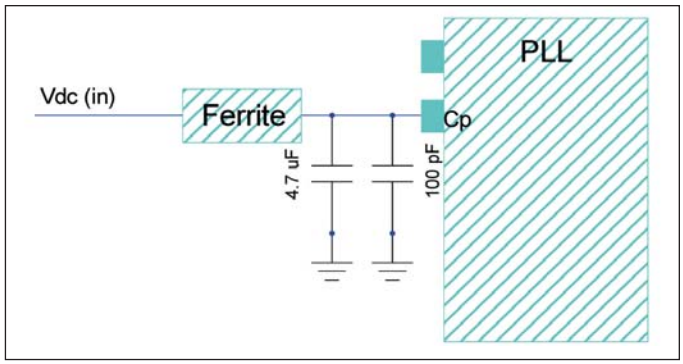


Figure 2 · Recommended circuit for spurious suppression on PLL's charge pump input.

gain in MHz/volt. 1/*s* is a Laplace term needed for the loop to operate in the phase domain. *N* is the value of the *N* divider.

$$\text{Forward Gain} = K\Phi * F(s) * Kv * 1/s \quad (1)$$

Equation 1) is the forward transfer function, without feedback.

$$\text{Open Loop Gain} = \left(K\Phi * F(s) * Kv * 1/s\right)/N \quad (2)$$

Equation 2) characterizes the Loops when it is not at equilibrium. This is used to evaluate lock time and loop stability.

$$\text{Closed Loop Gain} = \frac{K\Phi * F(s) * Kv * 1/s}{K\Phi * F(s) * Kv/s * N} \quad (3)$$

$$= \frac{\text{Forward Gain}}{1 + \text{Open Loop Gain}}$$

Equation (3) characterizes the loop it is phase locked. This function is responsible for shaping the PLL's inband phase noise and spurs. Detail on how these transfer functions affect the PLL in the way they do is beyond the scope of this article and can be found in *Deansbook* v4 [1].

External Noise Reduction

Voltages should be applied though a wideband ferrite surface mount part (see Figures 2 and 3). It's recommended that the ferrite filter's other end be directly connected to the junction of two capacitors. A capacitor is required whose value can range between (100 to 10 min.) µF, preferably on the higher side if possible. This capacitor should have very low ESR <2Ω down to 100 Hz. These values and ESR are recommended to filter noise down to low base-band frequencies. A capacitor of approximately 100 pF should be placed in shunt with the larger capacitor for high frequency suppression. The value of this capacitor can be altered if a particular high frequency spur (typically AM) requires attention. Both capacitors must be provided with a direct ground to avoid ground loops (floating grounds). Floating ground can allow spurious outputs to develop. The capacitors' ungrounded ends must terminate extremely close to the device input pin or pin pair (pin groupings). Insure the maximum voltage rating for the capacitors exceeds the applied voltages. The above guidelines provide for EMI, ripple and noise rejec-

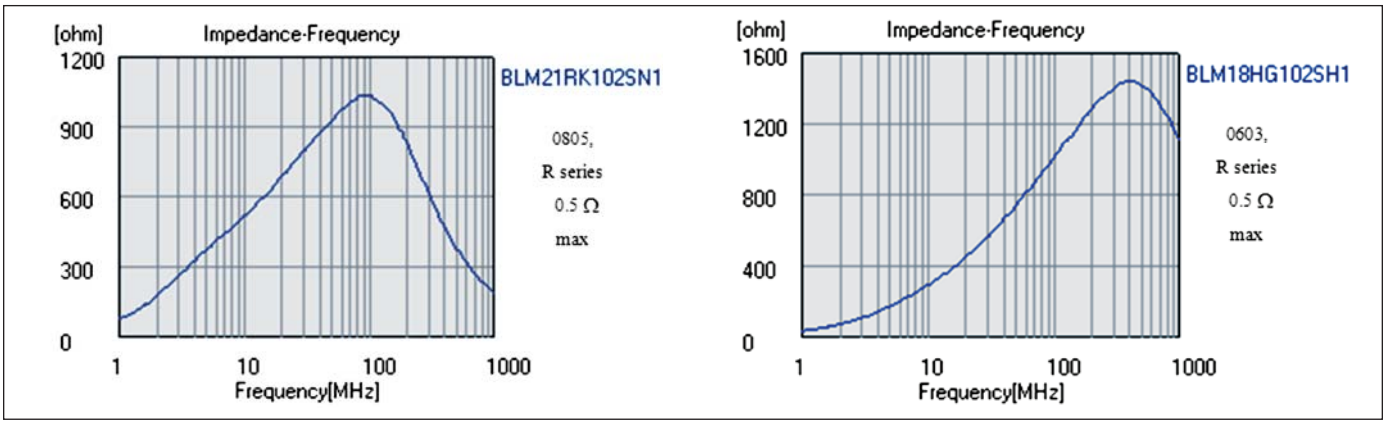


Figure 3 · Wideband impedance vs. frequency for different Murata ferrite products that are well suited for PLL noise suppression.

tion. It is recommended that these techniques be used on all PLL, clock, VCO and op-amp input power pins (pin-groupings) independently.

A low noise voltage regulator is important for low noise in the PLLs, with another used for the VCO. The regulator may require having the surrounded capacitors adjusted for low noise operation, although this may impede startup time in some application. The designer will have to determine a balance. It's recommended the regulator have good ripple rejection to prevent AM noise from appearing on the PLL's output. These spurs will occur at frequencies that are related to periodic noise and/or ripple that enters the PLL or VCO on an input power supply. These spurs can also show up on the output spectrum due to bad layout and-or poor grounding. If possible use low distortion capacitors in the loop filter. This will help prevent piezoelectric affects from causing sudden short term frequency "hits" (sudden changes or instabilities) in the PLL's output. These are film capacitors, available in values up to at least 4.7 µF.

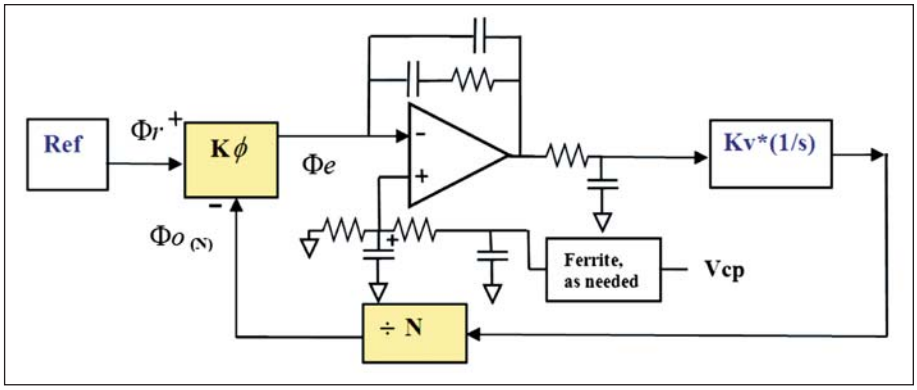


Figure 4 · Basic PLL with active 3rd order loop filter and *Vcp*/2 noise suppression circuit.

Active Loop Filters

Higher voltages than the charge pump can supply are required to cover frequency ranges for some ultra low noise or wideband VCOs: (Vcp – 0.3 Vdc) ≤ $Vtune$. This requires an active loop filter, which uses an op-amp. Here the PLL's charge pump drives the op-amps and performs a current to voltage transformation. The change pump drives the inverting input of an op-amp. The op-amp output is low impedance. The noninverting input is set equal to Vcp/2, to reduce spurs [1]. The ferrite shown in Figure 4 may not be needed due to the high value resistors used in the voltage divider. A ≥1 µF capacitor can be placed at the resistors' junction. This filters the resistors KTM noise at the op-amp input. A loop filter is designed, surrounding the op-amp. The loop filter should consist of a larger value capacitor with a capacitor and resistor in series, if possible. These capacitors are critical to filter noise. Other topologies can result in greatly increased phase noise. If an additional one or two poles are required after the op-amp for spurious rejection, then attempt to reduce the series resistors to further reduce noise. If the series resistor(s) are ajusted downward to reduce noise, the shunt capacitor(s) values need to be increased so the open loop phase margin stays within 45° ± 5° at 0 dB gain at the desired filter crossover frequency, Fc. This usually results in ≈ 3 dB of peaking in phase noise at Loop filter crossover frequency Fc. The phase margin can be extended past 70° in order to reduce the peaking at Fc to improve phase noise, with a slight penalty in lock time. Resistor noise adds to the VCO noise profile as well, but to a lesser extent. The basic formula for resistor noise is

$$V_n = \sqrt{4kTR}$$

Although it should be noted that loop filter design vs. the specific noise contributions of each resistor is beyond the scope of this article, for further derivations see [1]. The guideline provided will result in reduced resistor noise when designing for an active loop filter. The op-amp selection is important for low noise. Several criteria are critical: $e_{(n)}$ is the total voltage noise contributions from the op-amp, $I_{(n)}$ is the input referred current noise and low input bias current. It can be helpful if the op-amp operates from a single power supply. One good choice is the OPA211 from Texas Instruments with a noise voltage of

$$1.1\ nV/\sqrt{Hz}$$

and an input referred noise current of

$$1.7\ pA/\sqrt{Hz}$$

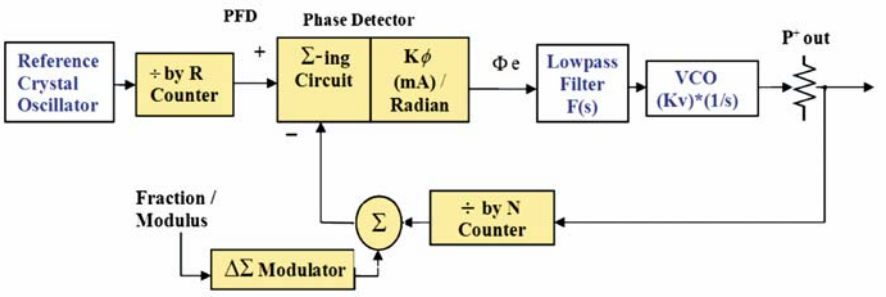
The OPA211 can be run single supply up to 36 Vdc. Another extremely low noise op-amp is the ADA4899 from Analog devices with noise voltage of

$$1\ nV/\sqrt{Hz}$$

and an input referred current noise of

$$2.6\ pA/\sqrt{Hz}$$

The ADA4899 runs up to 12 Vdc. It's also important to try and use high quality, low distortion capacitors any loop filter design. The catch is that higher voltages result in physically larger capacitor for a given value.



Formulas Used to Determine the Frequency for Fractional PLLs:

Relationship of PFD: (Reference-Clock) / R = PFD (Phase Frequency detector) (4)

Modulus * (Δ Frequency) = PFD (5)

RF(Carrier) = PFD [N + (Fraction / Modulus)] (6)

Example: 2.121 GHz, ΔFrequency = 75 kHz, Ref = PFD =14.925 MHz, Modulus, 199

2.121 GHz = 14.925 MHz [N + (Frac / 199)]

2.121 GHz / 14.925 MHz = 142 = ÷ N

Remainder = 0.110552764 = Frac / 199

Fraction Numerator = 22

Figure 5 · Basic topology for delta sigma modulator fractional synthesizer.

One trick is to reduce *Icp*. This results in lower values for the loop filter capacitors, while maintaining the same loop bandwidth and cutoff frequency. As described in the next section, the delta sigma fractional PLLs must reduce *Icp* to implement Cycle Slip reduction (a speedup feature).

Delta Sigma Fractional Synthesizers

The current state of the art for low cost, reduced current, high performance PLLs lies with the fractional synthesizer with delta sigma (ΔΣ) modulators (see Figure 5). The actual circuitry inside the modulators is vendor specific and propriety. These PLLs contain built-in fastlock and cycle slip reduction circuitry that is straightforward to implement, reducing the amount of programming. Fully digital 3rd and 4th order delta sigma modulators are used to reduce phase noise and fraction spurs. A 3rd order modulator could alternate between 8 different values to achieve the final fraction for a value = 50-1/3 (50.3333), i.e. 49, 50, 51, 52 [2]. The same 3rd order modulator will be summed 51 times for a fractional denominator of 51. For the case of 60-3/51 (60.0588) the modulator will be equal to 60 (48 times) +61 (3 times). This spreading out of the fraction digitally ditherers the phase noise and fractional spurs. This makes these devices performance superior to previous PLLs.

It's a bit more complex for devices such as the LMX248X series and the ADF4157. This is due to the fact that these PLL can handle extremely large fractions. The LMX series PLLs can contain a fractional denominator (modulus) up to 4,194,303 or 2^{22} –1. The ADF4157 PLL can contain a Modulus up to 3,355,4431 or 2^{25} –1. Since the basic relationship between the PFD and the modulus still holds true, these PLLs can be used to generate sub-Hz frequency changes. This allows the PLL to be directly modulated via the data input data in very tiny increments. In this manner a series baseband input can be used to directly modulate the PLL and create extremely smooth changes in phase and or frequency. This is due to the tiny increments between adjacent steps. Consider a 10 kHz frequency change accomplished using Hz or sub-Hz steps. In this way digital processing can convert input data (analog or digital) to a digital stream which modulates these newer delta sigma fraction PLLs to derive: phase modulation, analog FM or digital FM modulation. In the past extra complexity was required to accomplish similar modulation schemes, such as the using of DSS, modulating the VCXO in sync with the PLL. and other techniques.

Fractional spurs always occur at integer multiples related to the frequency spacing. For fundamental fractional spurs, the one that is equal to the frequency spacing itself is most problematic, since it is closer to the carrier and subject to less filtering. Depending on the modulus chosen, sub-fractional spurs can also be generated. These may be lower in magnitude in their dBc base level, however sub-fractional spurs often occur closer to the carrier, so they receive little filtering. Analog Devices uses 3rd order ΔΣ modulators for their ADF4153 to ADF4156 series PLLs. Analog Devices states a maximum fractional spur base level of –45 dBc worse possible case without filtering, not including integer boundary spurs (IBS). My experience has generally shown the fractional spurs produced by these devices to be somewhat lower. The ADF4157 produces no fractional spurs, except for IBS. National Semiconductors LMX248X series PLLs allow the user to select between either a 2nd, 3rd or 4th order ΔΣ modulator. The LMX series 3rd order is a trade off providing slightly more attenuation of sub-fractional spurs while sacrificing ≈10 dB of attenuation on the fundamental fractional spurs. The LMX series 4th order modulator provides a typical fractional spur base level of (–55 to

Condition (Dither off)	Qty of Sub-Fractional Spurs	Spur Interval
Modulus is Divisible by 2, not 3	1	Frequency Step/2
Modulus is Divisible by 3, not 2	2	Frequency Step/3
Modulus is Divisible by 6	5	Frequency Step/6
Modulus is Prime Number	0	Frequency Step

Table 2 · Relationship of subfractional spurs.

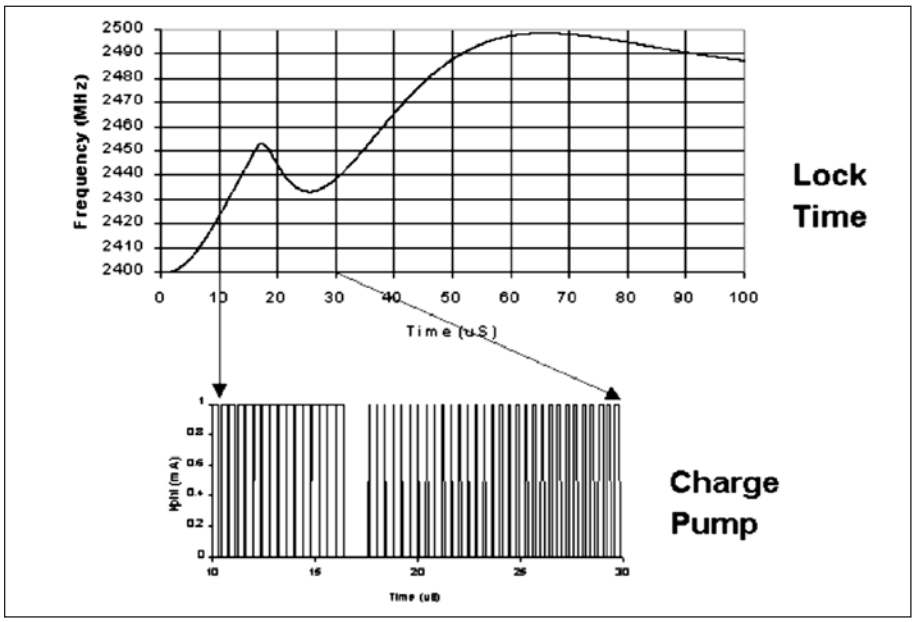


Figure 6 · A single cycle slip (top) and missing charge pump pulse needed to prevent the cycle slip (bottom). Courtesy of *Deansbook* v4.

–65) dBc for all fractions spurs, without filtering. See Table 2.

The fractional spurs that reach the highest magnitude are the IBS. IBS are typically (6 to 8) dB higher than the typical maximum fractional spurs occurring at the same offsets from the carrier. This spur occurs whenever the fractional numerator is equal to 1 or modulus–1. With the earlier example a relatively low value of *N* was used to achieve spacing frequency spacing equal to 50 kHz. However with frequency steps of 50 kHz the main fractional spurs will occur at 50 kHz. Since the modulus of 307 is non-divisible (a prime number), subfractional spurs won't occur. An appropriate loop filter must be designed to provide spurious attenuation. It's recommended that the loop bandwidth be 5 to 10 times lower than the frequency spacing in order to provide adequate spurious rejection. This is not to be confused with the fact that PFD/*Fc* should exceed 100 for the best attenuation of sigma-delta noise. However when the loop filter's *Fc* is low, it takes the PLL longer to achieve lock. Also, as the ratio between the PFD and *Fc* exceeds 100, cycle slipping begins. By the time this ratio exceeds 1000, cycle slipping is very significant. As the duty cycle for the charge pump exceeds 100 percent, regardless whether it's sinking or sourcing current, extra cycle(s) get in and reduce the tuning voltage. The PLL then has to play catch up and takes longer to lock. See Figure 6.

Fortunately many of these new PLLs have incorporated cycle slip reduction (CSR) circuitry to greatly reduce this issue. When using CSR you program the PLL for low charge pump current and set the CSR bit to automatically pull in the lock time. This is accomplished by an increase in charge pump current which effectively increases the loop bandwidth for an amount of time programmed into a set of registers for the LMX248X series PLLs. Once the counter times out, the PLLs automatically go into the normal mode of operation. The ADF4150, ADF4153 to ADF4157 series PLLs CSR circuit senses when the frequency is close to the final frequency and start reducing the charge pump current back to minimum without requiring a counter. The LMX248X series PLLs and the ADF4150 all contain separate fastlock and mux output pins. This allows for the use of an active loop filter while maintaining a separate output to verify the status of the PLL. The mux output can be used, depending on how the PLLs programmed to verify the *R* divider, the *N* divider or as a PLL lock indicator, amongst other things. Here the amount of time the fast lock pin is held low is controlled by a register. Once this register times out the pin goes to a high impedance state and the charge pump current, which was increased during fast lock, is auto-

National Semiconductor's Formula for Flat Phase Noise Region.

Phase-Noise for LMX-series PLLs =

$$-216 + 20 \log (N) + 10 \text{ Log (PFD)} + 10\text{Log} (1 + Kpd \cdot Knee/Kpd) \quad (7)$$

N = Divider value "*N*"

PFD = Phase detector frequency in Hz

Kpd·Knee = is equal to a constant for the "LMX245X series" 380 µA

Kpd = Charge Pump gain (same units as *Kpd·Knee*), can range from (1520 to 95) µA

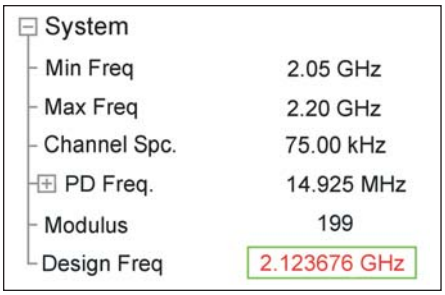


Figure 7 · PLL specifications.

matically set to the steady state value, which is held in another register.

Example of Fractional PLL Design Using ADIpllSIM software

For this example, the PLL design was modeled using the ADF4156 PLL IC from Analog Devices, a low noise custom VCO, and a low noise TCXO model from Greenway. Basic design specifications are shown in Figure 7.

R-set is a resistor that's used to establish the range of *Icp*. The value used for R-set was 10 kΩ. Increasing R-set from 5.1 kΩ to 10 kΩ, results in a halving of maximum charge pump current (*Icp*). If we use the lowest possible Icp this reduces the values of the capacitors for the loop filter. *Note:* the ADI devices do not show phase noise dependence on *Icp*. This helps when space requirements are tight. The 3rd order loop filter was tweaked for noise reduction. *Fc* = 11 kHz, *N* =142 and the fraction was varied to show worse case typical and IBS fractional spurs. The simulation results are shown in Figures 8-11. Since *Fc* is equal to 11 kHz, the loop filter (Figure 12) provides >>20 dB/decade of attention to spurs. The fact that (14.925/0.011) MHz = 1361.4 results in >136 decades of frequency spacing between the PFD and *Fc* and speaks for itself. The reference spurs will fall below the noise floor.

The phase noise at 10 kHz offset is –91.5 dBc Hz, at 20 kHz offset its –98 dBc/Hz. The 3rd order 11 kHz loop filter provides excellent spurious suppression. The fundamental fractional spur is attenuated by >27 dB and is has a level approx. –72.1 dBc. The IBS receives the same attenuation, but was modeled to be 8 dB higher, a realistic worse case scenario. Despite tweaking for low noise the phase margin at *Fc* is maintained. The improvement in frequency acquisition (locktime) is seen in the frequency error vs. time graph. The PLL is locked at ≈350 µs. CSR results in ≈3 times faster frequency acquisition from F_{min} to F_{max}. Locktime could be improved by decreasing the PFD, at the expense of phase noise. Note: Every halving of the PFD adds 3 dB noise. Also as the PFD to *Fc* ratio <<100 additional ΔΣ modulator noise can appear. Increasing *Fc* will also speed up locktime at the expense of spurs and phase noise for low noise VCOs.

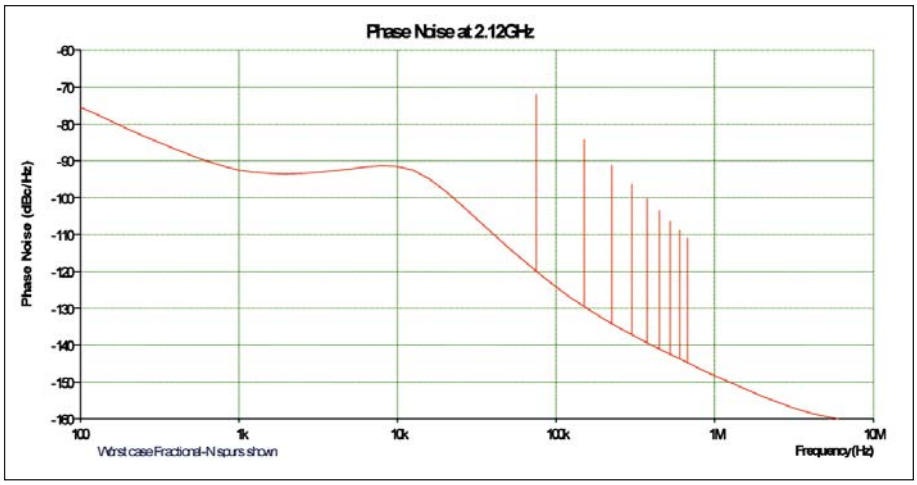


Figure 8 · Plot of PLL phase noise and worse case fractional spurs (non-IBS), frac/mod = 54/199.

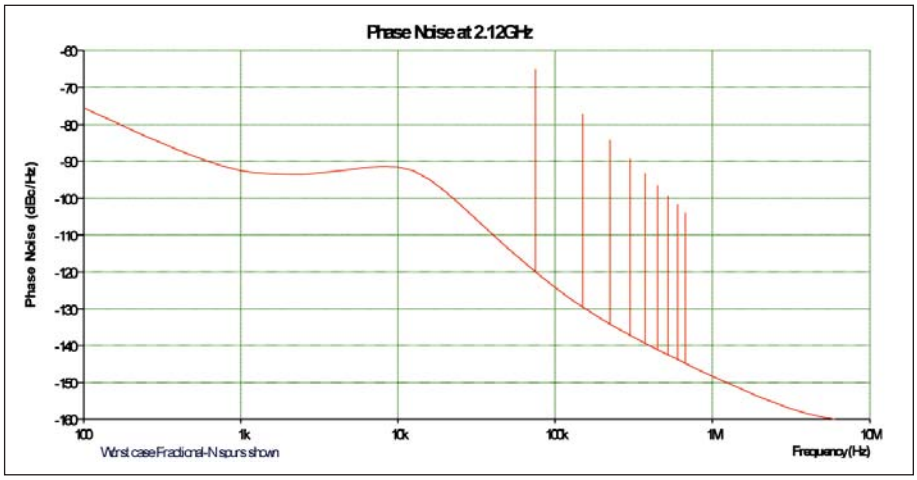


Figure 9 · Plot of PLL phase noise and worse case IBS, frac/mod = 1/199.

Measured Results of ADF4156 PLL

An ADF4156 evaluation board was used for the purpose of measuring the phase noise, the circuit was setup identical to that of the above simulation. The evaluations board's crystal oscillator and VCO were replaced with low noise devices. The circuit was battery powered to eliminate noise. The measured data was taken at 2.12382 GHz, which is equal to

$$\left(\sqrt{FL * Fh}\right)$$

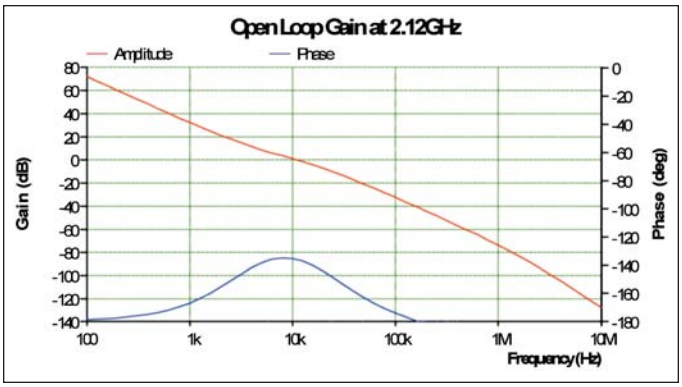


Figure 10 · Phase margin is 44.5 degrees, magnitude 0 dB at 11 kHz.

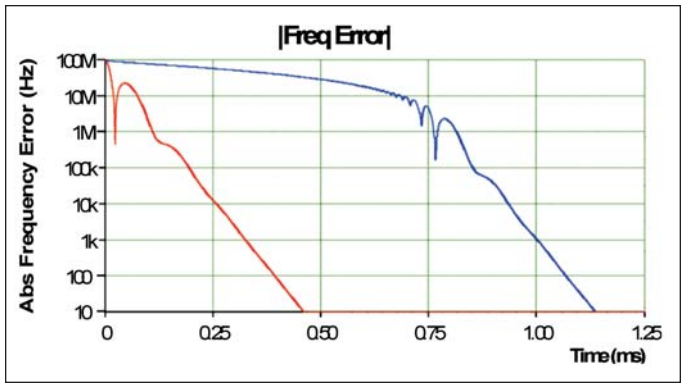


Figure 11 · Frequency Error: Red is with CSR enabled, Blue is without CSR.

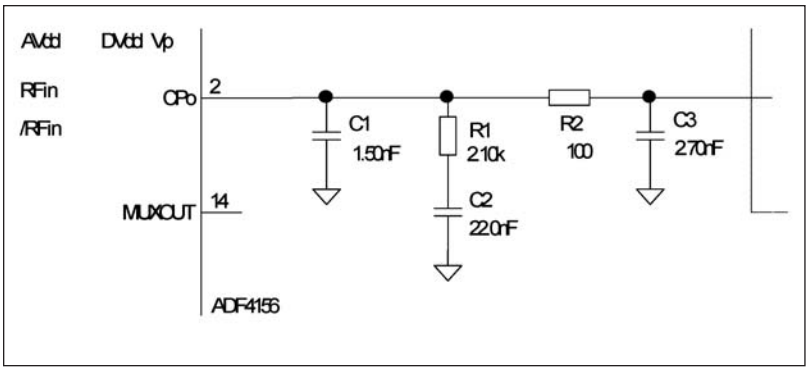


Figure12 · Loop filter design.

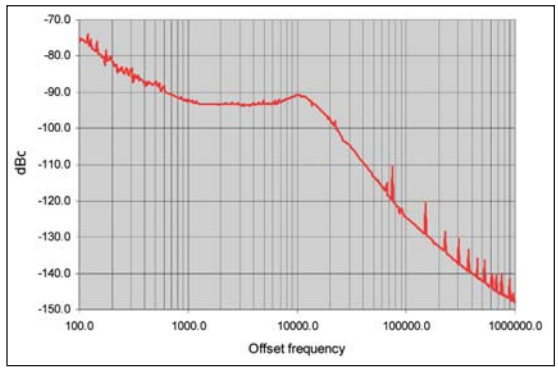


Figure 13 · Measured Phase Noise data, dBc/Hz for ADF4156 PLL.

As shown in Figure 13, the phase noise at 10 kHz offset is –90.8 dBc Hz; at 20 kHz offset its –98 dBc/Hz. The fraction spurs are displayed on the plot and appear very low. However phase noise measurements cannot be used to measure the magnitude of spurs (although this is generally a good sign). The PLL displayed similar phase noise and power out at each band edge. Both main fractional and IBS were found to be lower than worse case simulated spurs. The magnitude for the highest main fractional spur was –86.1 dBc, which is ≈ 6dB lower than that of the simulation. The fractional spurs could be attenuated further by adjusting the phase value on the PLL for each frequency. You can sweep the input phase word, while monitoring the fractional spurs (including the IBS) until maximum attenuation occurs.

Fractional Spurs

Offset	Description	Roll-Off	Worst Case Numerator	Worst Case Spur	Spur for this Numerator
75.0000	1st Fractional Spur	-26.5	1	-81.5	-81.5
150.0000	2nd Fractional Spur	-38.6	2	-93.6	-99.6
225.0000	3rd Fractional Spur	-45.8	3	-100.8	-110.3
300.0000	4th Fractional Spur	-50.9	4	-105.9	-118.0
375.0000	5th Fractional Spur	-55.0	5	-110.0	-124.0

Integer Spurs

Spur Offset (kHz)	Description	Spur Gain (dB)	Leakage Component (dBc)	Pulse Component (dBc)	Spur Level (dB
14925.000	1st Integer Spur	-99.0	-193.5	-144.0	-144.0
29850.000	2nd Integer Spur	-117.0	-211.5	-155.0	-155.0
44775.000	3rd Integer Spur	-127.6	-222.1	-163.5	-163.5
59700.000	4th Integer Spur	-135.1	-229.6	-171.0	-171.0
74625.000	5th Integer Spur	-140.9	-235.4	-178.0	-178.0

Charge Pump Leakage	1	nA
Base Pulse Spur	-332	dB
Fractional Modulus	199	
Fractional Numerator	1	
Number of Spurs to display	5	

Figure 14 · Worse case spurs.

Example of ΔΣ Fractional PLL using WEBENCH PLL DESIGNER

This example PLL design was modeled using the LMX2485 PLL IC from National Semiconductor, using the same VCO phase noise profile. Figures 14-15 summarize the design and predicted performance. The upper tuning range is reduced to 2.2 GHz, since the maximum charge pump voltage was lower, 3.3 Vdc. 380 µA is selected for the charge pump current. This results in a 3 dB increase in inband phase noise

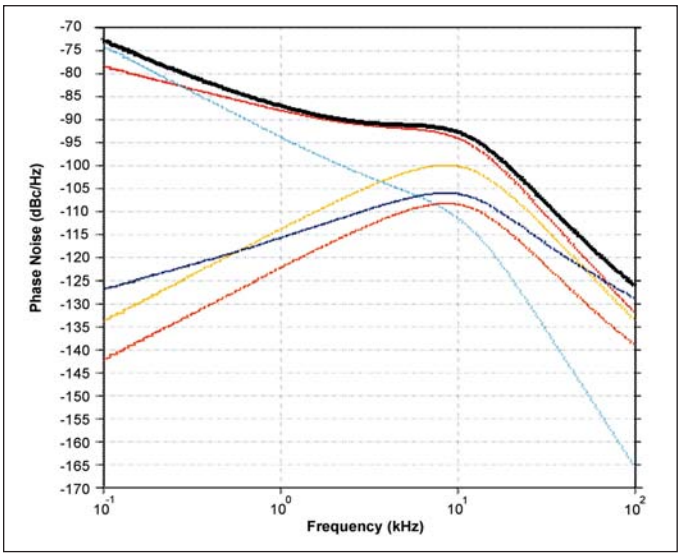


Figure 15 · Plot of the PLL's phase noise in black.

Name	Ideal Value	Std Value
C1	6.8 nF	2.3 nF
C2	43.0 nF	54.0 nF
C3	1.6 nF	7.2 nF
R2	750.0 Ohm	750.0 Ohm
R3	2.7 Kohm	100.0 Ohm

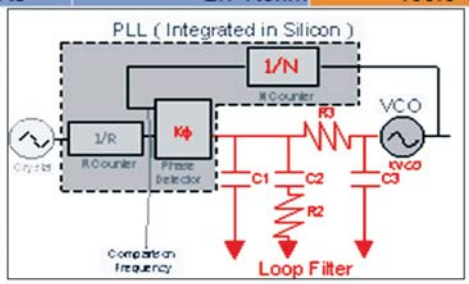


Figure 16 · Loop filter design used Std Value for lower noise.

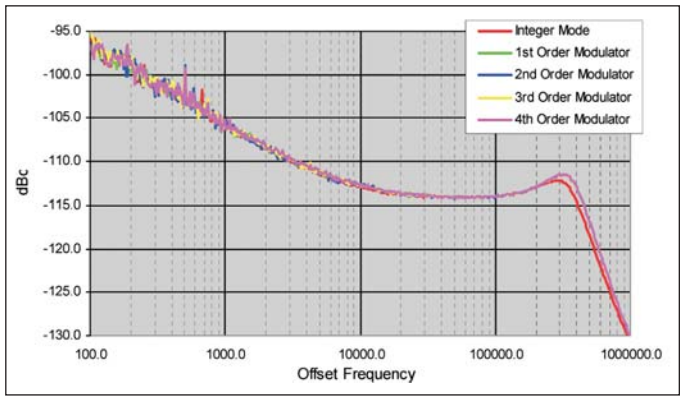


Figure 17 · Measured wideband phase noise data taken at 2.1 GHz for the LM2541 PLL. The plot overlays four different ΔΣ modulator settings.

(eq. 7); but lets the charge pump current quadruple when CSR is enabled for fastlock time. For the LMX series PLLs, reducing *Icp* can increase CSR time up to a factor of 16 times, if there's enough cycle slipping to warrant being pulled in that quickly. *Fc* = 11 kHz with a phase margin of 45 degrees.

The phase noise from at 10 kHz offset the phase noise is –86 dBc; at 20 kHz it's –97 dBc. The fundamental fractional spur is attenuated by >26.1 dB and has level approx. –81.5 dBc. The program has flexibility by allowing the users to tweak T3/T1, change the loop and optimizing for locktime vs. spur gain. The loop filter was optimized to reduced in-band phase noise, at the expense of a few dB less spur suppression.

Measured Results of LM2541 PLL

The LM2541 PLL-VCO is a new, ultra low noise PLL with a noise floor of –223 dBc/Hz in the fractional mode. This device can be used with either an integrated or external VCO. Figure 16 shows the result of a PLL arrangement setup for the purpose of determining the device's low in-band phase noise. The phase noise results (Figure 17) remain virtually unchanged, regardless of which ΔΣ modulator is selected. It contains all the other features of the LMX248-series PLLs. Test conditions: The PFD = 100 MHz, *N* = 21, Frac/Modulus = 0 /400, *Icp* = 3.2 mA, *Fc* ≈ 350 kHz. The PLL uses a 4th order loop filter, which was not tweaked for noise. Although the fraction is 0 the device is operating in the fractional mode. However with a fraction of 0 the PLL should produce no fractional spurs. The measured data was taken at 2.1 GHz. The phase noise at 10 kHz offset is –112.9 dBc/Hz; at 70 kHz offset it's –114.3 dBc/Hz, at 200 kHz offset its –112 dBc/Hz.

Note: the datasheet for the LMX2541 currently does not contain fractional phase noise plots. To date, this is the only published data of the LMX2541 being used in the fraction mode. The degradation is very minor from that of the integer mode, which is favorable for the PLL. Once all the on-board VCO and associated circuits are disabled, the PLL draws about 70+ mA with an external VCO.

Conclusion

Design details and low noise techniques have been provided for modern PLL ICs. Practical information detailing many of todays fractional PLLs using modulators has been provided. Two separate simulations were performed using software from two different sources, a design example was included, and data for a newly released very low noise PLL was presented. It is hoped that these methods and insights will assist other designers seeking low noise performance.

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Author Information

Jim Carlini is a self-taught RF-Microwave Engineer with 15 years of R&D and production experience. Jim has designed a wide range of RF and microwave circuitry for both military and low cost commercial markets. Jim's circuit designs have ranged in frequency from 19 MHz to 11 GHz, (with filter designs extending to >31 GHz). Many of his designs were receiver-exciter related, including discretely built PLLs, oscillators, LNAs and down-convertors, as well as the control circuit needed to run the RF circuitry and interface them with baseband. He has also designed a wide variety of planar circuitry including couplers, summing and power distribution networks, as well as antennas.

Jim has served as a Teaching Adjutant for the graduate EM lab at the Rochester Institute of Technology, and has done design, analysis and troubleshooting work for Bosch, RIT, Cybernet Systems and Harris RF Communications. He can be reached at jimcarlini@gmail.com