Anritsu Company introduces three new options for its models MP1763C and MP1764C/D 12.5G Bit Error Rate Test Set (BERTS) that accurately evaluate new high speed devices used in storage area network (SAN) and 10 Gigabit Ethernet applications. With these options, Anritsu now offers the only 12.5G BERTS with the differential inputs, 1/4-speed differential outputs, and CDR (Clock/Data Recovery) required for evaluating 4.25G Fibre Channel as well as 10 GbE XAUI and SFI-4P2 devices. The options also solidify the number one position of the Anritsu 12.5G BERTS in the marketplace.

Quarter-Speed Differential Output

The new 1/4-speed differential option enables differential output of both data and clock at a rate one-quarter that of the standard 50M to 12.5G output. This allows the 12.5G BERTS to analyze new high-speed devices used in 10G Ethernet, as well as high-speed buses and backplanes such as PCI Express, much less expensively than a using a parallel BERTS. With its new CDR option, the 12.5G BERTS can use input data as a trigger signal for error rate detection and waveform monitoring. An external clock or CDR is not required, and when the CDR option is used jointly with the new differential input option, high-speed differential devices can be evaluated without an external jig. The CDR is variable and supports bit rates from 62.5M to 11.1G, including unique support for 4.25G Fibre Channel.

The core Anritsu 12.5G BERTS consists of the MP1763C Pulse Pattern Generator (PPG) and MP1764C/D Error Detector (ED). Covering the wide range of 50M to 12.5G, the BERTS support STM-0/STS-1 to 10 GbE, STM-64/STS-192, and OTU-2, in addition to 4.25G Fibre Channel.

Anritsu offers significant new options for its 12.5G Bit Error Rate Testers.

Anritsu Company
Tel: 800-ANRITSU (800-267-4878)
www.us.anritsu.com
HFeLink 302