From October 2006 *High Frequency Electronics*

Minimization of DDS Spurious Content in Multi-Channel Systems

By Ryan Groulx and Shawn Mason
Rockwell Collins

This article reviews the mechanisms that result in the generation of spurs in DDS systems, and shows how to select the best clock frequency to minimize those spurs.

Implementing a Direct Digital Synthesizer (DDS) IC in a new design can be a daunting task. Many times, the DDS is looked upon as a "noise generator" and the unfortunate designer is left to deal with whatever output spectrum the DDS presents after the basic design is complete. The DDS is in a unique class of ICs that joins the once separate worlds of digital and RF circuit design. Despite these challenges, the designer can predict the output spectrum of the DDS with a high degree of accuracy with the knowledge of several basic concepts.

Two topics will be covered. The first topic will be an analysis that can be completed by the designer to predict the spurious signals that result from harmonic remapping in the DDS given a predefined DDS clock and output frequency. The ideal DDS clock choice for a given output frequency will also be discussed.

The second topic will build on the first by examining a channelized frequency source where a DDS would more likely be used. A sample design and algorithm will be stepped through to show how an optimal DDS clock frequency can be chosen based on designated output channel frequencies, local oscillator (LO) choice, and filtering.

Output Spurs Due to Harmonic Remapping

One of the most prominent sources of spurs in the output spectrum of a DDS is due to harmonic remapping. These spurs are essentially the harmonics of the desired DDS output that get "transplanted" back into the 1st Nyquist zone, which extends from 0 Hz to half of the DDS clock frequency.

The first step in calculating the spurious output spectrum due to harmonic remapping is to create a list of harmonics of the desired output frequency. It is usually best to calculate out as many harmonics as possible, the more the better.

The next step is to calculate which Nyquist zone each of the harmonics falls into. The Nyquist zones span integer multiples of the Nyquist frequency. The Nyquist frequency is equal to 1/2 of the clock frequency, and therefore each Nyquist zone starts or stops at an integer multiple of the Nyquist frequency. The first Nyquist zone would extend from 0 Hz to 1/2 of the clock frequency. The second Nyquist zone would extend from 1/2 the clock frequency to the clock frequency, and so on.

For a given output harmonic, the Nyquist zone into which it falls may be calculated as:

$$Zone = ceil\left(\frac{F_{Harm}}{F_{Nyquist}}\right) \quad (1)$$

where:

F_{Harm} = harmonic frequency.
$Zone$ = Nyquist zone into which $F_{harmonic}$ falls
$F_{Nyquist}$ = Nyquist frequency ($F_{CLK}/2$)
$Ceil$ = ceiling function. This function rounds to the next higher integer toward positive infinity.

The remapping of the harmonic frequency depends on if the harmonic falls within an even or odd numbered Nyquist zone. The

Algorithm for Predicting Output Spurs

1. Create a list of "N" harmonic frequencies of the desired DDS output frequency, F_{Out}:

   $F_{Harm} = n \cdot F_{Out}$, where n is an integer ranging from 1 to N.

2. For each harmonic frequency, calculate the Nyquist Zone into which it falls:

   $$Zone = ceil\left(\frac{F_{Harm}}{F_{Nyquist}}\right)$$

3. If the harmonic lies in an *odd* Nyquist Zone (i.e., Zone 1, 3, 5, 7 ...) then calculate the remapped harmonic frequency as follows:

   $$F_{remap} = F_{Harm} - floor\left(\frac{Zone}{2}\right) \cdot F_{Clk}$$

   OR, if the harmonic lies in an *even* Nyquist Zone (i.e., Zone 2, 4, 6, 8 ...) then calculate the remapped harmonic frequency as follows:

   $$F_{remap} = \frac{Zone}{2} \cdot F_{Clk} - F_{Harm}$$

Figure 1 · Harmonic remapping algorithm.

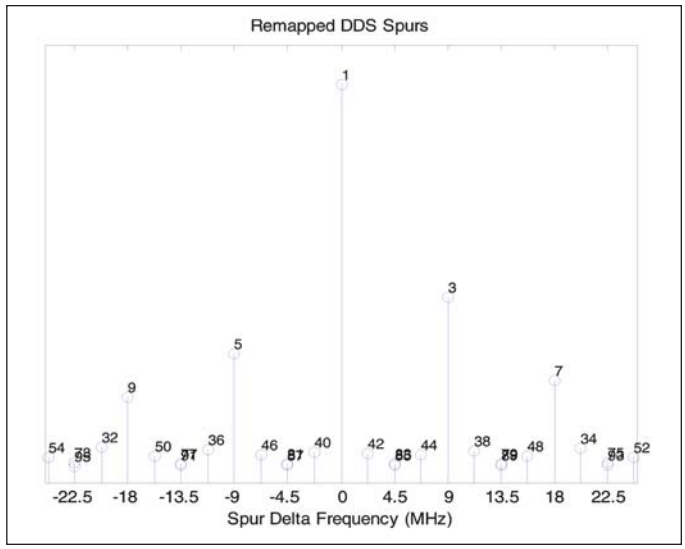

Figure 2 · Simulated results for 99.25 MHz spectrum.

remapped frequency may be calculated as follows:

If the harmonic falls within an *even* numbered Nyquist zone:

$$F_{remap} = \frac{Zone}{2} \cdot F_{Clk} - F_{Harm} \quad (2)$$

If the harmonic falls within an *odd* numbered Nyquist zone:

$$F_{remap} = F_{Harm} - floor\left(\frac{Zone}{2}\right) \cdot F_{Clk} \quad (3)$$

where:

Floor = floor function. This function rounds to the next lower integer toward minus infinity.

It is very important to note that there are discrete locations that spurs can appear in the DDS output spectrum. These spur locations are located at integer multiples of the greatest common divisor between the DDS clock frequency and the desired output frequency, or:

$$\Delta_{spur} = \gcd\left(F_{Clk}, F_{Out}\right) \quad (4)$$

where:

Δ_{spur} = frequency spacing of spurs due to harmonic remapping
F_{Clk} = DDS clock frequency
F_{Out} = fundamental DDS output frequency
gcd = greatest common divisor function.

There is a unique case where no spurs will appear in the output spectrum. This occurs when the clock frequency is an integer multiple of the output frequency. When the clock is an integer multiple of the output, the result of Equation 4 (the spur spacing) is equal to the output frequency. Therefore, the output spectrum will contain only harmonics of the output frequency.

The amplitude of the spurs can not be accurately predicted due to the unique non-linearity's in the DDS output DACs, but it follows that the higher order harmonics will have a lower amplitude relative to the lower order harmonics.

Simulation

A simulation was run in MatLab using a DDS clock frequency of 378 MHz and a desired output of 92.25 MHz. Given this, it can be calculated that spurs could appear at 2.25 MHz intervals from the desired output frequency of 92.25 MHz. The simulation shown below is ignoring all spurs that fall outside of 92.25 MHz ±25 MHz. Also, the harmonics were calculated out to the 100th harmonic. The remapped frequencies that fall within ±25 MHz of 92.25 MHz are listed in Table 1. Figure 2 shows an approximation of the DDS output spectrum. The amplitudes are only approximations that are based on the order of the harmonic to which it is related.

Measurements

The AD9959 evaluation board was used in this test. The clock for the DDS was provided by a signal generator with the output set to 378 MHz at 0 dBm. The DDS output spectrum was captured on an Agilent E4440A spectrum analyzer, see Figure 3. The span of the analyzer was set to 50 MHz so that it equals the span seen in Figure 2.

Delta Frequency (MHz)	Harmonic #
–24.75	54
–22.5	73
–22.5	95
–20.25	32
–18	9
–15.75	50
–13.5	77
–13.5	91
–11.25	36
–9	5
–6.75	46
–4.5	81
–4.5	87
–2.25	40
0	1
2.25	42
4.5	83
4.5	85
6.75	44
9	3
11.25	38
13.5	79
13.5	89
15.75	48
18	7
20.25	34
22.5	75
22.5	93
24.75	52

Table 1 · List of spurious frequencies due to harmonic remapping, from the MatLab simulation.

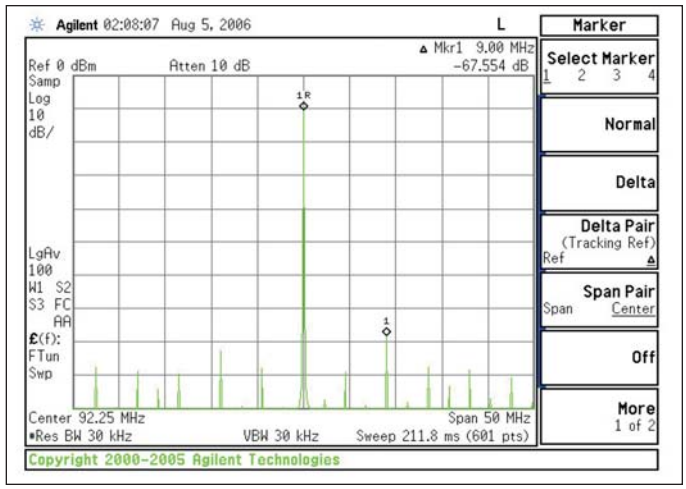

Figure 3 · 92.25 MHz spectrum analyzer measurement.

Frequency Offset (MHz)	Amplitude (dBm)	Source Harmonic #
–22.5	–87	73rd & 95th
–18	–86	9th
–13.5	–89	77th & 91st
–9	–82	5th
–4.5	–86	81st & 87th
4.5	–86	83rd & 85th
9	–75	3rd
13.5	–85	79th & 89th
18	–87	7th
22.5	–89	75th & 93rd

Table 2 · Measured spectrum results.

There are five major spurs (spurs above –90 dBm) visible on both sides of the carrier. Table 2 lists the spurs harmonic relationship to the carrier as well as approximate amplitude.

Choosing Best Clock for Multiple Output Frequencies

The previous method is sufficient as long as the designer is constrained to using a given clock and output frequency. However, the designer is often faced with a more difficult problem of having to choose a clock that minimizes spurious levels over several output frequencies, or channels. The choice of LO frequency and filtering bandwidth must also be taken into account. A more detailed algorithm is required to identify the best possible DDS clock frequency.

The "best" DDS clock frequency is one that produces the minimum amount of spurs on all desired output frequencies. The first step is for the designer to choose an appropriate DDS chip and identify the required output frequencies. After this is done, the maximum and minimum DDS clock frequencies may be identified. The maximum allowable DDS clock frequency is dictated by the DDS manufacturers data sheet, and the minimum DDS clock frequency should be greater than twice the highest desired output frequency. A good rule of thumb is keep the highest desired output frequency equal to at most 40% of the clock frequency, or:

$$F_{ClkMIN} \geq \frac{F_{Out}}{0.40} \tag{5}$$

Now that the minimum and maximum DDS clock frequencies are defined, the designer can now begin the process of choosing the best clock for their application. Obviously, there are an infinite number of possible clock frequencies within the DDS clock limits, but the designer can quickly reduce the possible clock frequencies by performing a simple algorithm.

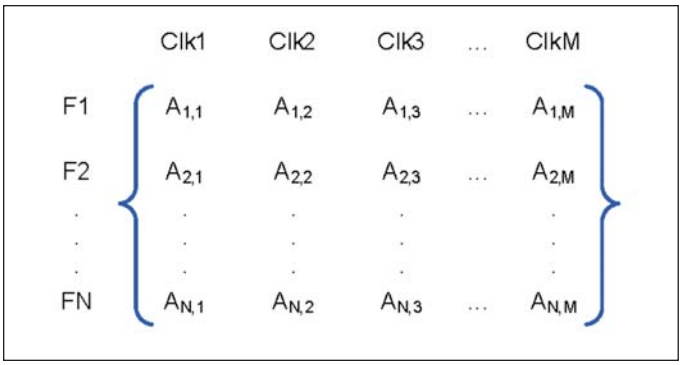

Figure 4 · Remapped harmonic matrices for all output and clock frequencies.

We know from Equation 4 that spurs can only exist at certain intervals from the fundamental and that the interval is equal to the greatest common divisor (GCD) of the fundamental and the clock. The largest possible interval for multiple output frequencies would be equal to the GCD of all of the output frequencies, and the only clock frequencies that can produce this spacing for all required output frequencies are ones that are evenly divisible by this spacing. Therefore, a list of clock frequencies can be made, starting at the minimum (as defined in Equation 5) stepping at intervals equal to the GCD of the output frequencies and ending at the maximum DDS clock frequency. An example is shown below:

Example: A DDS is chosen that has a maximum clock frequency of 400 MHz. Four output frequencies are desired: 120, 125, 130, and 140 MHz. The DDS minimum clock frequency should be no less than 350 MHz, as defined by Equation 5. The GCD of the output frequencies is 5 MHz. Therefore, the number of best case clock frequencies are now reduced to eleven: 350 to 400 MHz in steps of 5 MHz.

Therefore, in order to reduce the number of potential spurs in a given bandwidth for multiple output frequencies, the clock frequency should be chosen so that it is evenly divisible by the GCD of all of the output frequencies.

Now that the possible clock frequencies have been reduced significantly, the remaining frequencies can be "ranked" in terms of which ones produce the fewest and lowest amplitude spurs for all the desired output frequencies in a given bandwidth. This process is best implemented in software (e.g. MatLab, MathCad, Excel).

In order to rank each clock frequency, it is necessary to identify the factors that will influence the number and amplitude of the spurs in the output spectrum. There are three primary weighting factors that should be applied to all spurs in order to properly rank the clock frequency. These factors give a greater weight to less desirable spurs.

Spur Weighting Factors

1. Order of harmonic causing spur (lower order harmonics should be given greater weight than higher order harmonics)
2. Whether the spur comes from an *even* or *odd* harmonic (an odd order harmonic spur should be given greater weight than an even order harmonic spur)
3. The frequency difference of each spur from the desired output (spurs located closer to the fundamental should be given greater weight than spurs further away)

The remapping algorithm must be completed for each output frequency at every potential 'best-case' clock frequency. This will produce an $N \times M$ matrix as seen in Figure 4. Each of the items labeled "*A*" in the figure is a matrix resulting from the remapping algorithm performed on the clock and output frequencies. For simplicity, these sub-matrices should contain two rows, one for the remapped frequency and one for the order of the harmonic that produced it. The number of columns in these matrices will be equal to the maximum harmonic order that is set in the remapping algorithm (refer to Step 1 in Figure 1).

Each one of the sub-matrices can be reduced by eliminating any spurs that fall outside of a given bandwidth around the desired output frequency (i.e. spurs that may be filtered off easily by external filtering). This may also help to speed up the process for larger numbers of clock and output frequencies.

A weight should now be calculated for each sub-matrix "*A*." For each spur in each sub-matrix "*A*," the three weighting methods listed above should be applied. The three weights will be multiplied together to produce a net weight for each spur in each sub-matrix "*A*." Now all of the spurs' weights can be summed in each sub-matrix "*A*." This produces an individual weight for each sub-matrix "*A*." To get a net weight for each clock frequency (columns in Figure 4), the weights of all the matrices in a given column will be summed.

Now each clock frequency will have a weight, or rank, associated with it. These ranks can now be used to determine the best choice of clock frequency.

The entire weighting procedure for a given clock frequency can be defined as:

$$W_{CLKm} = \sum_{i=1}^{N}\left[\sum_{j=1}^{P}\left[\prod_{k=1}^{3}\left(W_k\left(Spur_j^{<A_{i,m}>}\right)\right)\right]\right] \qquad (6)$$

$$m = 1,2...M$$

where:

GCD (MHz) of Clock Frequency & Output Frequency						
Clock Freq. (MHz)	Score	130 MHz	135 MHz	140 MHz	145 MHz	150 MHz
490	2.4535	10	5	70	5	10
495	2.4899	5	45	5	5	15
450	2.5093	10	45	10	5	150
500	2.5145	10	5	20	5	50
480	2.5557	10	15	20	5	30
390	2.6225	130	15	10	5	30
420	2.8318	10	15	140	5	30
435	3.2841	5	15	5	145	15
405	3.7357	5	135	5	5	15
375	3.7621	5	15	5	5	75
465	3.8162	5	15	5	5	15
460	3.8634	10	5	20	5	10
475	3.8961	5	5	5	5	25
485	3.9530	5	5	5	5	5
470	4.0415	10	5	10	5	10
455	4.2389	65	5	35	5	5
380	4.7060	10	5	20	5	10
400	5.5705	10	5	20	5	50
440	5.8586	10	5	20	5	10
430	5.9504	10	5	10	5	10
410	6.1418	10	5	10	5	10
385	6.2909	5	5	35	5	5
445	6.2996	5	5	5	5	5
425	6.3264	5	5	5	5	25
395	6.6377	5	5	5	5	5
415	6.7361	5	5	5	5	5

Table 3 · Clock frequency results and scores.

$Spur_j^{<A_{i,m}>}$ = the j^{th} spur in sub-matrix $A_{i,m}$
$W_k(Spur_j^{<A_{i,m}>})$ = the k^{th} weighting factor applied to the j^{th} spur in sub-matrix $A_{i,m}$
P = number of spurs in sub-matrix $A_{i,m}$
N = number of desired output frequencies
W_{CLKm} = the weight of the m^{th} clock frequency
M = number of possible clock frequencies

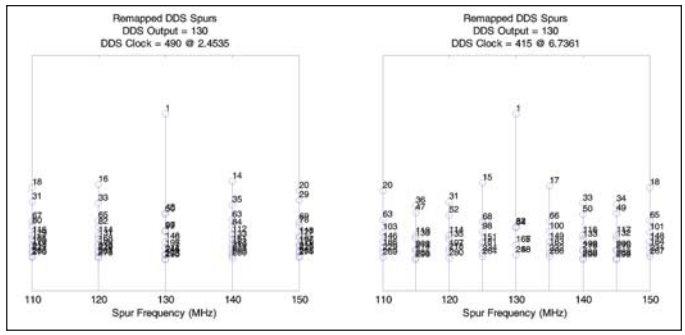

Figure 5 · 130 MHz simulated results—490 MHz (left) and 415 MHz (right) DDS clock.

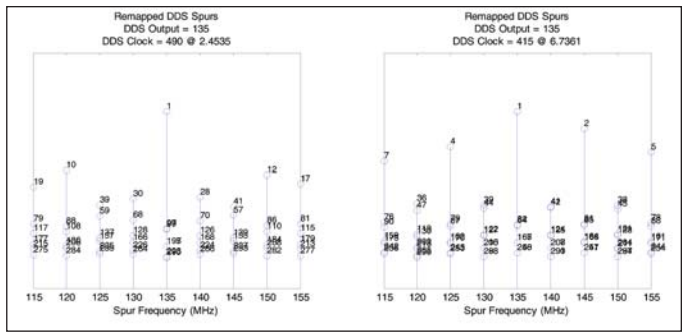

Figure 6 · 135 MHz simulated results—490 MHz (left) and 415 MHz (right) DDS clock.

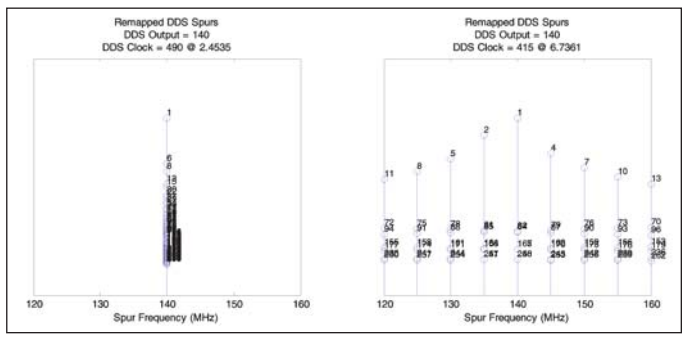

Figure 7 · 140 MHz simulated results—490 MHz (left) and 415 MHz (right) DDS clock.

Simulation

The simulation is based on an Analog Devices AD9959 DDS. The requirement is to have five output frequencies of 130, 135, 140, 145 and 150 MHz. External to the DDS will be a band-pass filter that is centered at 140 MHz. It is assumed that the filter will be of sufficient order and bandwidth to allow us to ignore any spurs that fall outside of a 20 MHz bandwidth (140 ±10 MHz).

The AD9959 has a maximum clock rate of 500 MHz. The minimum clock rate will be set to 375 MHz based on Equation 4. The GCD of the five output frequencies is 5 MHz. This allows us to create an array of 26 possible clock frequencies: 375, 380, 385 … 500 MHz.

The results of the simulation are listed in Table 3. The first column is the clock frequency. The second column is the score that was computed for that clock frequency based on the weighting factors set-up in MatLab. For this simulation, the lower the score, the better the clock frequency.

Figures 5 through 9 each show two plots of the five output frequencies. The plot on the left is the estimated spectrum resulting from the clock frequency with the lowest score (490 MHz with a score of 2.4535), and the plot on the right is using the clock frequency with the highest score (415 MHz with a score of 6.7361). The integer appearing at

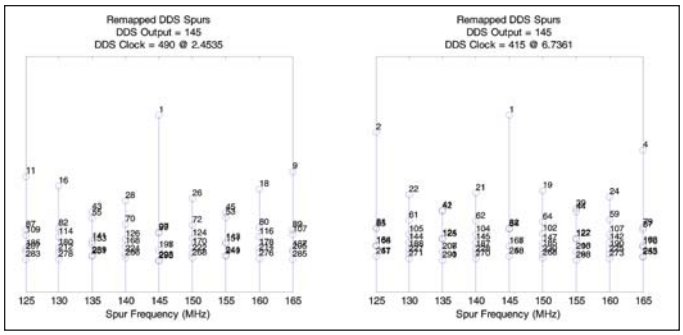

Figure 8 · 145 MHz simulated results—490 MHz (left) and 415 MHz (right) DDS clock.

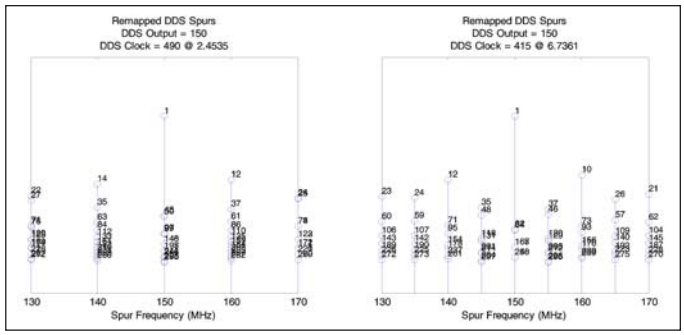

Figure 9 · 150 MHz simulated results—490 MHz (left) and 415 MHz (right) DDS clock.

the peak of the spur is the order of the harmonic that created it.

It should be noted that the amplitudes of the spurs in the following plots are not to scale. The amplitude was based on the order of the harmonic that created it, thus 2nd and 3rd order harmonic spurs have the highest amplitudes. The absolute amplitudes of the spurs are difficult to predict accurately.

Measurements

Figures 10 through 14 show the measured results. Each figure displays two versions of the spectrum of one of the output channels (130, 135, 140, 145 or 150 MHz). The spectrum plots on the left were produced using the clock frequency with the lowest (best) score which was 490 MHz. The spectrum plots on the right were produced using the clock frequency with the highest (worst) score, which was 415 MHz. It can be seen that the plots on the left are generally 'better' than those on the right with regards to number and amplitude of spurs.

Design Considerations

In a multi-channel system the use of the GCD method in the DDS clock selection algorithm ensures that all spurs will be the maximum distance from the center frequency and those that are present are the lowest possible. This should maximize the performance of IF filtering. However, spurs that are present will most likely be located at the center frequency of the off channels, which in the presence of other systems may result in IF interference. If this interference cannot be tolerated, an optimal clock frequency can be found by manually sweeping the clock to find the frequency that result in no low order (2nd through maybe 10th) harmonics in the passband of each of the channels.

Conclusion

The designer faces many challenges when implementing a DDS design. However, by understanding the origin of DDS spurs their effects can be minimized. The concept of harmonic remapping was introduced and analysis tech-

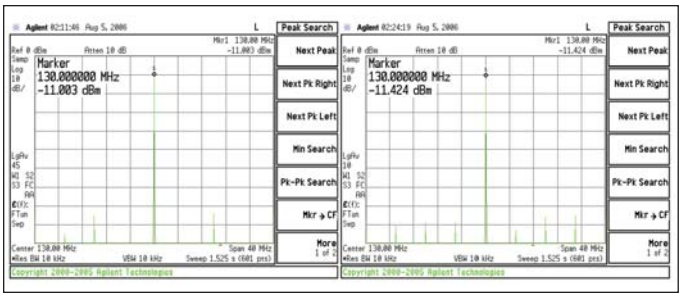

Figure 10 · 130 MHz output measured—490 MHz (left) and 415 MHz (right) DDS clock.

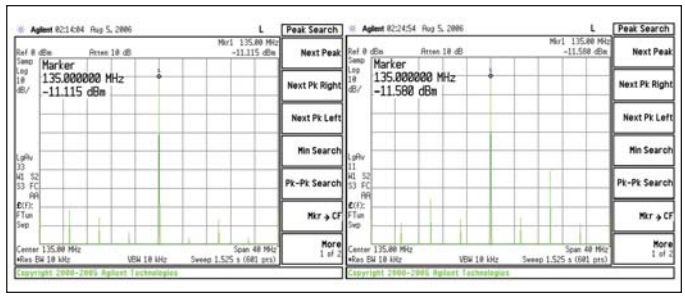

Figure 11 · 135 MHz output measured—490 MHz (left) and 415 MHz (right) DDS clock.

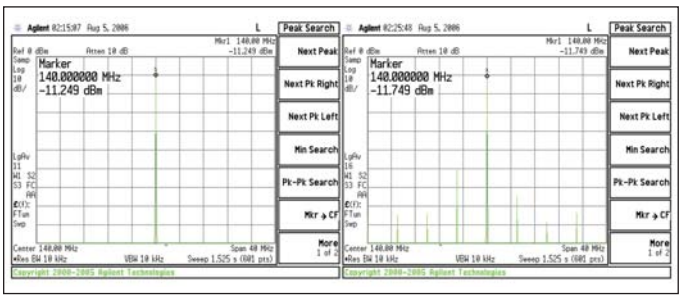

Figure 12 · 140 MHz output measured—490 MHz (left) and 415 MHz (right) DDS clock.

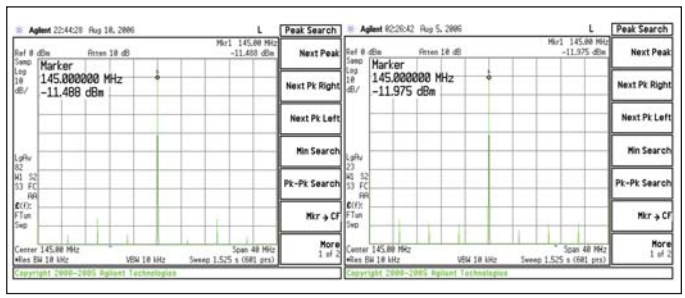

Figure 13 · 145 MHz output measured—490 MHz (left) and 415 MHz (right) DDS clock.

niques were demonstrated that allow the designer to accurately predict the harmonic content of the DDS output signal.

It was then shown how these analysis techniques could be extended to choose a clock frequency that minimizes the spurious content of several frequency outputs in a multi-channel system. After applying the harmonic remapping analysis to find the spurious content of each DDS clock/frequency output combination, a weighting function was applied to assign a relative score to the combination. By simply choosing the minimum sum of the scores for each DDS clock matrix column, the preferred clock frequency can be found. This process can easily be automated in several mathematical analysis tools. While several design considerations must be taken into account the designer has been provided with a powerful analysis tool to successfully complete a DDS implementation.

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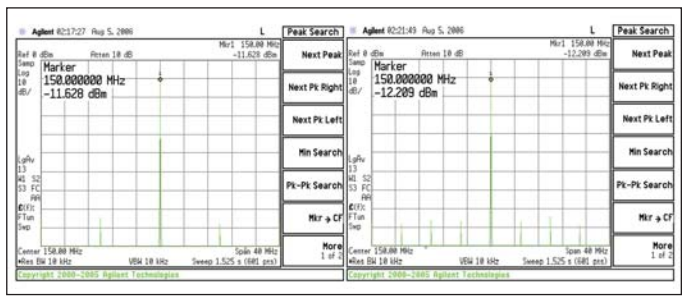

Figure 14 · 150 MHz output measured—490 MHz (left) and 415 MHz (right) DDS clock.

Author Information

Ryan Groulx received an A.S. degree in Avionics Technology from Embry-Riddle Aeronautical University in 1995a B.S.E.E. from University of South Florida in 1997 and a M.S.E.E. from Florida Institute of Technology in 2000. Ryan is a Senior Electrical Engineer at Rockwell Collins in the Weather Radar program. He can be reached by email at rcgroulx@rockwellcollins.com or by phone at 321-953-1757.

Shawn Mason received his B.S.E.E. from the Georgia Institute of Technology in 2002 and is pursuing his M.S.E.E at the Florida Institute of Technology. Shawn is an Electrical Engineer at Rockwell Collins in the Weather Radar program. He can be reached by email at smmason@rockwellcollins.com or by phone at 321-674-5389.