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Open RFIC Design Platform Integrates Highly-Capable Design Tools

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The newest version of this RFIC and high-speed analog IC design tool includes advanced features for design accuracy and user productivity

The Analog Office design suite is a powerful design system that is specifically architected and optimized from the ground up for next-generation analog and radio-frequency integrated circuit (RFIC) designs. Much more than a point tool, the Analog Office integrated solution boasts an industry-leading, concurrent interconnect-driven and RF-aware design methodology that delivers unprecedented ease-of-use, interactivity, and openness.

High-frequency circuit impairments in today's complex analog and RFICs, such as compression, noise, distortion, and phase noise, as well as the physical parasitics like interconnect impedance, coupling and packaging effects, need complete "RF closure" between the RFIC's system and circuit, electrical and physical, and design and test activities before commitment to costly IC implementation.

The Analog Office design system provides an new approach that achieves optimum RF design closure through a unified data model and design environment encompassing all of the design domains. The data model is high-frequency aware, permitting accurate extraction and modeling of all design elements, including active and passive devices, as well as interconnects, at high-frequency. The solution is built on AWR's open high-frequency design platform, enabling easy integration of the most capable tools to capture, synthesize, simulate, optimize, layout, extract, and verify designs from system to final tape-out. The Analog Office design suite is fully integrated into existing digital and mixed signal IC design flows from Cadence and Synopsys, and enables analog and RFIC design engineers to significantly shorten their development cycles and speed wireless products to market.

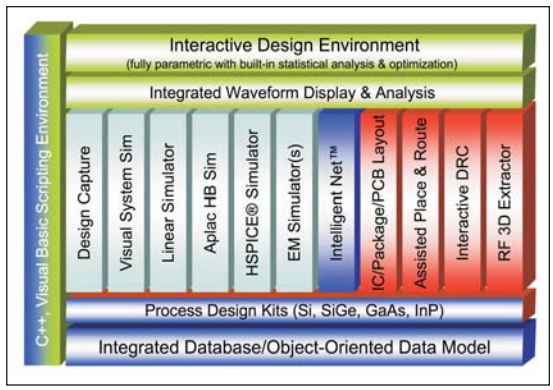

Figure 1 · The Analog Office 2006 open design platform integrates best-in-class tools, including four circuit simulators and five electromagnetic simulators.

Analog Office 2006 design platform features the second generation of the AWR Intelligent Net™ (iNet) technology, which powers "on-the-fly" interconnect extraction through an advanced interconnect-based design methodology. In this latest release, AWR continues its commitment to provide the industry with an easy-to-use, open RF design platform that is fully integrated with five best-in-class electromagnetic (EM) tools, as well as four circuit simulators (see Figure 1). Analog Office 2006 software offers a proven design flow and validated process design kits (PDKs), which enable multiple tape-outs, including several to the Jazz Semiconductor silicon germanium (SiGe) process.

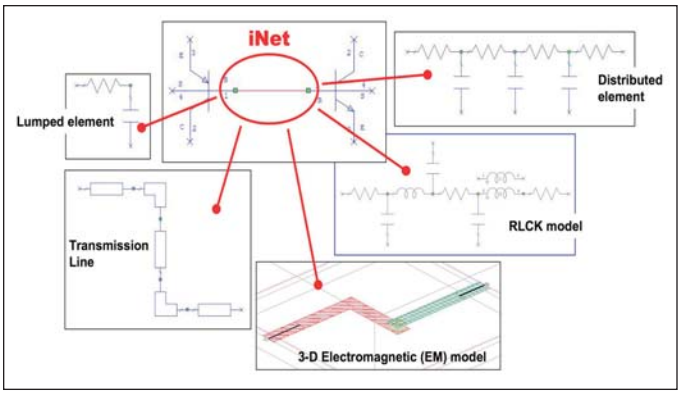

Figure 2 · Analog Office 2006 iNet2 technology features "on-the-fly" extraction of interconnect parasitics.

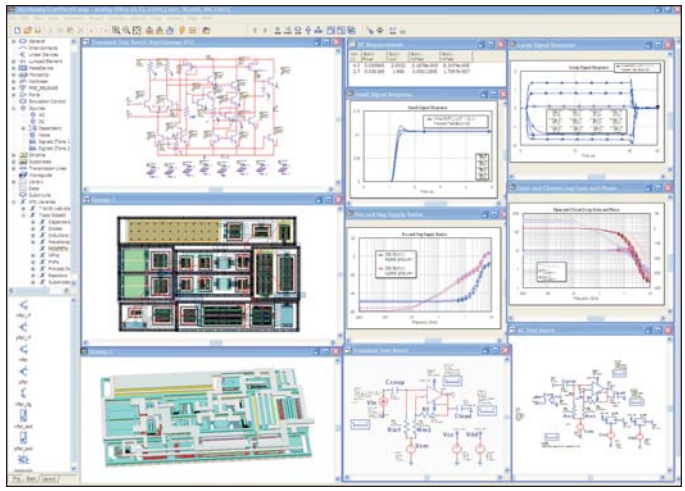

Figure 3 · iNet2 technology helps model and simulate critical nets in this broadband operational amplifier while the layout is in progress. The opamp is designed in a Jazz SiGe60 process.

Feature Descriptions

Integral to the Analog Office design suite is an interconnect-driven/RF-aware design methodology built around AWR's iNet technology. Similar to a timing-driven or wire-driven digital design methodology, the iNet methodology focuses on accurate RF interconnect modeling and analysis throughout the entire RFIC design process to reduce or eliminate design iterations, shorten the design cycle, and ensure first-time design success. Unlike existing net constructs built on a "digital-centric" data model, the Analog Office iNet technology is based on an RF-accurate net model with multiple levels of abstraction. Models for short-circuit, lumped, resistance-inductance-capacitance (RLC), distributed RLCK (including coupling inductance), fully-distributed transmission line, or full 3D EM elements use a single environment and data model. iNet technology provides concurrent and real-time physical modeling of RF interconnects while the layout is in progress, eliminating the need for a serial post-layout connectivity extraction step. Simulation and analysis can be invoked immediately to verify the performance of the design as soon as the critical nets are laid out, without waiting for the rest of the circuit to be completed (see Figure 2).

iNet2, the second-generation of this iNet technology, and its associated data model have been dramatically improved to deal with more complex, higher density RF layouts. Nets can now be created in segments which are then connected in a hierarchical fashion. This greatly simplifies the routing of the power supply and ground interconnects. Net creation and modification has been made much more flexible. Switching layers is effortless and via connections are automatically sized and inserted between metal layers and on device pins. Even if the layout is not completed, at any time during layout creation, the user can extract all or part of the implemented interconnect using NET-AN, the very accurate, embedded RLC and coupled C/L 3D multi-net net extractor from OEA International. The design can then be simulated with the parasitics of selective nets. (e.g., critical signal paths). Other systems cannot do partial extraction, requiring the layout to be completed and fully synchronized with the schematic (on a separate data base) via LVS before the layout parasitics can be considered. At that point problems can be hard to identify because correlation between the layout and schematic can be confusing. And when problems are identified, major rework is usually required. Within Analog Office software, the schematic and layout are in one database, and thus are always in sync, maintaining constant "connectivity-on-the-fly." Critical nets can be routed, modeled, and refined concurrently with the electrical design process. In this concurrent process, designers can more easily adjust the design or layout to correct any problems as they go. The full layout can then be completed (or a partially finished layout handed off to a layout specialist for completion), with assurance that major rework will not be necessary (see Figure 3).

Higher Capacity, Faster Layout Capabilities

Analog Office design suite provides IC designers with a complete physical design system to fully implement their analog and RF IC designs within a single environment, eliminating the need for switching between multiple environments and databases.

The package offers a completely interactive custom layout tool with integrated device-level, placement, and routing features to speed up the creation of analog and RF circuit blocks and chips. An integrated design rule check (DRC) capability and interface to industry's leading DRC tools ensure the physical layout being created always meets the process design rules, resulting in a cor-

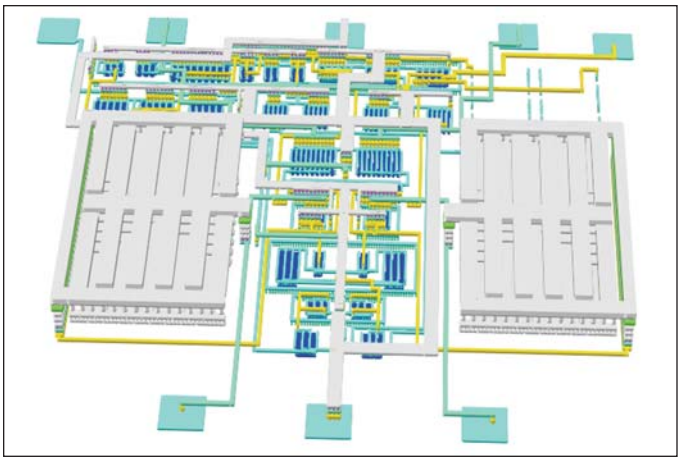

Figure 4 · A 3D view of the opamp layout in 0.13 µm RF CMOS process. allowing visualization of the layers.

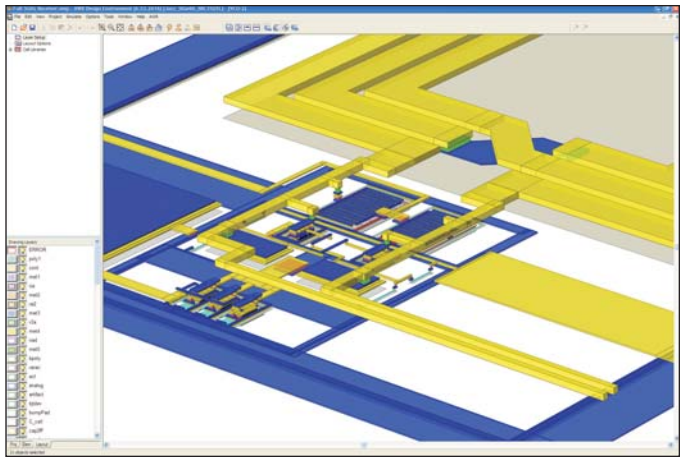

Figure 5 · A detailed 3D view of a 5.8 GHz voltage-controlled oscillator designed in Analog Office 2006 reveals a complex interconnect structure and device layout in the Jazz SiGe60 process.

rect-by-design, error-free layout. The layout editor is directly connected to the EM socket, providing on-the-fly EM extraction and modeling of arbitrary layout structures and complex spiral inductors. At every step during the physical design process, the iNet technology continuously updates in real time the underlying interconnect data model, and after each interconnect is "implemented" or laid out, concurrent simulation and analysis can be immediately invoked on the schematic or layout to verify the performance of the overall design without waiting for the final layout of the whole design to be completed (see Figure 4).

The Analog Office 2006 release features dramatic improvement in layout editing capacity and performance. Speed in common layout operations, such as opening designs, redrawing, and general editing, have been accelerated up to 100 times over the previous version. Physical layouts of hundreds of thousands of devices can be opened and viewed in a matter of seconds rather than minutes.

iNet2 technology now powers the manual routing of interconnects in a manner that is faster and more natural to IC designers. An iNet is a collection of wire segments connecting device and port pins. As the net is routed, connected pins are highlighted to assist the routing task. When a net is routed over a pin, a connection is automatically created and proper contacts or vias are inserted to complete the connection. Once created, connection points between two layers or vias can easily be edited and resized. While routing, the system can auto-set the layer of net segments using the horizontal-vertical (HV) routing option.

Nets, once completely laid out, can be easily ripped up and rerouted while retaining full connectivity. "Rubber band editing" eases net routing—when an end point is moved, only that segment and previous segment are moved. Net segments can be copied and pasted easily and connectivity can be associated with different nets. This feature is extremely useful when routing differential nets or "electrically-equivalent" nets, very common in analog and RFIC layout, where certain nets have to be matched electrically.

A new double buffering feature provides a fully rendered and dynamically displayed graphic view of the edited layout objects, speeding up editing tasks. An updated layout configuration dialog enables the user to easily switch layout viewing and editing configurations, and a new layer dialog box simplifies the task of setting up layers, turning them on and off, and hiding certain layers.

The pin data model in layout cells now adopts the OpenAccess pin data model, offering more flexible connectivity within the cell and between the cell pins and external nets. Routes can now go through cells. In addition, ports in the design can now have artwork cells associated with them, providing more flexibility in layout.

Along with feature enhancements and improvements in speed and capacity, the Analog Office layout editor now features full color editing animation and is rendered using the industry-standard OpenGL, which utilizes high-performance 3G graphics acceleration hardware found in most modern design workstations and high-end personal computers. OpenGL incorporates a broad set of rendering, texture mapping, special effects, and other powerful visualization functions (see Figure 5).

SPICE Extractor for Simulation in the Time Domain

Analog Office 2006 software includes an innovative approach to enable accurate modeling of interconnects and passive devices operating at RF and microwave frequencies. The approach is based on a technique of decomposing circuits into components that are either uniform

transmission lines, or elements of reasonably small electrical length. Accurate modeling of distributed components such as interconnects, transmission lines, transmission line discontinuities (such as T-junctions, crosses, etc.), and passive devices (such as resistors, capacitors, spiral inductors, and baluns) is essential if accurate simulation results for the complete circuit are to be obtained. Accurate transient simulation of transmission lines is obtained by using the HSPICE W-element with frequency-dependent RLGC matrices that are automatically generated from Analog Office's internal frequency-domain component models. The SPICE extractor also provides an accurate and efficient approach to transient simulation using models for passive components based on rational function approximations of frequency-dependent N-port parameters. Especially useful for simulations based on EM-analysis results, the rational function approximations are converted to Laplace transfer function models for efficient HSPICE simulation. Extensive testing with realistic customer circuits has demonstrated the success of these approaches.

Interface to the APLAC Simulator

The Analog Office 2006 release offers the power of the high performance, high capacity APLAC harmonic balance and RF-specialized time-domain simulators. APLAC's RF design technology has been widely used by Nokia Mobile Phones for many years, and has been used in the design of mobile phone RF ICs worldwide. The simulators offer many analysis options, including a unique transient-assisted harmonic balance simulation capability to handle difficult-to-solve frequency divider circuits and provide accurate non-linear phase noise measurements. APLAC simulators also include the most advanced non-linear device models for III/V and silicon technologies.

Improved NET-AN Integration

NET-AN, a 3D electromagnetic simulation technology from OEA International, has been incorporated into Analog Office through the AWR EM Socket™, an interface that integrates third party simulators into the Analog Office environment. NET-AN creates models of selected nets, normally called "extracted nets." The models are networks of lumped, circuit elements, such as resistors, inductors (including mutual coupling), and capacitors. The specific types and number of elements depends on the options chosen by the designer. The design flow works as follows:

- Lay out the critical nets using the iNet technology
- Select the nets of interest for extraction by using an extraction block
- If desired, use more than one extraction block for multiple extractions—for example, a high-speed analog/RF net and a low speed control line might be two different extractions
- Send the layout to NET-AN through the AWR EM Socket. This is executed automatically if the extraction is enabled.
- The simulation is run with the extracted elements included in the simulation

The selected nets are then modeled using NET-AN, with simulation controlled through the Analog Office EM Socket. Specifically, the simulation is controlled through the parameter settings of the extraction block, and the options settings in the generated EM Document.

The major NET-AN options, each of which trades off speed for accuracy, are explained below. The best choice depends on the level of detail needed for a specific net.

- Simulation Mode: Sets the type of elements that are used in the extracted model. Options are:
  - Shorts: All nets are modeled as perfect shorts
  - R: Model the nets as resistors only
  - RC: Model as resistors, capacitors only
  - RCL: Model as resistors, capacitors, and inductors
  - RCLK: Includes mutual inductance between inductors (greater than specified K_{min})
  - RL: Model nets as resistor and inductor only
  - RLK: Model nets as resistor and inductor only—includes mutual inductance.
- RC Time Constant: Sets the time constant in ps. The smaller the RC time constant, the greater the number of segments.
- Expansion Distance: Determines the maximum distance between two coupled nets (capacitive). Nets greater than this distance are regarded as uncoupled.

Busses/Bundles, Iterated Instances and Inherited Connections

With the improvements included in the new 2006 version, the Analog Office product can now handle complex, deep-submicron RF CMOS circuits with significant digital content. Arraying components, passing signals through lots of hierarchy, and representing large bit-width busses is an easy process with the new editor features. Complex Cadence schematics that use these features can now be more easily translated to the Analog Office software (see Figure 6).

In addition to handling the complexities of modern RFIC design in the schematic, Analog Office software stands alone in the ability to connect these features to layout. Because of the unified data model, connectivity is maintained between the schematic and layout. Busses, inherited connections, etc. in the schematic can be easily

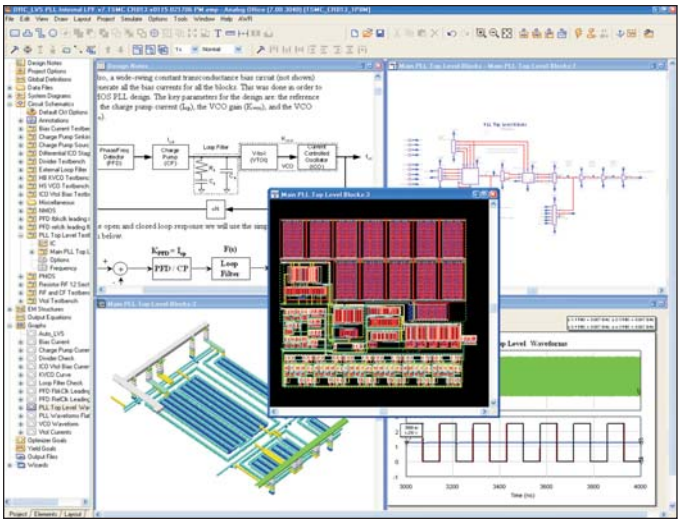

Figure 6 · Analog Office 2006 software handles mixed-signal design such as this complex phase-locked loop in a TSMC 0.13 µm RFCMOS process.

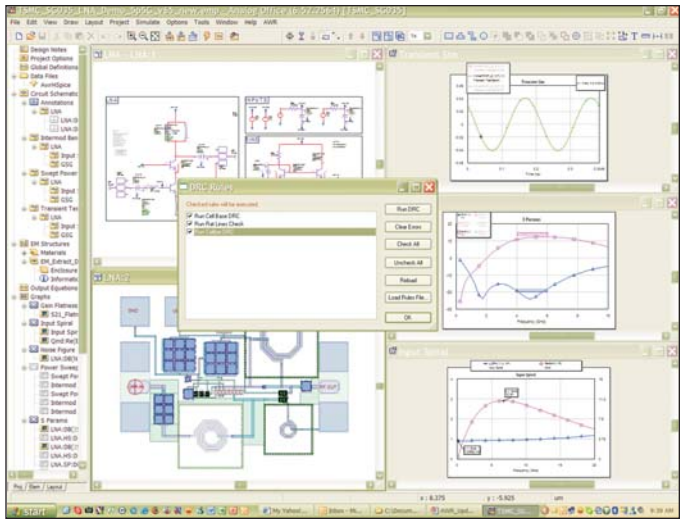

Figure 7 · The Analog Office 2006 interface to Mentor's Calibre DRC tool enables interactive verification of the layout.

referenced in the layout on-the-fly. A unique new feature of the new system is the ability to map component multiplicity into the layout. Now the designer can flexibly array complex device modeled as extracted components using the vectored instance. This feature provides the ability to model parasitic degradation within the arrayed device (like device de-biasing in arrayed power devices).

ERC for Current Density, Operating Limits, Shorts

Utilizing the unique AWR integrated electrical/physical data model, shorts between nets can now be detected without having to run full layout-versus-schematic (LVS), and the real interconnect current density can be displayed and the net graphically highlighted if electromigration rules are exceeded. Analog Office can do this on circuits that are partially laid-out. In addition, device voltage, current, and power limits can be checked and flagged to ensure they are not overstressed. Many other electrical rule check (ERC) rules are possible and under development to take advantage of this architecture.

Link to Mentor Calibre DRC and LVS Interfaces

The Analog Office design suite can be used to design the entire analog or RFIC from system-level modeling and simulation through to final layout and tape-out. The Analog Office suite of tools generates the necessary industry-standard files, such as LVS, netlist, and GDSII, to interface to a final verification flow based on industry-popular IC physical verification tools from Mentor Graphics, Synopsys, and Cadence.

The Analog Office 2006 release includes an improved interface between the Analog Office design platform and the Mentor Calibre DRC, as well as a completely new interface to the Mentor LVS physical verification tool. The appropriate data is exported to be analyzed by Calibre and the results are displayed within the Analog Office environment (see Figure 7).

Direct Import of HSPICE and Spectre Netlists

Analog Office 2006 software now includes the ability to import Spectre and/or HSPICE formatted netlists directly into the design platform, making them immediately available for simulation within the environment. This enables the user to bring in legacy designs or designs from other groups or companies without having to access a complete foundry process design kit (PDK).

Seamless IC Package Module Co-Design

For the design of ICs, an IC suite with IC timing analysis is needed. For the design of PCBs and modules, a PCB tool with SI tools is required. In the GHz range, the packaging of the die not only degrades the performance, but coupling to die makes it almost impossible to design the IC separately from the package. All of these issues are compounded when the preciously packaged IC is integrated onto a module or a PCB. Traditional IC tools are difficult to adapt to PCB design because they do not support packaged components very well and PCB tools have a limited notion of continuously scalable layout cells. The result has been flows that span half a dozen or more disparate tools, requiring that data be translated, designs be manually repaired, and the database be synchronized by hand, all with no guarantee of closure.

Analog Office 2006 software supports multiple technology files, enabling import of IC, package, and PCB design files, and allowing concurrent simulation and

analysis of critical interconnects spanning multiple implementation domains across ICs, packages, modules, and PCBs, all within the same project without the need for translation.

Recent Success

Analog Office software was recently used by a major Japanese electronics manufacturer to successfully design a 5.8 GHz radio-frequency integrated circuit (RFIC) in an advanced SiGe process from Jazz Semiconductor. The RF receiver design is the first complete silicon-based RFIC successfully designed and taped out using the entire Analog Office design flow from schematic capture, simulation, analysis, layout, extraction and complete DRC and LVS verification. First tapeout was done in August 2005 and the resulting chip, fabricated in October 2005, is fully functional and achieves full specifications.

Summary

The Analog Office 2006 design suite can be used to design high-frequency RFICs that are at the heart of next-generation wireless devices. These ICs, which operate at the 2.4, 5.8, and higher GHz frequency spectrum, drive a wide range of wireless applications such as wireless local area networks, wireless handsets and base stations, as well as emerging wireless broadband applications such as WiMAX and ultra wideband (UWB). High-speed networking applications, such as eletro-optical transceivers and switches, as well as network access applications such as home gateway boxes, xDSLs, and cable modems also employ analog ICs at the front end to transmit and receive high-speed signals.

Analog Office software can also be used to design high-precision and high-performance analog ICs such as amplifiers (low noise, differential, logarithmic, etc.), mixers, and modulators and demodulators, as well as high-speed digital circuits such as clock-data recovery circuits (CDRs), PLLs, and voltage-controlled oscillators (VCOs).

Built on an advanced software architecture, the unique core technology in the Analog Office design platform and underlying modern object-oriented data model provides an open and flexible environment that enables analog and RFIC design engineers to significantly shorten their development cycles and speed wireless products to market. The RFIC design process is accelerated by allowing the entire engineering team to effortlessly integrate and access all the best-in-class tools in one single environment and design flow, providing an accurate understanding of the impact of today's complex modulated RF signals and "real world" circuit performance. This protects customers' investment in models and simulators, lowers their cost of support, and enables easy customization of specific flow requirements. The result is a highly capable design approach that enables interactive tradeoffs between design requirements and circuit implementation.

Author Information

Tom Quan is vice president of marketing at Applied Wave Research, Inc. (AWR). He has over 20 years of experience in technical and marketing roles in the semiconductor and EDA industries. Prior to joining AWR, Tom was vice president of marketing at Cadence Design Systems and before that held executive management positions at Monterey Design Systems, Duet Technologies and High Level Design Systems. Tom holds a BSEE from the University of California, Berkeley, and an MBA from Santa Clara University. Tom can be reached at: tomq@appwave.com

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