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Linearity Improvement Techniques for Wireless Transmitters: Part 2

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This two-part article presents a wide range of techniques for amplifier linearization, along with historical notes to help us appreciate the creative work in their development

Reflect Forward Linearization Amplifier

The reflect forward adaptive linearizer (RFAL) technique uses the input reflected signal from one power amplifier to develop an intermodulation-correcting signal forwarded to the input of the other power amplifier which are connected in parallel or balanced configuration [23, 24]. Figure 6 shows a block diagram of the RFAL amplifier which includes the two identical power amplifiers, a low-distortion booster amplifier, forward and reflected paths with two directional couplers at the input, and delay line and in-phase combiner at the output. With the RFAL technique, the power combining efficiency of the two power amplifiers approaches that of the conventional parallel power amplifier configuration, while the intermodulation products can be improved from 20 to 30 dBc at the center bandwidth frequency.

The basic principle of RFAL operation can be described as follows: when the two-tone forward fundamental signal is reflected from the transistor input of upper power amplifier, the resulting reflected two-tone fundamental signal is out-of-phase relative to the input forward signal and is in-phase relative to the output signal. In this case, the intermodulation components appeared at the upper power amplifier input as a result of its active device nonlinearity are in-phase relative to the output intermodulation components. The input reflected composite signal containing the fundamental and intermodulation components is used as a correcting signal for the lower power amplifier. This correcting signal, when properly amplified and phased in the reflected path, cancels the output intermodulation distortions produced by the lower power amplifier when it is combined with the input signal flowing through the forward path. The booster amplifier in a lower path is necessary to equalize the drive signal levels for both upper and lower power amplifiers. In this case, the signals from the upper and lower amplifying paths have the in-phase fundamental and out-of-phase intermodulation components at the corresponding inputs of the output in-phase combiner, thus resulting in a distortion cancellation in the combined signal flowing into the load. The LDMOS RFAL amplifier with output power of 43 dBm achieves an improvement of the third-order intermodulation products by over 15 dB and a total efficiency of more than 20% over the frequency range from

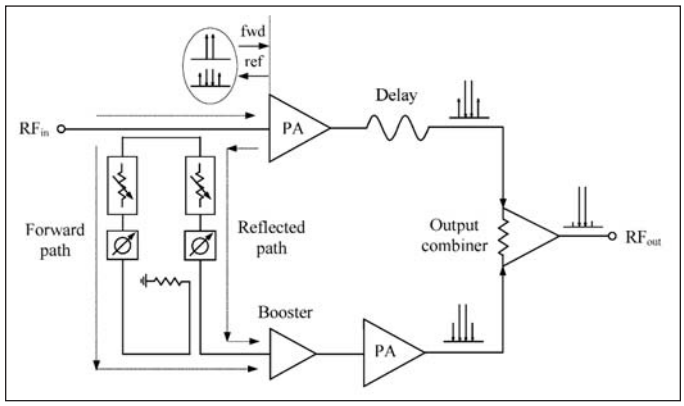

Figure 6 · Block schematic of reflect forward linearization amplifier.

865 to 895 MHz [25]. For very high cancellation requirements over wide temperature and drive conditions an adaptive feedback network can be used to monitor the relative amplitude and phase at the outputs of the power amplifiers and drive the voltage variable attenuators and phase shifters to maintain the optimum conditions.

Predistortion Linearization

To achieve simultaneous high-efficiency and low-distortion operating conditions of the power amplifier when the linearity requirements are not extremely high, it is possible to use a predistortion linearizer, which provides the positive amplitude and negative phase deviations for input RF signal to compensate for the active device nonlinearity. This is possible since nonlinear behavior (when a power amplifier is operated close to saturation) usually represents the opposite behavior of its amplitude and phase characteristics. Historically, the initial idea to compensate for the third-order intermodulation products arising in vacuum-tube amplifier was to use the linearization scheme where a nonlinear amplifier having a compressing characteristic is followed by a nonlinear element having an expanding characteristic and producing the third-order distortion of opposite sign to that of the amplifier [26]. The block diagram of the linearized power amplifier system with a predistortion linearizer with indication of the appropriate amplitude and phase dependences at each stage of the system is shown in Figure 7, where a variable attenuator for adjusting the amplitude level of the input signal is also included. At microwaves, a linearized power amplifier usually includes two isolators for stable operation conditions. The conventional predistortion linearizer circuits generally use either diodes or transistors as sources of intermodulation [27, 28].

As an interesting fact, as early as the beginning of the1920s, it was claimed that, by using similar vacuum tubes in both stages of a two-stage power amplifier with similar signals at their inputs, the even harmonics generated by the first amplification are neutralized by the even harmonics generated by the second amplification because they are similar in amplitude and opposite in phase at the output of the second vacuum tube [29]. Indeed, as it turned out with regard to modern transistor power amplifiers using GaAs pHEMT devices, it is enough to choose a proper bias point for a driver-stage device in a two-stage amplifier to provide a negative phase deviation to compensate for the positive phase deviation of the final stage [30]. In this case, the quiescent current of the driver-stage device, whose size is three times smaller than that of a final-stage device, is sufficiently small. As a result, for a quiescent current equal to 1.25% of the device DC saturated current, an improvement of more than 5 dB in *ACLR* of a whole high-efficiency two-stage cellular-phone WCDMA power amplifier operating at 1.95 GHz can be achieved at backoff output powers close to the saturation power.

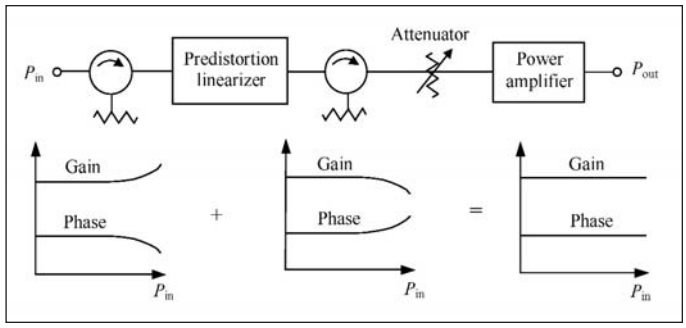

Figure 7 · Block diagram of power amplifier with predistortion linearizer.

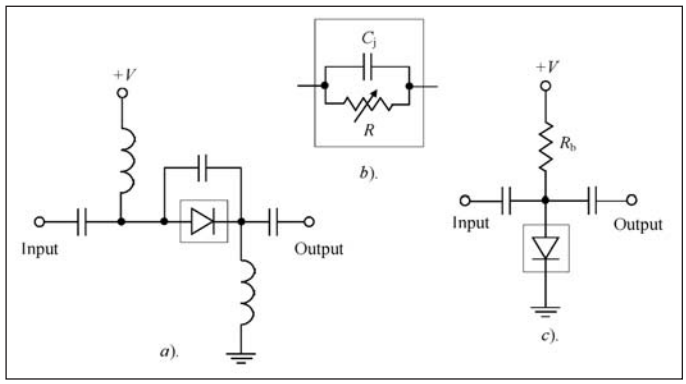

Figure 8 · Simple diode-based predistortion linearizers.

Figure 8(a) shows the schematic of a simple diode linearizer composed of a series Schottky diode and a parallel capacitor with two RF chokes for DC feed and two blocking capacitors, which provides positive amplitude and negative phase deviations when input power increases [31]. The equivalent circuit of the series diode is shown in Figure 8(b), where R is the diode equivalent resistance and C_j is the junction capacitance. With the increase of an incident input signal power, the forward diode current increases that leads to the decrease of the diode resistance R. In this case, the positive amplitude and negative phase deviations can be achieved under low forward-bias conditions when the diode current ranges from 0.1 to 1.0 mA, and, in the latter case, the phase deviation can reach a value of –30°. Applying such a linearizer to a 1.9 GHz MMIC power amplifier with saturated power of 22.5 dBm, an improvement of adjacent channel power ratio (*ACPR*) of 5 dB can be achieved for the QPSK modulated signal when output powers are less than 15 dBm.

A similar improvement of *ACPR* can be achieved by using a linearizer based on a parallel Schottky diode with the bias feed resistor R_b, which is shown in Figure 8(c) [32]. With the increase of input power, the bias point of a diode changes due to the voltage drop across the resistor R_b caused in turn by the increased diode forward current.

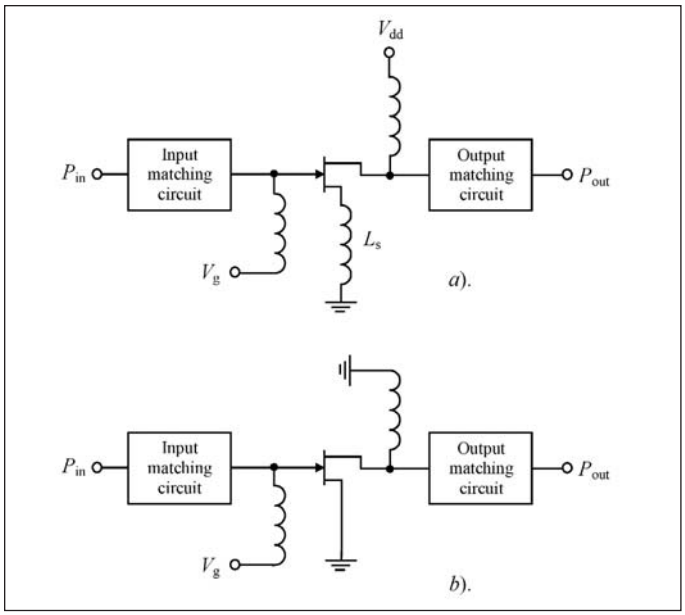

Figure 9 · Transistor-based linearizers.

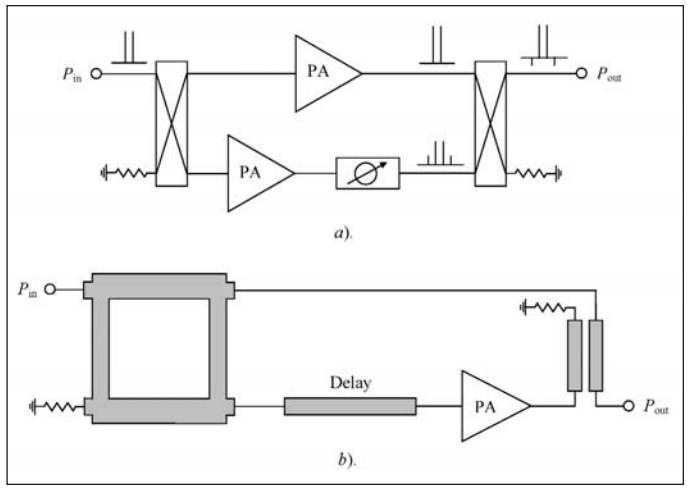

Figure 10 · Block diagrams of power amplifier linearizers with input power splitting.

As a result, due to the decreased diode resistance R, the linearizer achieves positive gain and negative phase deviations. By applying such a linearizer to a 2.7 GHz power amplifier, a maximum improvement of 5 dB was achieved for low quiescent current conditions at output power of 34 dBm.

Positive amplitude deviation with negative phase deviation can also be achieved using a series-feedback GaAs MESFET amplifier with a large source inductance L_s, a block diagram of which (including matching circuits) is shown in Figure 9(a) [33]. The required amplitude and phase deviations are due to nonlinearities of the device transconductance gm, gate-source capacitance C_{gs}, and differential drain-source resistance R_{ds}. For the device with a gate width of 1.2 mm, a nonlinearity of g_m contributes to the positive amplitude deviation when L_s = 20 nH. At the same time, nonlinearities of both g_m and R_{ds} contribute to the negative phase deviation when $L_s \geq 3$ nH. A nonlinearity of C_{gs} has a negligibly small effect on both the amplitude and phase deviations. As a result, for a linearizer with L_s = 16 nH at an operating frequency of 1.9 GHz, the positive amplitude and negative phase deviations were obtained across the input power dynamic range from 5 to 18 dBm, with amplitude deviation of 2.5 dB and phase deviation of 30° at 18 dBm input power. The GaAs MESFET device was biased in Class AB mode with a drain-source supply voltage of 2 V providing a quiescent current of 78 mA. By applying this linearizing technique to a 1.9 GHz MMIC power amplifier with 1-dB compressed power of 17 dBm, an improvement of *ACPR* up to 7 dB was achieved for a π/4-shifted QPSK signal.

As an alternative, it is also possible to achieve positive amplitude and negative phase deviations using a source-grounded MESFET device with zero drain-source supply voltage [34]. The schematic diagram of such a linearizer is shown in Figure 9(b). In this case, for the device with a gate width of 240 mm at the saturation power of 20 mW under the gate bias condition of V_g = –0.4 V, the 3-dB increased power gain and of about 30-degree negative phase were achieved using the varying drain-source resistance. Because of its simplicity, such a linearizer can operate from 2 to 12 GHz with good thermal stability. When it was implemented into a 50 W solid-state power amplifier system at operating frequency of 7 GHz, the system noise power ratio was improved over 15-dB dynamic range, in particular by 2 dB at the 3-dB output power backoff point.

A more advanced configuration of the predistortion linearizer is based on the splitting of the input signal into nonlinear and linear paths using a directional coupler or a hybrid divider with subsequent subtraction of the resulting signals in the output coupler-subtracter. The block diagram of such a predistortion linearizer which employs two power amplifiers in a balanced configuration using two 90-degree hybrids is shown in Figure 10(a) [28]. In this case, the upper power amplifier is operated in a linear Class A mode while the lower power amplifier is biased in a nonlinear Class AB or B mode to generate the proper intermodulation products by controlling the input power and device bias conditions. The phase shifter in a lower amplifying path is necessary to optimize the level of the fundamental components in the resulting output spectrum. Since both devices present approximately the same input impedances, a low input return loss is provided because the most of the reflected power flows into the isolated port. Figure 10(b) shows the practical microwave microstrip implementation of a two-path predistortion linearizer with an input 90-degree branch-line hybrid

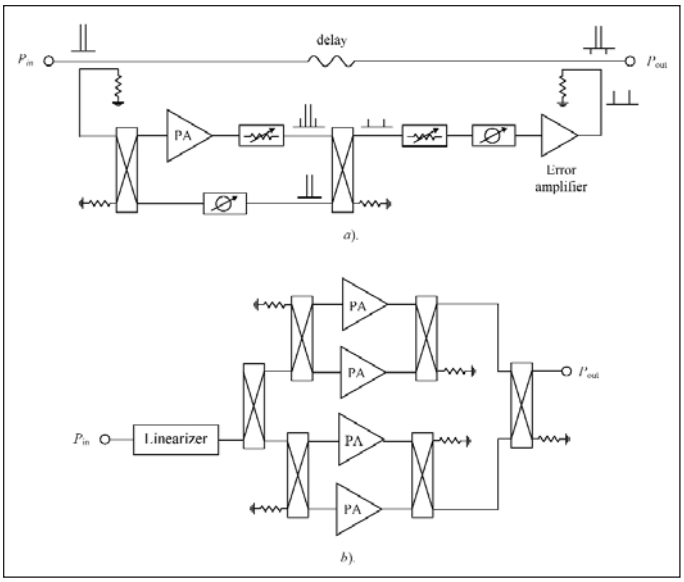

Figure 11 · Power amplifier module with linearizer.

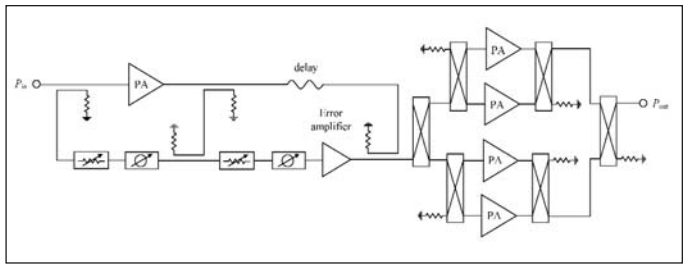

Figure 12 · Power amplifier module with feedforward predistortion linearizer.

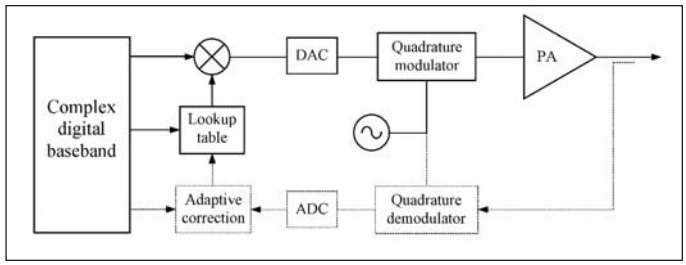

Figure 13 · Digital predistortion system.

coupler, a nonlinear power amplifier in a lower path and an output directional coupler [35]. The microstrip transmission line in a lower amplifying path having a required electrical length compensates for the additional phase shift provided by the active device, whereas the required amplitude conditions are realized with the coupling coefficient of an output coupler-subtracter to be chosen. As a result, for a Ku-band multicarrier 4.5-W power amplifier, the phase deviation of a 12-dBm signal at the linearizer output up to –10° was achieved with a 22-dBm signal at the linearizer input.

Figure 11(a) shows the modified three-path predistortion linearizer structure, where a balanced configuration with a nonlinear power amplifier is adjusted for suppression of the fundamental components with the resulting error signal. Then, the amplitude-adjusted and properly phased error signal is amplified by an error amplifier and added to the linear component in the upper path which is a delayed portion of the input signal. However, it is very difficult to match the nonlinear characteristics of the predistorter and the main power amplifier, because generally they differ both in size and number of stages, which can only result in less than 10 dB improvement of adjacent channel leakage power ratio (*ACLR*) at 5 MHz offset from the center bandwidth frequency [36]. Therefore, it is very important for further linearity improvement to use similar devices in the predistorter and in the main power amplifier with a preferred balanced structure. As an example, the block schematic of a power amplifier module which includes a three-path predistortion linearizer and a main power amplifier based on four power amplifiers configured into a balanced structure is shown in Fig. 11(b). In this case, when the same transistors are used both in the linearizer and main balanced power amplifier operated in Class AB mode, a 12-15 dB improvement of *ACLR* for the signal with peak-to-average ratio (PAR) of 6.5 can be achieved, depending on how close the device operation mode is to saturation.

The concept of a feedforward loop with its high cancellation performance can be used for a predistortion linearizer implementation. Since the feedforward loop is placed in front of the main amplifier, the linearity and power requirements of the error amplifier are reduced significantly compared to the conventional feedforward system. In this case, the delay-line and coupler losses are less significant factors affecting the amplifier performance. Figure 12 shows the simplified schematic diagram of a power amplifier module with the feedforward distortion linearization using five identical power amplifiers based on MRF5S21090 LDMOS devices [37]. For a forward-link four-carrier WCDMA signal at 2.35 GHz, the *ACLR* was enhanced by about 7 dB at 5 MHz offset and the total efficiency of 12.7% was achieved at an average output power of 47.8 dBm, backed-off by 10.8 dB from the total peak power of 720 W.

Figure 13 shows the block schematic of a digital predistortion linearizer where the predistortion algorithm is based on an initially measured PA amplitude-to-amplitude modulation (*AM-AM*) and amplitude-to-phase modulation (*AM-PM*) response extracted from the *S*-parameter measurements by a vector network analyzer (VNA) [38]. The amplitude and phase characteristics are interpolated using splines, which are continuous piecewise cubic functions with continuous first and second derivatives. The

interpolated amplitude and phase characteristics are then used to compute the appropriate predistortion coefficients representing a lookup table which are multiplied with the original IS-95 signal to generate the desired predistorted baseband signal. The results show the limitations of this technique when the LDMOSFET power amplifier operation conditions are close to saturation, only a little more than 6-dB improvement in *ACPR* can be achieved. Generally, an adaptive correction mechanism is required to maintain the performance over varying load, supply voltage, or temperature conditions. This means that the lookup table needs to be updated continuously to keep differences between the source signal and the transmitted signal sufficiently small. This can be realized by downconverting the portion of the transmitted signal and comparing it with source signal. In this case, it is important to provide the optimization of the wordlengths required in different parts of the predistortion linearizer to reduce power consumption and increase bandwidth for the required adjacent channel interference level [39]. The feedback complexity can be reduced with special adaptation algorithm when a single mixer and ADC are used in the feedback path instead of the full quadrature demodulation [40]. In addition, a non-iterative adaptation method can be used to eliminate the convergence constrains usual for iterative methods [41].

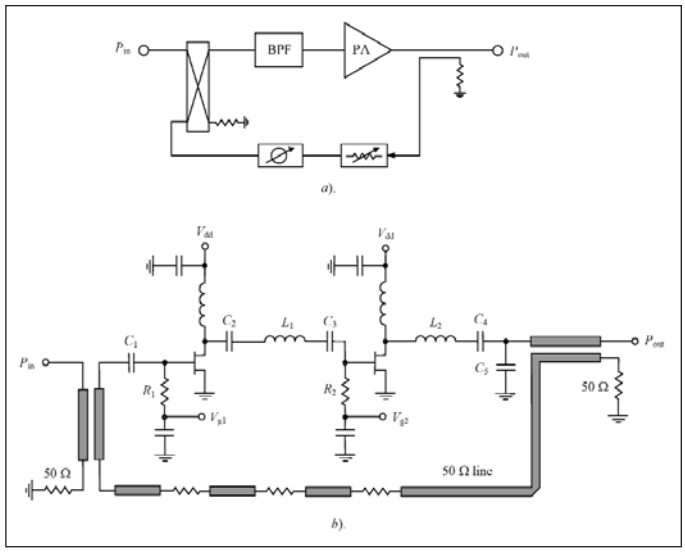

Figure 14 · Negative feedback power amplifier schematic.

Feedback Linearization

The principle of feedback linearization of the power amplifier at the carrier frequency was invented by Harold S. Black in 1927. A year later he filed the patent application on a vacuum-tube feedback amplifier [42]. Black recognized that by using a large amount of feedback in an amplifier comprising several vacuum-tube stages in cascade to yield a very high open-loop gain gives a glorious opportunity to make a negative feedback amplifier having increased bandwidth, and which is insensitive to nonlinearity and uncertainty in the characteristics of the vacuum tube [43]. The gain of the negative feedback amplifier decreases by amount of the feedback or loop gain; so do the nonlinear components. In this case, the negative feedback amplifier becomes insensitive to the gain or phase variations as long as its stability conditions are satisfied. In the latter case, if each of three tuned circuits of a three-stage vacuum-tube RF feedback amplifier can be assumed to have the phase-gain characteristics of the interstage circuits very nearly to infinite Q-tuned circuits, the maximum amount of feedback will allow a phase margin of 30° from a total phase shift of 180° [44]. Unfortunately, the significance of this invention, as well as the operation principle of a negative feedback amplifier, was not fully understood at that time. For instance, Black's director of research insisted that a negative feedback amplifier would never work, similarly the Patent Office initially did not believe it would work and took over nine years to decide to issue the patent [45]. Even today, Black's pioneering role for further achievements in feedback theory and practice is not well known.

The basic structure of a negative feedback amplifier at microwave frequencies is shown in Figure 14(a) where the power amplifier, bandpass filter (BPF) and feedback loop elements are chosen to provide a loop transmission greater than one with a phase shift of 180° within the operating bandwidth [46]. In this case, the BPF must be a single tuned resonator, so that the phase shift introduced will be less than 90°. By using a 50-dB gain power amplifier, an improvement of the third-order intermodulation components by 10 dB (from –30 dBc down to –40 dBc) at midband frequency of 2 GHz with the power gain of the closed loop system of about 34 dB and output power of 33 dBm was achieved [47]. It should be mentioned that the feedback power amplifier designed to operate at 835 MHz in communication system can provide a distortion improvement of 10 dB at saturated region, if the feedback gain of at least 20 dB is achieved [48]. Although, a feedback gain of 10 dB results in approximately 10-dB improvement in adjacent channel leakage power at 3 dB power backoff from saturation. In contrast, for the simple resistive feedback single-stage power amplifier, the level of the third-order IMD components at 2 GHz can be reduced by about 5 dB for the medium-signal levels only [49].

Figure 14(b) shows the circuit schematic of the two-stage power amplifier designed for a 3.4-4.2 GHz frequency bandwidth [50]. The output power of 27 dBm was achieved by using a power MESFET device with a gate length of 0.5 mm in the second stage. Loop gain was adjusted by changing the coupling in the output direc-

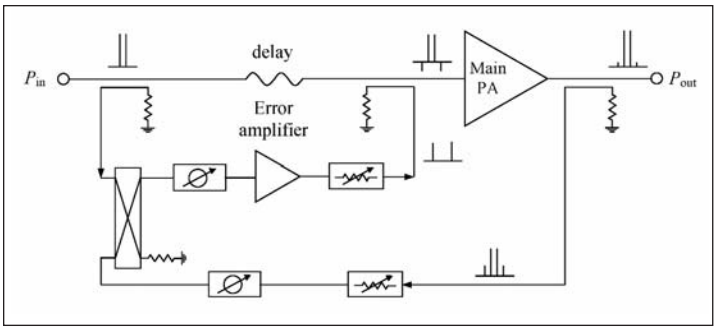

Figure 15 · Power amplifier module with feedback-feedforward linearization.

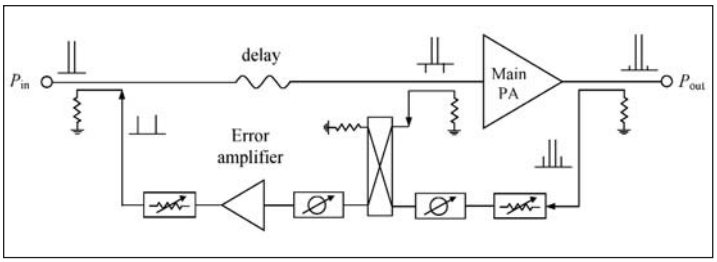

Figure 16 · Power amplifier with feedback predistortion linearization.

tional coupler, whereas a phase shift of 180° in the feedback path at midband was obtained using a microstrip line with the proper electrical length. The predicted open-loop gain was 19 dB at 3.7 GHz, decreasing to 13 dB at the upper bandwidth frequency. The shunt resistor at the input of the first MESFET device is necessary to improve the input return loss. As a result, for the closed-loop configuration, an improvement of the third-order intermodulation components of 7 to 9 dB over a 750 MHz bandwidth at –3 dB power backoff with a power gain of about 10 dB and an input return loss of more than 10 dB.

To improve the gain capability of the negative feedback amplifier, it is possible to combine its simplicity with a feedforward technique to provide a separate path for the error signal only. Figure 15 shows the schematic of the power amplifier module with a feedback-feedforward linearization when the intermodulation distortion products at the main PA input (symbolically plotted as out-of-phase) should be phased in a way that they cancel the intermodulation distortion products at its output. This modified negative feedback circuit can provide a reduction in the intermodulation distortion products equal to the traditional negative feedback topology without the usual reduction in overall amplifier gain [51]. According to the intermodulation distortion analysis based on Volterra series, the reduction of the power amplifier linear gain is dependent on the feedback at the fundamental only, while the third-order intermodulation components are reduced due to effect of the feedback factor both at the fundamental and at the intermodulation frequencies when a reduction is equal to the loop gain in the latter case [52]. This means that, if the fundamentals were removed from the feedback loop, there would still be a reduction of the intermodulation products due to the feedback at the intermodulation frequencies with unaffected amplifier gain. In this case, the feedback signal is coupled from the output of the power amplifier, properly attenuated and phase shifted to form the error signal with cancelled fundamental by combining with a lower portion of undistorted input signal. The resulting error signal is then amplified, scaled in the amplitude and phase, and finally combined with a delayed upper portion of the undistorted signal to form the composite signal at the amplifier input with out-of-phased distortion products required to cancel the intermodulation products at the amplifier output. The stability analysis shows that, for narrow-band amplifiers with minimum loop delay, the reduction of third-order intermodulation products can exceed 20 dB [51].

The feedback linearization technique can also be implemented reversely to a feedforward scheme, as shown in Figure 16, where the linearizing circuit consists of the feedback, canceling and feeding blocks [53]. At the canceling block, the amplitude-corrected and phase-shifted feedback signal is combined with the sampled input signal to form the error signal, which is then amplified and added with proper amplitude and phase to the input undistorted signal within the feeding block. As a result, for a 38-dB main amplifier gain, the cancellation of the third-order intermodulation products from –22 to –42 dBc were achieved at the output power P_{1dB} = 27 dBm and operating frequency of 1.85 GHz. However, the critical problems of this analog feedback predistortion scheme are the bandwidth limitation caused by the loop delay and an oscillation tendency caused by the feedback nature. By employing a digital lookup table (LUT) technique, these limitations can be overcome, while maintaining the advantages of the feedback circuit [54]. As a result, the distortion is corrected in a digital domain and further enhanced by the feedback linearization. In this case, the structure of a digital feedback linearizer is the same as the analog feedback counterpart, except that the feedback signal in the cancellation loop constructs a LUT in the digital domain, and the gain factors of the signal canceling and feedback paths are adjusted by the DSP instead of using the variable attenuators and phase shifters. The predistortion signal is extracted directly from the LUT, which has been updated using the error signal extracted at the signal cancellation loop beforehand. Thus, the time delay through the loop is eliminated, and the bandwidth limitation does not exist anymore. At the same time, the oscillation tendency of the feedback

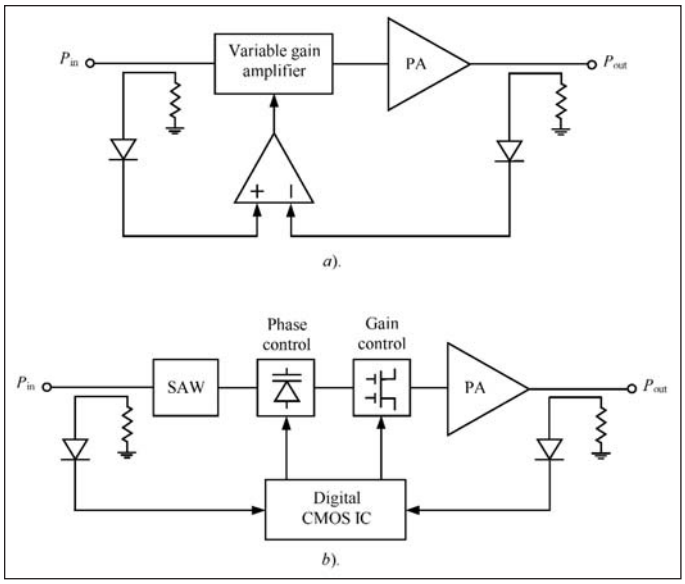

Figure 17 · Block diagrams of power amplifier with adaptive predistortion.

circuit can be suppressed easily by digital control of the feedback loop parameters. Compared to the conventional digital predistortion technique, less number of iterations is required for convergence with simpler algorithm.

The envelope-feedback linearization is a simple and popular technique to improve the distortion associated with the amplitude nonlinearity of the power amplifier [44, 55]. The basis of this technique, shown in Figure 17(a), is to compare the envelopes of the input and output signals, and to control the instantaneous gain of the power amplifier so as to minimize the difference between them. In this case, the RF input and output signals are sampled by the corresponding input and output couplers and then each fed to the proper input of the differential amplifier. The difference signal, representing the error between the input and output envelopes, is used to drive a variable gain amplifier to modify the envelope of the input signal which drives the power amplifier. The linearization effect depends on the nonlinearity of the detectors, especially at low signal levels, the bandwidth, time delay and phase-gain characteristic of the feedback loop and the sensitivity of the variable gain amplifier. Therefore, where the *AM-AM* distortion is dominant, the two-tone intermodulation products are typically reduced by up to 10 dB. To provide a significant improvement in the nonlinear distortion cancellation, both RF feedback and envelope feedback methods can be combined [44].

Figure 17(b) shows the envelope-feedback power amplifier module with a digital adaptive predistortion developed for CDMA handset application in a frequency range of 887-925 MHz [56]. The block diagram of the power amplifier module includes additionally a SAW filter, a phase-controlling block and a CMOS integrated circuit incorporating two look-up tables to linearize *AM-AM* and *AM-PM* characteristics. The variable gain amplifier is based on a dual-gate MOSFET to linearize *AM-AM* characteristic, which can easily vary the power gain by controlling its second-gate bias voltage in a range of more than 10 dB. In the phase-controlling block, a varactor diode was used with the phase range of more than 10°. By producing appropriate *AM-PM* predistortion data including phase characteristics of the dual-gate MOSFET and the following PA block, the total *AM-PM* can be linearized. Because the variations of phase with supply voltage and temperature according to the measurement results were insignificant, it was enough to use the lookup table with modified initial data to minimize phase variations versus input power that were predictable in advance. To linearize *AM-AM* characteristic, the adaptive predistortion was used by modifying the data in look-up table during linearization process. It was found that the allowable time delay must be less than 40 ns for CDMA signal. As a result, by using a digital adaptive predistortion mechanism for only *AM-AM* characteristic, the *PAE* was increased up to 48% for the output power of 27.5 dBm and *ACPR* of –49 dBc. The CMOS integrated circuit, whose size is 2.5×2.5 mm^2, consumed of about 15 mA.

The *AM-AM* linearization can also be achieved by dynamically varying the gate bias voltage of the final-stage transistor. In such an adaptive double-envelope feedback two-stage MESFET power amplifier the gain variations are detected directly while the phase variations are detected through a 90° branch-line coupler [57]. This is possible since, when the gate goes more negative, the MESFET is closer to pinch-off and its gain is reduced. On the other hand, as the gate goes more positive, the MESFET will approach Class A, where its gain is maximal. The dynamic bias on the gate of the device resulted in a 1 dB increase in P_{1dB} which improved the *PAE* by 5%.

To overcome the limitation of the envelope-feedback technique to correct for *AM-PM* distortion, the polar-loop technique can be used where a phased-lock loop is added to the envelope feedback system resulting in a polar-loop feedback [58]. However, the key disadvantage of a polar feedback occurs in the generally different bandwidths required for the amplitude and phase feedback paths, as well as locking capability of the phased-lock loop is limited at low signal level in the presence of interference coupled to the transmitter output from antenna that leads to a poorer overall performance. The Cartesian-feedback technique can solve at some extent the problems associated with the wide bandwidth of the signal phase by applying modulation feedback in the in-phase (I) and quadrature (Q) Cartesian baseband components. Figure 18(a) shows the basic block diagram of the Cartesian loop transmitter with two identical feedback loops for I and Q chan-

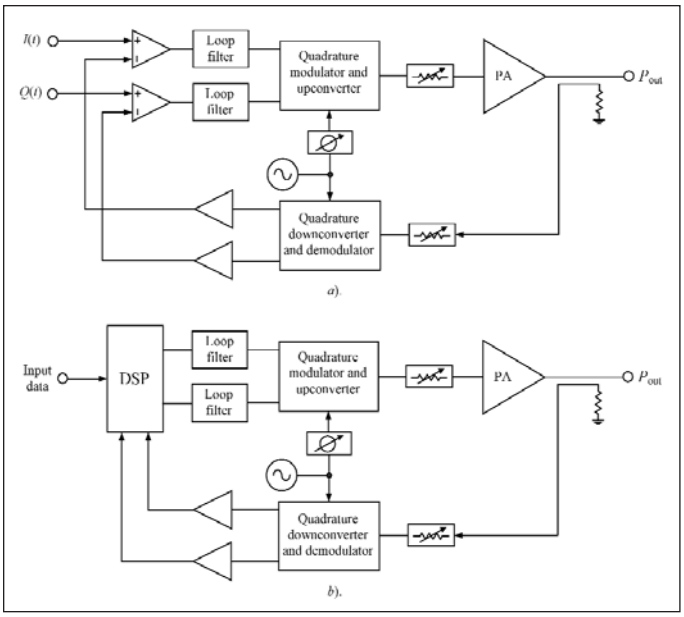

Figure 18 · Digital predistortion system.

nels [12, 59]. In this case, the sampled output signal is quadrature downconverted and demodulated to Cartesian co-ordinate signals, amplified and then subtracted from the corresponding input signals to form a distorted error signal which is complementary to the distortion signal at the PA output after being filtered and upconverted. The amount of the distortion reduction is equal to the loop gain and is high inside the passband of the loop filters. The phase shifter is necessary to control the phase delays which cause rotation of the signal constellation. The bandwidth of the Cartesian components is narrower than that of the RF signal, however errors in the feedback loop are not corrected and feedback components must be as linear as the desired loop linearity. The Cartesian feedback can be used to linearize multicarrier power amplifiers, improving output spectrum by 10-30 dB [60].

Further linearity improvement can be achieved by using a combined Cartesian loop and adaptive baseband predistortion linearization techniques using DSP, as shown in Fig. 18(b) [61]. Adaptive predistortion provides a continuous adjusting of the loop time delays and updating of the predistorter lookup table with information of the PA nonlinearity, which changes with supply voltage, temperature, load voltage standing wave ratio (*VSWR*), output power, and other environmental effects. For example, by using the predistorter implemented in DSP with 5 bit effective resolution digital-to-analog converters at its output and optimized using a direct search algorithm, a further 11 dB reduction of the third-order intermodulation components was achieved when a predistorted component was added to the error signal [62]. However, as the bandwidth of transmitting signal gets wider, the feedback loop delay mismatch becomes increasingly detrimental to the convergence of LUT adaptation algorithm. In this case, the analog Cartesian feedback, which is separated from LUT, can be used only for LUT training, thus resulting in the energy-efficient and low-complexity adaptive linearization [63]. Then, after the completion of LUT training, the analog Cartesian is turned off so that open-loop predistortion is performed using a compact Cartesian LUT to linearize wideband signals. The renewal of the LUT can happen without interrupting ongoing communication because the LUT training needs a millisecond and most communication protocols implement enough buffering for an error control method such as automatic repeat request. How often the LUT would need a renewal depends on PA characteristics and the environmental conditions.

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