From June 2008 *High Frequency Electronics*

Building a Microwave Frequency Synthesizer—Part 2: Component Selection

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This series of articles continues with a review of individual components from the perspective of their practical use in microwave frequency synthesizers

As discussed in the previous article, a frequency synthesizer can be thought of as a black box containing various components (e.g., oscillators, phase detectors, frequency dividers, multipliers, mixers, amplifiers, etc.), which being properly connected, translate an input reference signal to a number of output frequencies. The synthesizer implementation as well as its ultimate performance depends heavily on characteristics of the individual components used in the design. Although there is no set definition for the term "components" (they can be actually complex conectorized modules), in this article we will mostly refer them as surface-mount parts, which can be placed on a printed circuit board. The characteristics and behavior of the main synthesizer parts are reviewed from the perspective of their use in practical synthesizer designs.

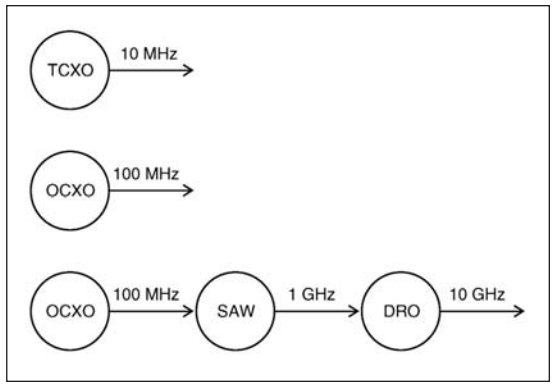

Figure 17 · Some common reference frequency generation schemes.

Reference Oscillator

A reference oscillator is one of the most important parts that defines stability and phase noise characteristics of frequency synthesizer. Various reference oscillator schemes are possible as shown in Figure 17. A 10 MHz temperature-compensated crystal oscillator (TCXO) provides low size and cost benefits for low- to moderate-performance applications. Better stability and noise characteristics are achieved by using an oven-compensated crystal oscillator (OCXO), but this is a more expensive and bulky part with a higher power consumption. It is worth mentioning, that using a higher frequency OCXO (e.g., 100 MHz instead of 10 MHz) can potentially result in a better synthesizer noise. There is a comparable noise floor for both parts, but the high frequency reference requires a significantly lower overall multiplication factor.

Even better phase noise performance at higher frequency offsets (100 kHz and above) can be obtained with additional low-noise oscillators (e.g., SAW, CRO, or DRO) locked to the main OCXO. The chain of oscillators (which can include two or even more parts) provides the lowest phase noise profile at any frequency offset and can be used in high-end synthesizer designs. The high-frequency oscillators are usually purchased parts, although, they can be built as a part of the synthesizer design to minimize the overall size and cost. However, building a low-noise microwave oscillator (e.g. a DRO) with adequate phase noise performance is not a trivial task; it requires careful design and optimization.

The phase noise behavior of a microwave oscillator (shown conceptually in Figure 18)

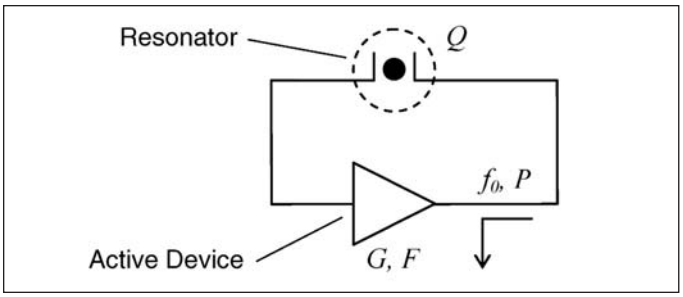

Figure 18 · Oscillator block diagram

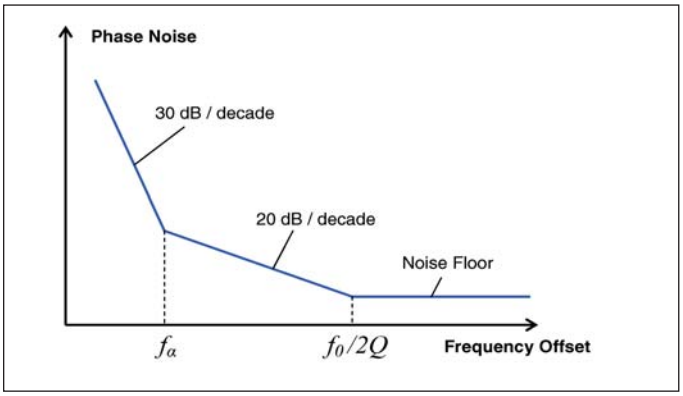

Figure 19 · Oscillator phase noise characteristics.

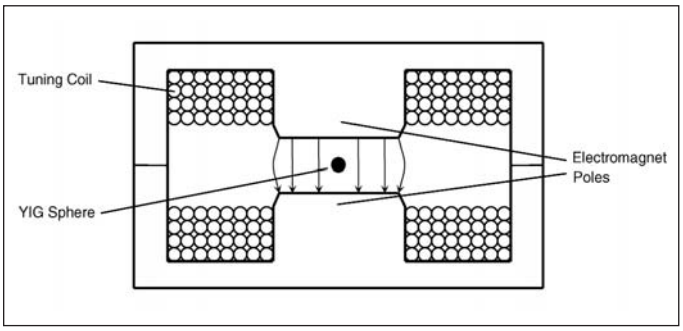

Figure 20 · A YIG resonator placed between poles of an electromagnet.

has been extensively investigated [23-27] and can be represented as follows:

$$\chi = 10\log\left\{\frac{GFkt}{2P}\left[\left(\frac{f_0}{2Q}\right)^2\cdot\frac{f_a}{f^3}+\left(\frac{f_0}{2Q}\right)^2\cdot\frac{1}{f^2}+\frac{f_a}{f}+1\right]\right\}$$

where: G is active device gain, F is active device noise factor, k is Boltzman's constant, T is temperature, P is RF power applied to the resonator, Q is resonator loaded Q-factor, f_0 is oscillation frequency, f_a is active device flicker corner frequency, f is offset frequency. This expression is essentially a modified Leeson's equation that depicts the oscillator phase noise behavior in the frequency offset domain. Although the formula defines four basic frequency offset regions, in microwave oscillators the $1/f$ term is usually ignored due to $1/f^2$ noise domination that leads to a "classical" oscillator phase noise profile shown in Figure 19. For offset frequencies higher than the resonator half bandwidth $f_0/2Q$, the phase noise is mainly determined by the available RF power level and active device thermal noise. This region shows nearly flat response called "noise floor." For frequencies between the half bandwidth and flicker corner frequency f_a , the phase noise increases at 20 dB per decade. In the last region, where the flicker noise dominates, the phase noise increases at 30 dB per decade.

This graph gives simplified, but nevertheless, very helpful visualization of the phase noise behavior as well as some intuitive ideas how to reduce its appearance in the oscillator output spectrum. Clearly, utilizing low flicker noise devices (e.g. silicon bipolar transistors) and applying a high-Q frequency resonator technology are effective, and commonly used ways to minimize the phase noise. Alternatively, the entire noise curve can be shifted down by increasing the oscillator signal-to-thermal noise ratio. This can be practically achieved by maintaining a higher power level in front of the resonator or/and reducing the active device noise factor, while the active device gain should be set to its optimum value (determined be the resonator coupling). Oscillator design methods and phase noise reduction techniques are described in [28-32].

VCO or YIG?

Historically, high-performance PLL synthesizers have relied on YIG-oscillators featuring broadband operation and excellent phase noise characteristics. The YIG is an acronym for yittrium iron garnet, a ferrite material that displays a unique, high-Q frequency resonance characteristic when exposed to a magnetic field [33-37]. The YIG resonator represents a small (8-20 mils in diameter) sphere placed between two poles of cylindrically reentrant electromagnet and coupled with small wire loops (Fig. 20). Frequency tuning is possible since the resonant frequency of the spherical YIG resonator in uniform magnetic field is a function of the magnetic field strength. The basic relationship between the resonant frequency f and magnetic field strength H is given by: $f = gH$, where: g = 2.8 MHz/Oe is a physical constant called gyromagnetic ratio. Therefore, the resonant frequency is in direct proportion to the magnetic field, which can be controlled by changing DC current injected into the electromagnet tuning coil. Practical usable frequency range of pure YIG resonators lies between 2 and 50 GHz. While the higher frequency is mainly limited by the magnet saturation and high power dissipation, lower limit is governed by the YIG saturation magnetization. Lower operating frequencies (a

few hundred MHz) are obtainable adding special dopes (such as gadolinium) that, however, degrades the Q-characteristics.

The YIG resonators offer a relatively high Q (greater than 4,000 at 10 GHz) that results in low phase noise performance. The YIG oscillators also feature very linear (and repeatable) tuning characteristics that simplify the synthesizer coarse tuning algorithm in multiloop schemes. The main disadvantages are high power consumption, large size, high cost, and especially low tuning speed due to high inductance of the tuning coil. Typical achievable switching time is in a milliseconds range.

An alternative solution is a voltage-controlled oscillator (VCO) based on either lumped LC or distributed microstrip resonators. Unfortunately, Q-factors of these resonators are not so high; typical values are between a few tens and few hundreds dependent on a particular technology and tuning range. The frequency tuning is achieved using varactor diodes, whose capacitance depends on the applied tuning voltage. Unlike YIGs the VCOs are extremely fast; microseconds operation is easily achieved. VCOs are currently available as tiny ICs, whose size, power consumption and cost is negligible in comparison with the YIG devices. However, the noise performance is considerably worse because of the lower Q of the utilized resonators (which is further degraded by the varactor diodes).

What technology is more preferable? The VCO clearly dominates in low-cost, low- to moderate-performance designs. However, for high-performance, broadband, low-noise applications (e.g., test and measurement) the answer is not so obvious. YIG-based solutions are usually simpler since the YIG-oscillator can forgive and mask many design imperfections. One can relatively easy achieve respectable phase noise performance with a simple single or dual-loop PLL by locking the YIG with a 10 kHz loop bandwidth and relying on its free-running noise at higher frequency offsets. Obtaining comparable noise performance with a VCO is much more challenging task since the designer can only rely on the reference oscillator and PLL characteristics. At a 100 MHz output frequency, today's commercial OCXOs perform at –160 to –176 dBc/Hz at 20 to 100 kHz offset. These numbers can be potentially translated to –120 to –136 dBc/Hz at a 10 GHz output. This theoretical performance corresponds to or even exceeds the performance of the best YIG oscillators at the same offset frequencies. However, it is very hard (if possible at all) to provide such an ideal translation since some noise degradation always occurs. Thus, achieving YIG-comparable noise characteristics for a VCO-based design is not a trivial task that calls for advanced multiloop solutions and also requires a great deal of effort to treat various "secondary" effects (e.g. voltage regulator noise, etc.). Nevertheless, the current technology trend toward faster tuning and lower cost puts the VCO in a better position for many practical scenarios.

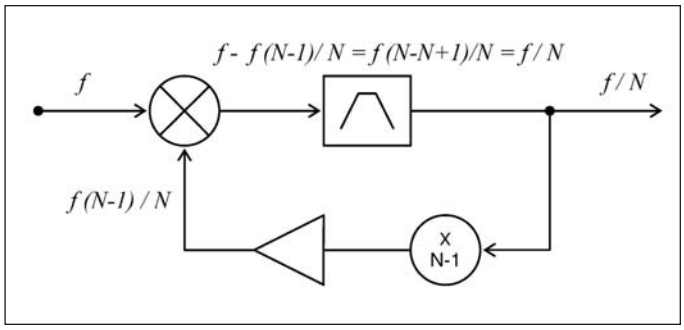

Figure 21 · Analog regenerative divider concept.

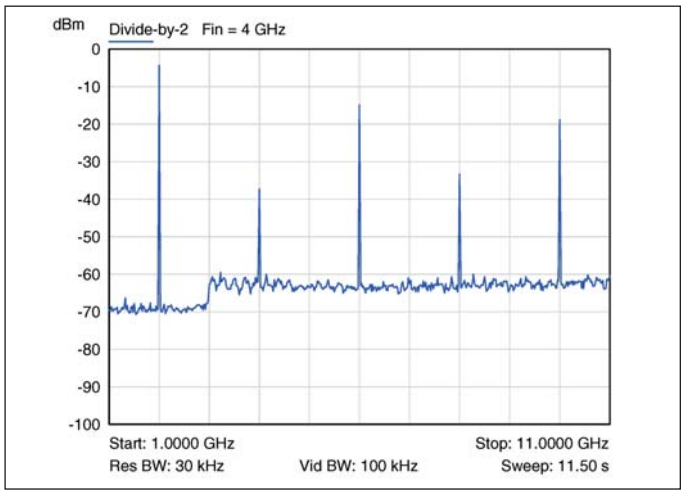

Figure 22 · Divider output spectrum.

Frequency Multipliers

Frequency multipliers are used to multiply reference signals or to extend synthesizer operating frequency bands. The device behavior and practical implementation is very well treated in [6, 17, 38]. It should be highlighted that a frequency- modulated signal is affected by the frequency multiplication process; i.e., phase noise and PM spurs are degraded at 20log$N$ rate, where N is the multiplication factor. Thus, the designer's primary concern is to avoid any extra degradation above the baseline of 20log$N$. From this point of view, passive, diode-based solutions are obviously preferred.

Frequency Dividers

A frequency divider is an essential part in a PLL synthesizer. It works in the exact opposite way that multiplier does, i.e., it brings phase noise and spurious improvement at the same 20log$N$ rate. Digital dividers (e.g., counters) are the most commonly used devices. The residual noise is probably the main concern since the divided sig-

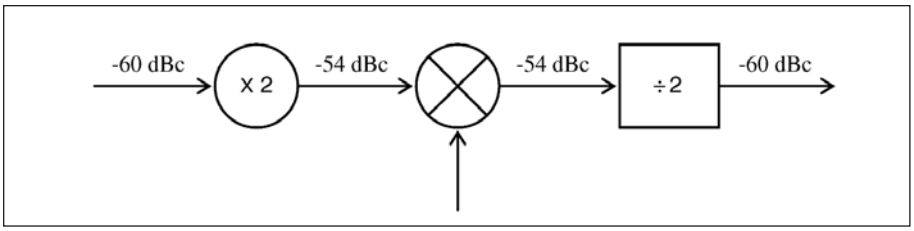

Figure 23 · Spur propagation through the signal chain.

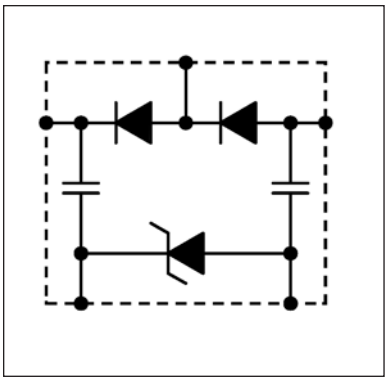

Figure 24 · Sampling phase detector.

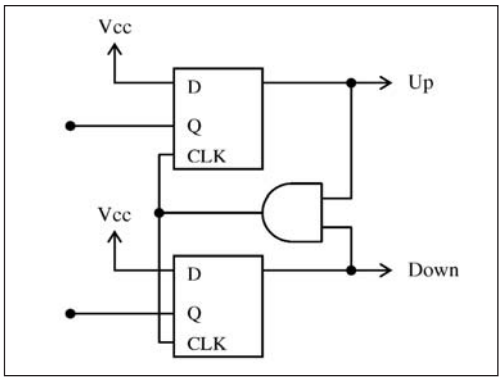

Figure 25 · Digital phase-frequency detector.

nal can easily hit into the divider noise floor. On the other hand, analog dividers (e.g. a regenerative scheme shown in Figure 21) provide the best noise performance but are rarely used due to their narrowband behavior as well as sensitivity to circuit parameters and signal level [39-41].

It is worth mentioning that the digital frequency divider tends to suppress even harmonics and accents odd products as shown in Figure 22. This is simply because the output of a digital counter is a square-wave signal that ideally contains odd harmonics only. This feature can be utilized to obtain fraction frequency multiplication and division coefficients (e.g., 3/2, 3/4, 5/4, etc.) that can be desirable in certain cases.

Mixers

Mixers are utilized in direct analog architectures as well as indirect schemes where frequency offsetting (mixing) is involved. In contrast to frequency dividers and multipliers, an ideal mixer provides a frequency shift without disturbing signal spurious and phase noise characteristics. A propagation of an FM-modulated signal with –60 dBc spurious level through a hypothetical, ideal multiplier-mixer-divider chain is illustrated in Figure 23 (it assumes that the signal has a pure close-in PM spur; practical scenarios are usually more complicated since AM-to-PM conversion and other effects can take place). Mixers are available in IC form and can be also built from discrete parts [38]. Similar to frequency multipliers, passive (diode-based) solutions are obviously preferable.

Phase Detectors

A phase detector compares two signals and generates a voltage, which is a measure of the phase difference between the signals [17]. The phase detector residual noise is one of the key parameter that affects the performance of a PLL synthesizer. From this point of view, a balanced mixer can be a good candidate for low-noise designs, especially if a high reference signal is used. A harmonic (sampling) mixer can be used as phase detector as well. It combines an SRD multiplier and mixing diodes in a common package (Figure 24) that leads to considerable reduction in synthesizer component count. It is worth mentioning, however, the sampling detector is very sensitive to circuit parameters; making one work properly is not trivial. The main disadvantages of the mixer-based phase detectors are relatively high undesired signals (e.g. reference harmonics and DC offset) and initial frequency acquisition problem when the PLL is out of lock.

A digital phase-frequency detector is a very popular and frequently used alternative since it provides a frequency-sensitive signal to aid acquisition. The detector can be constructed from discrete logic components as shown in Figure 25; it is also available in IC form (usually with an integrated charge-pump circuit). The main disadvantage of digital detectors is a higher residual noise in comparison with analog, mixer-based parts.

Integrated PLL ICs

Some vendors (e.g., Analog Devices, National Semiconductor and others) provide fully integrated ICs containing all necessary components required to build a whole synthesizer (Figure 26). A nice example is ADF4106 PLL IC from Analog

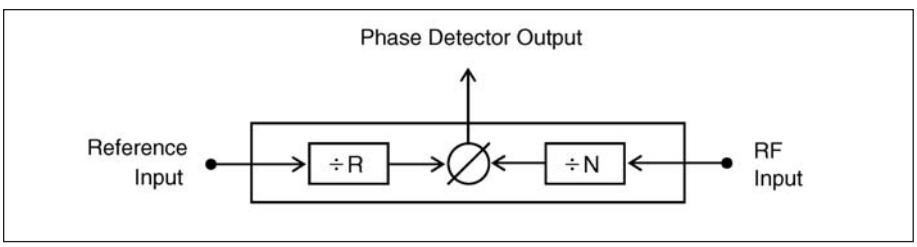

Figure 26 · Simplified depiction of integrated PLL functions on an IC.

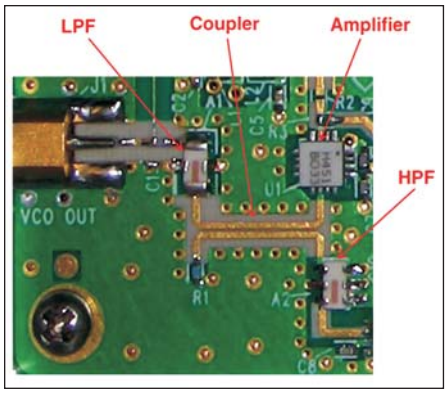

Figure 27 · Example of a PCB assembly.

Devices, which includes a digital phase detector with an integrated charge pump, RF and reference dividers, lock detector, and other circuits. All division coefficients can be programmed through a built-in 3-wire serial interface (clock, data, and chip select lines). The user can also program charge pump current (to adjust PLL bandwidth), change phase detector polarity (this feature can be very helpful if a frequency mixing employed), monitor frequency lock, or access some internal signals. The IC allows building a simple single-loop PLL synthesizer or can be used in more complex schemes.

Other synthesizer-oriented ICs may include more phase detector/divider sets to build a dual-loop synthesizer, fractional-*N* dividers, DDS, parallel interface for faster control, on-chip memory, etc.

Other Components

Depending on a particular architecture, frequency synthesizers can include many other components both active (e.g., amplifiers, switches, attenuators, phase shifters, etc.) and passive (e.g., resistors, capacitors, inductors, transformers, fixed attenuators, power splitters, couplers, filters, etc.) available in surface-mount packages.

Many passive components can also be printed directly on a PCB, such as the coupler and transmission lines in the assembly shown in Figure 27. The advantages of using printed components are obviously their low cost (just the PCB material itself) and more predictable frequency response due to the absence of package parasitics effects. The main disadvantage is that more "real estate" is required for some components in comparison with packaged versions. And finally, the simplest but very important element of any microwave design is a 50-ohm transmission line used to connect the mentioned above individual parts. The transmission line impedance depends on the line width as well as the thickness and dielectric constant of the

utilized PCB material. FR-4 works well at relatively low frequencies (a few GHz), while lower loss materials (such as Rogers 4003C) are preferable at higher frequencies. Also, it si preferred that a solder mask should be removed from high-frequency elements since it introduces extra loss and slightly changes the impedance. It is also worth mentioning that all packaged parts introduce discontinuity effects, which should be minimized (or compensated) to avoid any unexpected issues and provide a robust and reproducible design.

This article will be continued in the next issue, demonstrating the most important aspects of the synthesizer design process. Part 3 will show all design stages from a general block diagram to schematic, PCB layout, assembly, troubleshooting, testing, and documentation release. A simple, single-loop PLL architecture is used to discuss all aspects of the design process.

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