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A 1 to 2 GHz, 50 Watt Push-Pull Power Amplifier Using SiC MESFETs

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The performance advantages of silicon carbide (SiC) device technology aid in the design of broadband linear amplifiers such as this 1 to 2 GHz example

Because of their high RF power densities and correspondingly low intrinsic capacitances per watt of RF output power, silicon carbide (SiC) MESFETs are becoming increasingly popular in very wideband amplifier applications. This article describes the design and realization of a single-stage linear power amplifier covering the 1,000 to 2,000 MHz frequency range. The amplifier uses a 3rd generation SiC MESFET produced by Cree Inc. in a brazed ceramic package having a copper-molybdenum-copper flange. The amplifier uses two transistors in a push-pull configuration together with commercially available Anaren Xinger® baluns. Thus, each half of the amplifier is matched at its input and output to 25 ohms—this makes matching the transistors over an octave bandwidth easier and more efficient when compared to matching a single-ended amplifier of twice the power level to 50 ohms. Also the push-pull configuration affords higher harmonic and intermodulation performances as well as superior thermal management, because the sources of heat from the two transistors are spread over a larger area when compared to a single device. The amplifier was designed using Cree's proprietary large-signal MESFET model employing the Agilent ADS simulator. The basic specification for the amplifier is shown in Table 1.

Large-Signal Model Validation

This octave-band push-pull amplifier was designed using the relevant Cree SiC MESFET large-signal transistor model, which models both the semiconductor die as well as the ceramic package. The transistors used in this design have a gate periphery of 18 mm and nominal output powers of 30 watts at 1 dB gain compression. These transistors are third generation showing improved performance over second-generation devices in terms of gain and drain efficiency. They also feature improvements in die layout and the introduction of via'd source connections.

Frequency range:	1 to 2 GHz
Small signal gain:	10 dB min.
Power output at 1 dB compression:	50 watts min.
Drain efficiency target at 1 dB compression:	25%
Intermodulation distortion at 50 watts min. PEP:	–30 dBc
Waveform types:	GMSK, PSK, QAM, OFDM, AM, FM
Test with W-CDMA waveform with ACPR goal:	–36 dBc
Nominal drain voltage:	48 volts
Case operating temperature:	–40 to +70°C
Operating junction temperature:	200°C max.

Table 1 · Basic specifications for a single-stage linear push-pull power amplifier covering the 1,000 to 2,000 MHz frequency range.

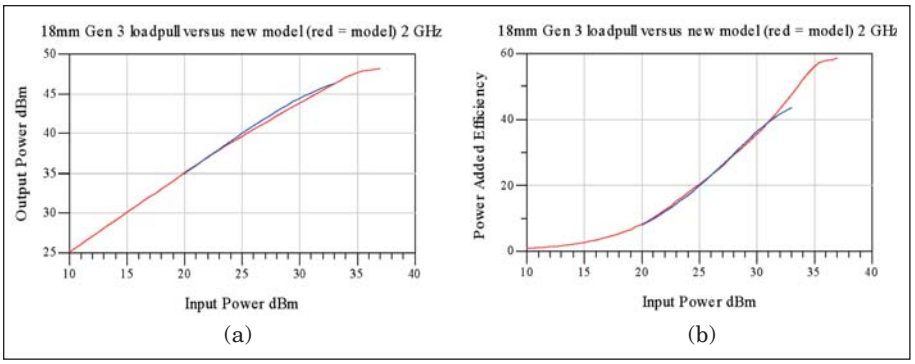

Figure 1 · Comparison of modeled and measured results for output power (a) and power added efficiency (b).

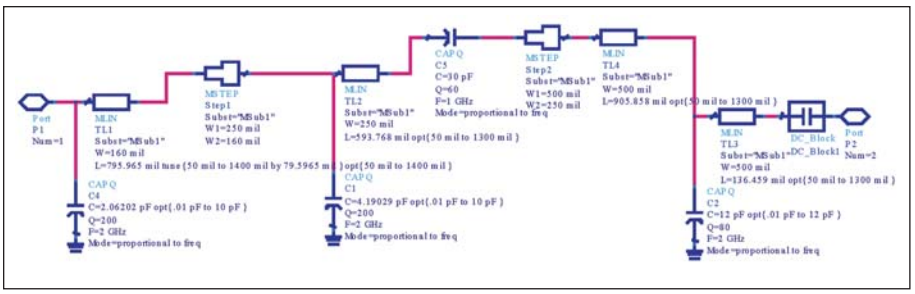

Figure 2 · Input network, 25 ohms to gate input impedance.

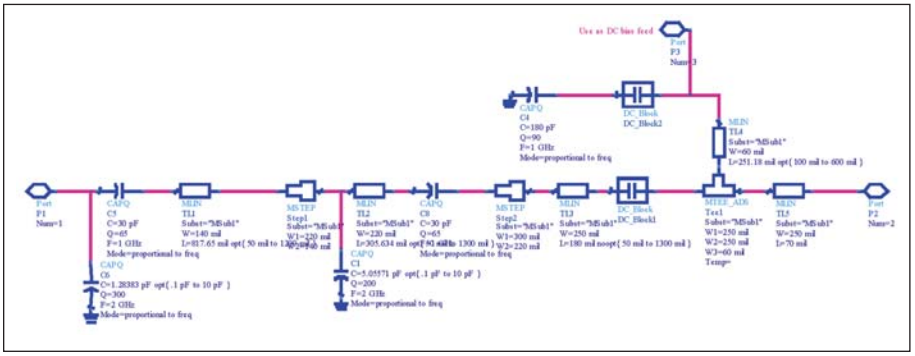

Figure 3 · Output network, 25 ohms to drain output impedance.

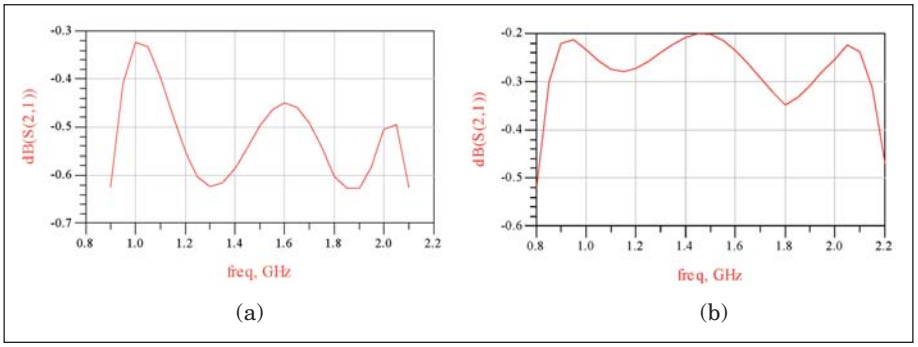

Figure 4a · (a) Input network response from 25 ohms to MESFET gate, and (b) output network response from 25 ohms to MESFET drain.

Therefore, as part of the amplifier design procedure, the large-signal model was validated against measured characteristics in a Maury load pull tuner system. Figure 1 shows agreement between the modeled and measured output versus input power characteristic, and the power added efficiency as a function of single tone input power characteristic, for a nominal Class A/B quiescent drain current of 750 mA. Both the modeled and measured results were provided with optimum source and load pull impedances at 2 GHz for gain and output power respectively. Small signal gain (under such narrow-band tuning) is 15 dB with a P_{1dB} output power of greater than 32 watts with a corresponding PAE of 42%.

Input and Output Impedance Matching Networks

The input and output matching networks were synthesized initially by treating the input and output impedances of the MESFET as passive circuits with equivalent real (resistive) and imaginary (capacitive) parts. The input-matching network (Fig. 2) consists of four distributed sections providing a broadband match from 25 ohms to the gate impedance over the 1,000 to 2,000 MHz frequency range. Similarly, the output-matching network (Fig. 3) consists of four distributed sections allowing a broadband match from the drain impedance to 25 ohms. In particular, the output matching network was designed to transform the drain impedances for maximum output power over the frequency range. Figures 4a and 4b show the insertion loss of these matching networks transforming from the gate and drain impedances. The input matching network has an average loss of 0.5 dB while the output matching network loss is kept to better than 0.3 dB. The ADS schematic of a complete 25 ohms in/out amplifier (one half of the push-pull pair) is shown in Figure 5. The small-signal gain of

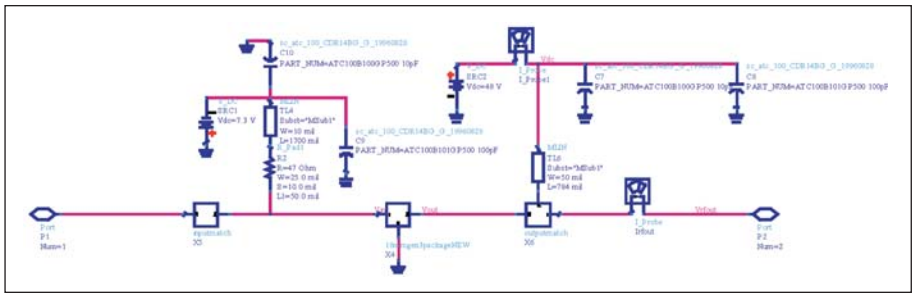

Figure 5 · Simulation schematic for the complete 25 ohm in/out amplifier (half of push-pull pair).

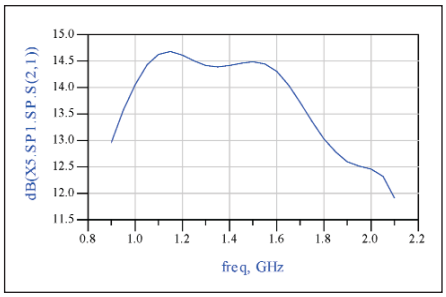

Figure 6a · Small signal gain prior to any optimization or adjustment.

the amplifier prior to any further optimization or adjustment is shown in Figure 6a, indicating a minimum gain of 12 dB over 1 to 2 GHz. This gain will decrease by more than 1 dB as the output power is increased because of gain compression and self-heating in the transistor due to finite drain efficiency. Figures 6b and 6c show the power characteristics and power added efficiency of the 25 ohm amplifier at 1 and 2 GHz respectively.

The Complete Amplifier

Two of the single-ended amplifiers were combined with off-the-shelf Anaren Xinger baluns (part number 3A525) as shown in Figure 7. The simulated small-signal gain of the complete amplifier is shown in Figure 8.

The simulated harmonic performance of the complete amplifier is shown in Figure 9 for a fundamental carrier frequency of 1 GHz. Note that the 2nd order harmonic is very low due to push-pull action. In addition all higher order harmonics are low due to the finite bandwidth of the amplifier.

Figure 10 shows the third-order 2-tone intermodulation distortion as a function of output power at 1, 1.5 and 2 GHz. Note that further optimization was required to achieve the –30 dBc requirement at the low end of the band. In order to achieve lower intermodulation distortion some series-gate resistance was added (as shown

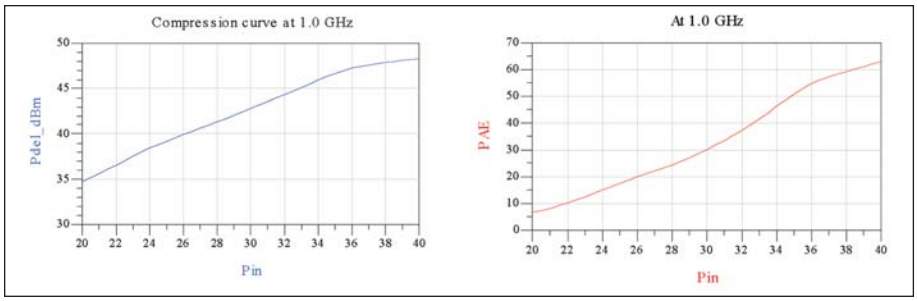

Figure 6b · For each 25 ohm amplifier stage.

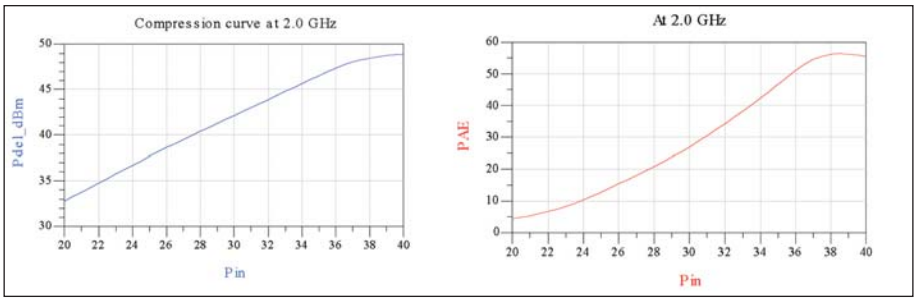

Figure 6c · For each 25 ohm amplifier stage.

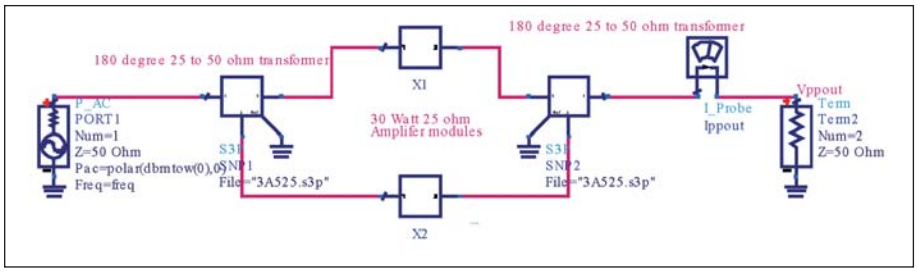

Figure 7 · Schematic diagram of the combined amplifiers.

in Fig. 11) which also improved S_{11} and stability but decreased gain by 1 dB or so.

Initial Performance Characteristics

The RF matching transmission lines, biasing networks, etc., were produced on softboard high dielectric PCB (Rogers 4350) having a dielectric constant of 3.48 and thickness of 20 mils. The PCBs are attached to an aluminum back-plate using multiple screws with integrated bias components. A first iteration board design

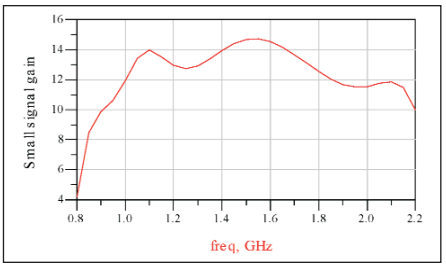

Figure 8 · Simulated gain of the complete push-pull amplifier.

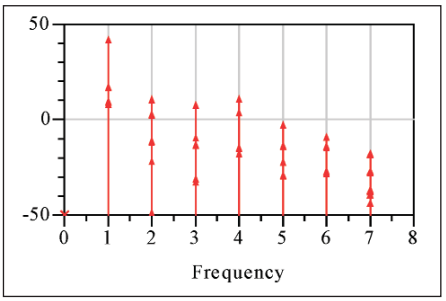

Figure 9 · Simulated harmonics of the complete push-pull amplifier.

(Fig. 12) resulted in small signal gain of >9 dB; saturated output power of greater than 47 dBm and PAE of >20% over 1.2 to 2.2 GHz. Performance at the low frequency end of the band is limited by the balun characteristics.

Investigations of the performance of the first iteration design resulted in the following conclusions:

1) The self-resonant frequencies of the tuning, bias, bypass and blocking capacitors have to be chosen carefully to avoid unwanted effects in the band of interest. This resulted in using smaller value capaci-

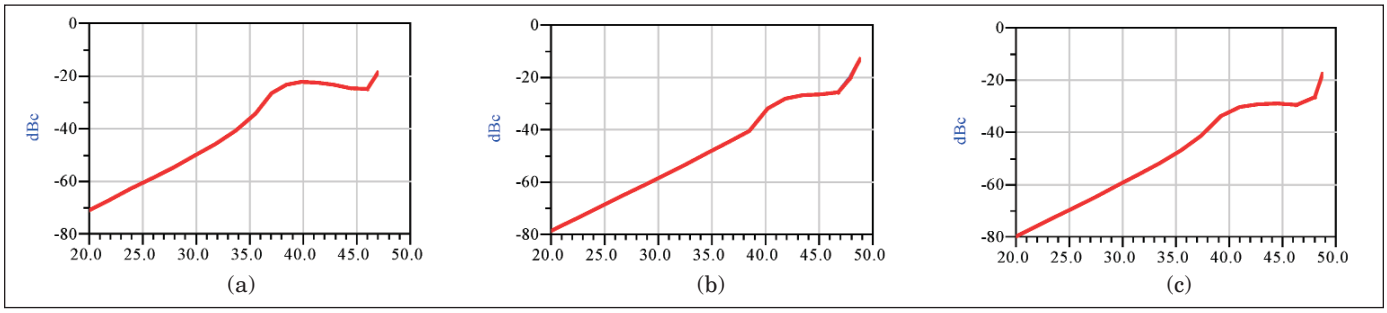

Figure 10 · Output power in dBm, both tones, for the complete push-pull amplifier at: (a) 1.0 GHz, (b) 1.5 GHz, (c) 2.0 GHz.

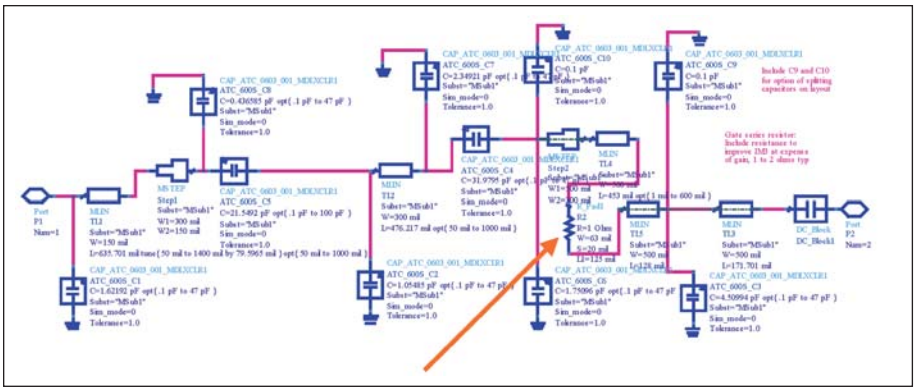

Figure 11 · Series resistance added to the gate circuit (arrow) improves IM3, provides stability, and lowers gain by 1 dB.

tors in parallel in many instances. Extensive use was made of the Modelithics substrate scaleable ATC capacitor models;

2) The Anaren Xinger baluns limit the amplifier performance below 1.1 GHz and above 2.5 GHz, so more optimum amplifier performance could be obtained with custom baluns;
3) The input matching network and package parasitics limit the amplifier performance above 2.3 GHz;
4) Improvements to grounding near the package gate leads was required; and
5) Optimization and tradeoff of the small-signal gain, 1 dB compressed output power, linearity and stability was made.

Final Design and Performance

Some improvements were made to the design by modifying the passive circuit models to more closely match the realized amplifier performance. The final board layout and assembly is shown in Figure 13. Improvements were also made in the transistor (type 440193) package model to take into account effective die-to-ground source inductance, package mounting and interfacing to the PCB board. Comparison of the measured and modeled small-signal gain over 800 to 2400 MHz is shown in Figure 14.

Dependent on frequency the 2 tone PEP output power achieved was between 49 and 64 watts with IM3 of between –29 and –38 dBc. Optimum results for IM3 were achieved at a quiescent drain current of 1200 mA per transistor. Typically (at 1.6 GHz) IM3's were –32 dBc at 55.5 watts PEP with drain efficiency of 25%.

Under the same quiescent drain current conditions (1200 mA per transistor) the complete amplifier was tested for linearity under W-CDMA 3GPP test model 1, single carrier with 64 DPCH test signal conditions. The required adjacent channel power (ACPR) specification was –36 dBc at ±5 MHz offset (applications for such amplifiers include reverse link communications). At this ACPR level, the average output power level, at a carrier frequency of 1600 MHz, was 20 watts (43 dBm) (Fig. 15) with a corresponding gain of 10 dB and a drain efficiency of 21%.

Thermal Performance

The worst-case conditions for the

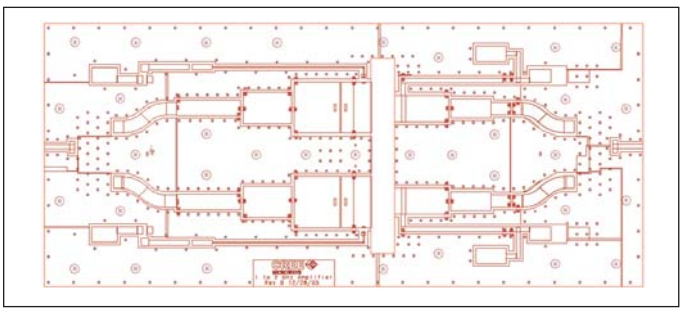

Figure 12 · Board layout for the SiC amplifier.

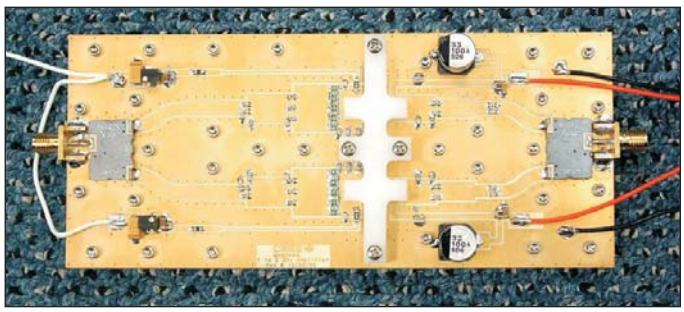

Figure 13 · Photo of the SiC amplifier.

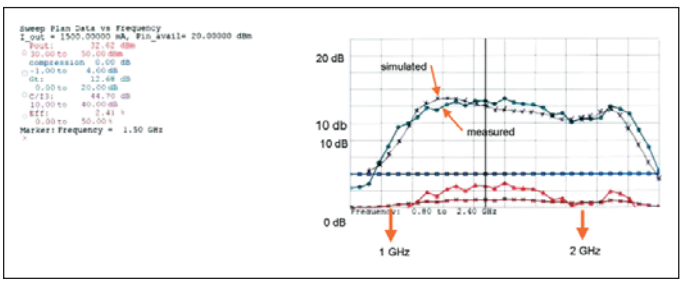

Figure 14 · Modeled/measured gain comparison.

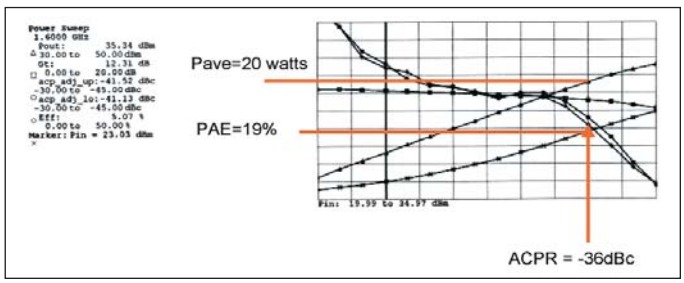

Figure 15 · Test result showing 20 W at –36 dBc ACPR.

complete amplifier were measured at 1950 MHz at a quiescent drain current of 1200 mA. Under such worst case conditions the average RF output power per transistor was 16.2 watts (42.1 dBm) with a corresponding dissipated power per transistor of 55 watts (drain efficiency of 23%). Since the thermal resistance of the package is 1.8°C/watt the temperature rise above case temperature is 99°C resulting in a transistor junction temperature of 169°C at a case temperature of 70°C. This is within the original specification limit of 200°C. The corresponding MTTF per transistor (at a junction temperature of 169°C) is 100 million hours based on measured reliability data.

Conclusions

This article has given a summary of the design approach, using large-signal SiC MESFET and passive component models, adopted for an octave bandwidth push-pull 50-watt power amplifier. The design provided an amplifier with gain greater than 10 dB over 1 to 2 GHz and drain efficiencies averaging 25% at P_{1dB} output power. The push-pull design not only provided a convenient method of broadband matching but also supplies the well-known advantage of even order harmonic rejection as well as improvements to intermodulation products compared to single-ended designs. The amplifier also exhibits significant linear performance and was tested using W-CDMA signals under reverse link conditions.

Author Information

Ray Pengelly gained his BSc. and MSc. degrees from Southampton University, England in 1969 and 1973 respectively. Ray has worked for the Plessey Company, Tachonics Corporation, Compact Software, and Raytheon. Currently, he is employed by Cree Inc. and is responsible for the business development of RF and wireless products and applications using SiC MESFET and GaN HEMT devices. He can be reached by email at ray_pengelly@cree.com, or by phone at 919-313-5567.

Carl Janke gained his BSEE in 1982 from the University of Florida. He was employed by Motorola from 1982 to 1987, working in pocket paging and 2-way handheld radio. In 1987 he moved to GE Mobile Radio (later GE Ericsson Mobile Communication) working on 2-way radio communication mobiles, handhelds, and base stations. He was employed by Ericsson from 1994 to 2001 as an RF Design Manager in the cellular phone design group. In 2001 Carl moved to Cree, where he has worked on SiC MESFET and GaN HEMT product development and applications engineering. Ha can be reached by email at carl_janke@cree.com or by phone at 919-313-5849.