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Design Study of a High Efficiency LDMOS RF Amplifier

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In this article, the author discusses which mechanisms can explain the observed high efficiency performance of a 5 watt, 150 MHz power amplifier using an LDMOS transistor

High efficiency RF power amplifiers have always been of interest to RF engineers. A large volume of literature on the subject, ranging from theoretical analyses to practical circuit designs, has been published over the years [1-4]. On the theory side, most analyses utilized considerably simplified models for the devices and circuits to make the mathematics involved manageable. These simplifications are necessary, and the analytical results based on them do reveal certain aspects of how to achieve high efficiency. However the actual device and circuit behaviors are often significantly more complex than the idealized assumptions used in the analyses, and several different effects can take place simultaneously at a real circuit operation condition. As a result, the characteristics of practical RF PA circuits do not always correlate well with the analytical predictions.

This article presents the design and development of a high efficiency RF PA design from the perspective of a practicing RF engineer. The PA evolved from a development project; a 5 W, 150 MHz design. A drain efficiency of 87% was achieved at the required power level and frequency. The circuit employs a commonly used matching network for practical PA circuits, which consists of serial transmission lines and shunt capacitors. Several controlled experiments were carried out to investigate the possible mechanisms for improved efficiency. It is concluded that the observed high efficiency is achieved by a combination of the clipping effect and appropriate harmonic tuning conditions.

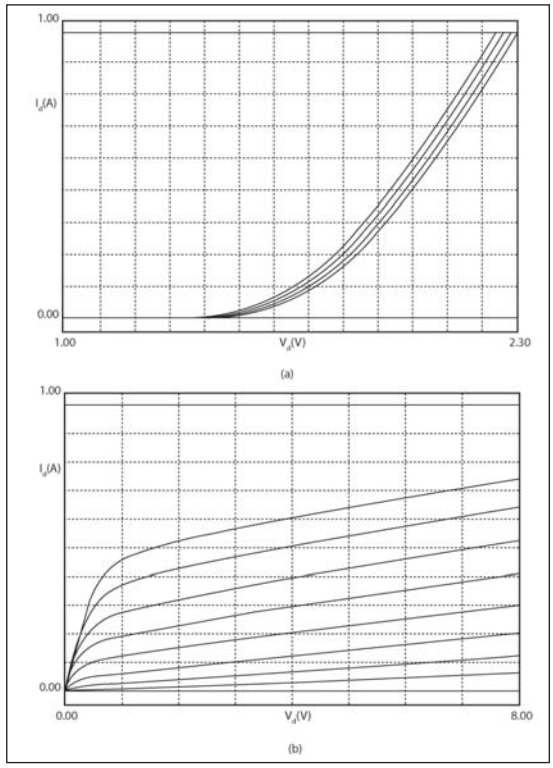


Figure 1 · DC characteristics of the Renesas NE5511279A: (a) Transfer curves; (b) I-V curves.

Circuit Description and Performance Data

The device used in this work is Renesas Electronics' medium power LDMOS transistor, NE5511279A. It has 10 W power capability and typically operates at a drain voltage of 7.5 V. It is usable for a frequency range up to 1 GHz or slightly higher. Figure 1 shows the DC characteristics of NE5511279A.

The circuit schematic and a photo of the actual circuit board are shown in Figures 2

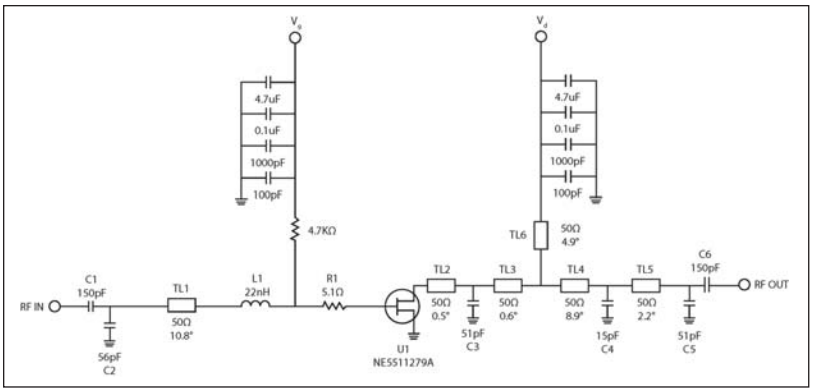


Figure 2 · Schematic of a high efficiency 5 W, 150 MHz power amplifier using NE5511279A.

and 3. The output matching is realized by several sections of 50-ohm transmission line and shunt capacitors. The transmission lines, when used as the series components for impedance transformation, have the advantage of low insertion-loss and low cost compared to inductors. For the same reason a section of PCB trace is often used for the drain bias circuit instead of a bulky and expensive inductor. At 150 MHz, however, the conventional λ/4 transmission line for the DC feed is too long to implement. In this work the DC feed line is a much shorter PCB trace (labeled TL6 in the schematic). Consequently, the drain bias circuit becomes part of the output matching network. TL6 is equivalent to a shunt transmission line and provides an additional inductive element for the matching circuit. It reduces the required lengths of the series transmission lines (TL2 though TL5), thus making the total PCB size smaller.

At the input, an inductor in combination with a transmission line and a shunt capacitor is used to realize the required impedance transformation. A 5-ohm series resistor is used at the gate to improve the stability margin. The amount of gain reduction due to this gate resistor is insignificant in this case. The component values and locations are first determined according to the prior knowledge for a typical PA design and then finalized through bench tuning. The input circuit is optimized to provide good input return loss (>15 dB) at the operating power level, while the output matching is tuned for best efficiency at the desired output power level.

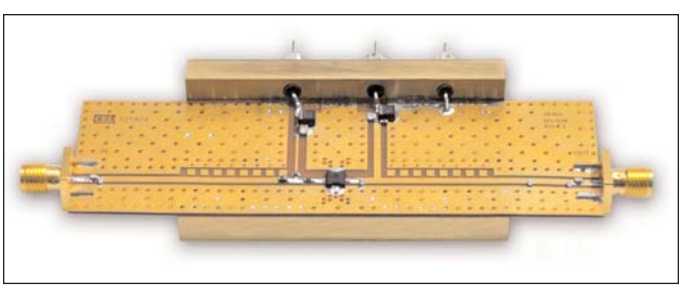


Figure 3 · Photo of the constructed PA circuit board.

The output power, drain efficiency and power added efficiency are plotted as a function of input power in Figure 4. It can be seen that quite high efficiencies, 87% for drain efficiency and 84% for power added efficiency, have been achieved with this relatively simple and conventional matching configuration. The remainder of this article will focus on the possible mechanisms for the observed high efficiency.

Background

Traditionally high efficiency power amplifiers are categorized into classes, such as class AB, B and C amplifiers, class F and inverse class F amplifiers and class E amplifiers. Each class corresponds to a specific mechanism for achieving high efficiency. From class A to class AB, B and C amplifiers, the progressive improvement in efficiency is achieved with the reduced conduction angle. In this category of amplifier, the waveform of drain current is assumed to be a truncated sine wave. The Fourier analysis of this waveform shows that the ratio of the fundamental to DC component increases as the conduction angle is reduced, resulting in increasing efficiency with the reduction of conduction angle [3]. In class F amplifiers the drain current is assumed to be a half sine wave (or class B condition) and the drain voltage is a square wave. This pair of waveforms does not have overlap in time domain and have zero overlap for all harmonics in frequency domain, thus yielding a perfect efficiency [2]. This perfect condition only occurs at the conduction angle π, and the efficiency drops when the conduction angle increases from that point. To support a voltage waveform of square wave the drain termination is required to be infinite and zero at odd and even harmonics, respectively. In actual circuit implementation, this requirement is usually realized by a drain load that is a short at the second

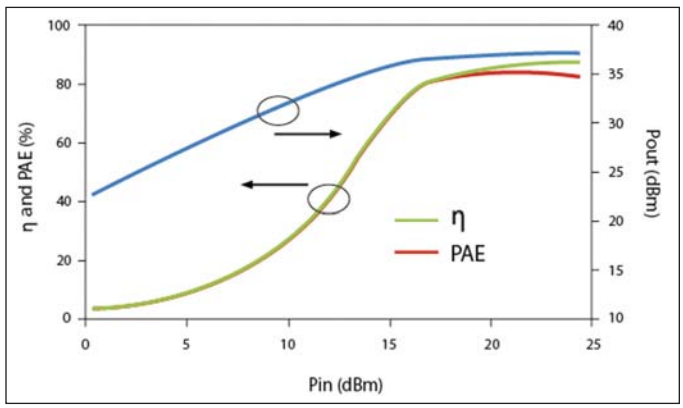


Figure 4 · Output power, P_{out}, drain efficiency, η and power added efficiency, PAE, versus input power, P_{in}. drain voltage, V_d = 7.5 V, quiescent current, I_q = 800 mA.

harmonic and open at the third. Thus, the design of a class F amplifier is basically a task of finding a network that transforms the 50-ohm broadband termination to the desired impedances at three frequencies of fundamental, second and third harmonics. Usually this is done with multiple transmission lines of specified characteristic impedance and electrical length [2].

For inverse class F, the concept is the same as that of class F, only the waveforms for current and voltage are switched. Because of the equivalence of the current and voltage in the formulation the inverse class F amplifier is also expected to have a perfect efficiency when the voltage waveform is a half sine wave. Similarly, the drain termination needs to be infinite at even harmonics and zero at odd harmonics in order to achieve the desired voltage waveform. Because the current waveform is assumed to be a square wave, in this case the efficiency in principle is no longer dependent on the quiescent current. This is a significant advantage of inverse class F in practical circuit designs because it allows high efficiencies at higher bias conditions [5].

Another category of high efficiency amplifier is the class E amplifier, which uses a very different concept to achieve high efficiency. In class E amplifiers the key elements are the transistor, which is modeled as a switch, and a shunt capacitor. The capacitor charges (when the switch is open) and discharges (the switch close) during each RF cycle. The rest of the circuit provides a condition such that only the power at fundamental frequency is delivered at the load, and the energy associated with discharging from the capacitor to the switch is zero. This way a 100% efficiency can be achieved [1]. A special circuit configuration along with a set of well-specified component values are required to realize the class E operation. Hence the circuit of this work does not fall into this class of high efficiency amplifier. Finally, it has been known that the efficiency can be increased by increasing the output load resistance from the value for optimal output power condition [6]. The mechanism for this efficiency improvement is the increased voltage swing that results from the lowering of the knee voltage. It is discussed in the next section.

Load Resistance and Its Impact on Efficiency

The effect of load resistance on efficiency can be understood by examining the two load lines that correspond to two output load resistances, as shown in Figure 5. For the simplicity of discussion, it is assumed in the plot that the DC current is set at the half point of the saturation current. Thus, the ratio of the fundamental frequency current to the DC current is the same for the two cases (an equivalent assumption is the conduction angle is the same). Also assumed are ideal I-V curves. It is clear from the plot that the high-slope load line (small resistance) corresponds to a higher saturation current I_{sat1}, thus higher output power. On the other hand, the low-slope load line (large resistance) allows more voltage swing ($V_{dc} - V_{k2}$ vs. $V_{dc} - V_{k1}$) thus better efficiency. For a general case the analysis is quite complex even for the idealized case because of the interactive nature of voltage and current involved. But it is not difficult to recognize that V_k is essentially a DC offset that contributes to the DC power consumption but does not allow RF swing. Therefore, efficiency can be improved from any technique that reduces V_k. In fact, in one of the publications [7] on the comparison between the Class F and inverse Class F amplifiers, the authors stated that the inverse Class F has higher efficiency than Class F. Examination of their formulation reveals that the benefit of inverse Class F in efficiency is strictly from the lower V_k assumed in the model.

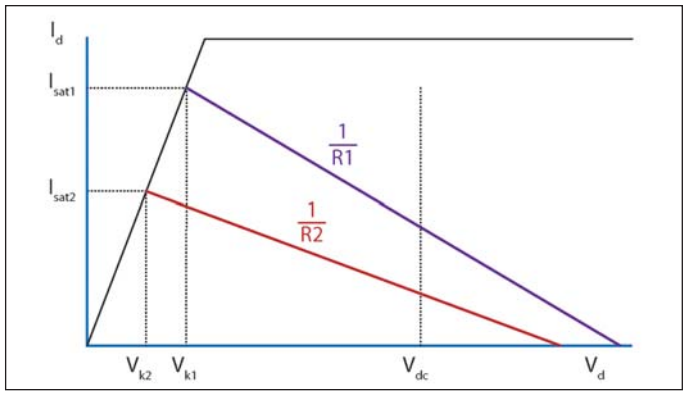
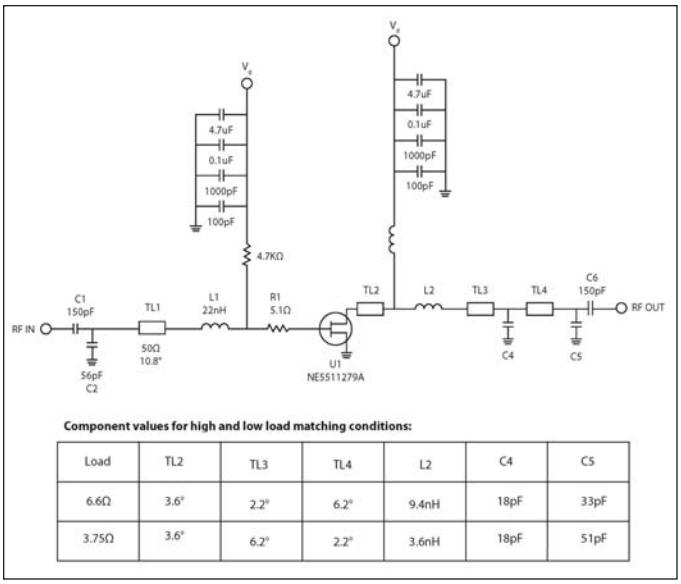


Figure 5 · Illustration of the effect of load line on efficiency. R1 < R2.

In the circuit described in Figure 2 the high efficiency was achieved with a high output load resistance and at the expense of output power. To verify the effect of the load resistance on the efficiency, a designed experiment was carried out in which two additional well-specified load impedances were used to compare the circuit performance. In the experiment, the matching networks were designed to transform the 50-ohm termination to nearly perfect resistive loads so that any possibility of unintended effects associated with the reactive part of the load impedance was minimized. Also, to reduce variables and simplify the design a choke inductor was used to isolate the RF circuit from the DC bias circuit, and a serial inductor was used to provide the necessary inductive element to transform 50 ohm to the desired resistive value. The actual circuits are shown in Figure 6. The inductor values were individually determined for this experiment. The matching networks for the target value of load resistance were designed using simulation and verified with actual *S*-parameter measurements. Figure 7 shows the Smith chart plots for the three load conditions used in this work



Component values for high and low load matching conditions:

Load	TL2	TL3	TL4	L2	C4	C5
6.6Ω	3.6°	2.2°	6.2°	9.4nH	18pF	33pF
3.75Ω	3.6°	6.2°	2.2°	3.6nH	18pF	51pF

Figure 6 · Schematic of circuits for two additional load conditions.

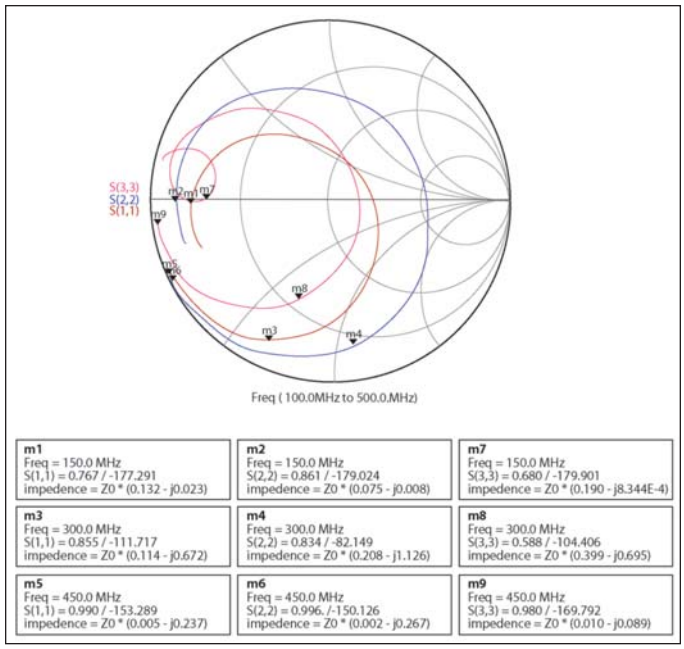


Figure 7 · Smith chart plots for three load impedances up to 3rd harmonic frequency.

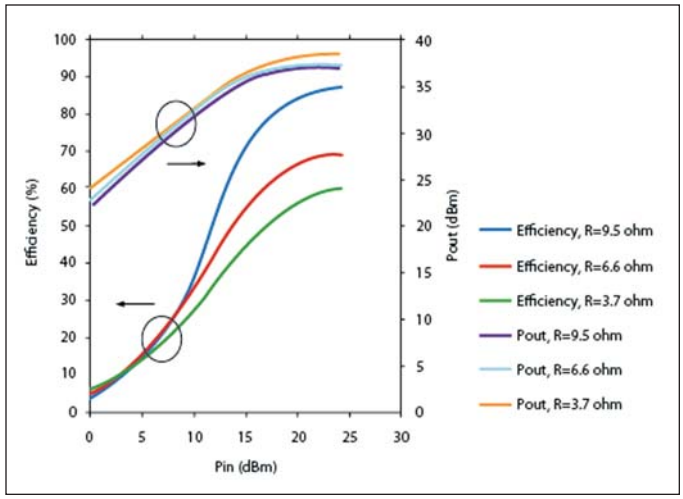


Figure 8 · Output power and efficiency vs. input power for three load conditions.

for a frequency range up to the third harmonic. The output capacitance of the transistor is estimated to be 35 pF and is included in the simulation. The parasitic components associated with packaging are ignored because of the relatively low operation frequency. The impedances at f_0, $2f_0$ and $3f_0$ are marked on the curves for each circuit. It can be seen that the fundamental load impedances are almost purely resistive at 3.75, 6.6 and 9.5 ohms, respectively, for the three matching circuits. The measurement results for output power and efficiency as a function of input power are shown in Figure 8 for the three load conditions. It is clear from the plot that the efficiency is increased with load resistance, while the output power is optimized at lower load resistance. In fact, from experiments the load resistance seems to be the most sensitive parameter that affects efficiency. Although the reduced V_k as a mechanism for the improved efficiency is consistent with the trend displayed in the measurement data, it alone is not sufficient to provide a quantitative account for the amount of efficiency improvements observed in experiments. Furthermore, even at the perfect condition of $V_k = 0$ the efficiency is not necessarily as high as 85%. Some other mechanisms are certainly also involved in this case.

For the convenience of discussion, in the remainder of this article only two load conditions, 3.75 and 9.5 ohms, are used for the comparison purpose. They will be referred to as high power and high efficiency conditions, respectively.

Conduction Angle and Clipping Effects

The most frequently discussed category of high efficiency amplifiers in textbooks is perhaps the class AB, B and C amplifiers in which high efficiency is achieved through reduction of the conduction angle. The conduction angle is a convenient parameter for analyses but cannot be directly controlled or easily measured in a real circuit. Because the conduction angle, θ_c is related to the quiescent current I_q and the RF current amplitude I_a by a simple equation, $\cos\theta_c = -I_q / I_a$, in experiments the quiescent current and input power level are often used as two variables to study the effect of the conduction angle on the circuit performance. For this purpose, the circuit

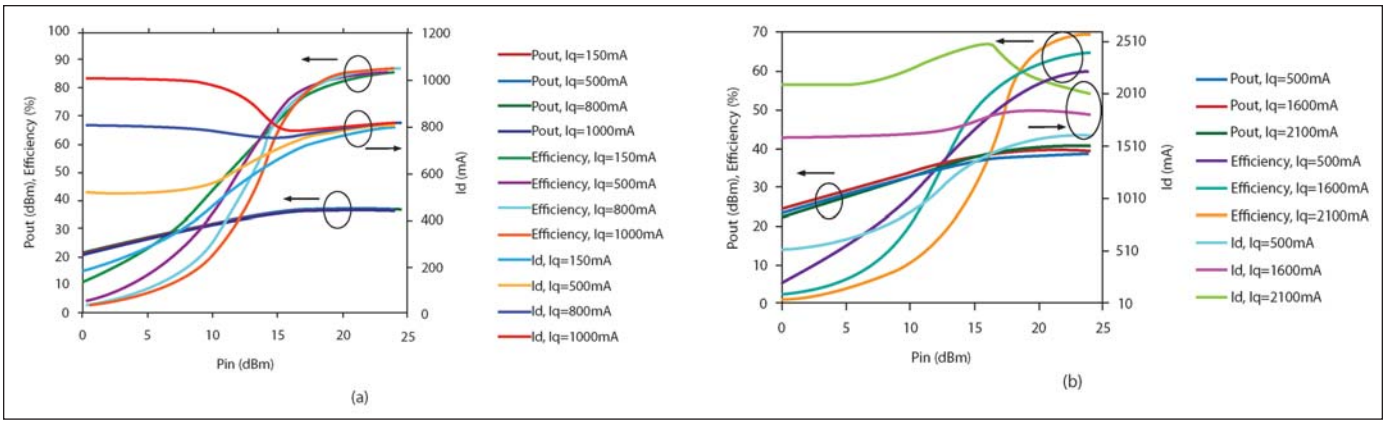


Figure 9 · Dependence of output power, efficiency and drain current with input power. (a) high efficiency load; (b) high power load.

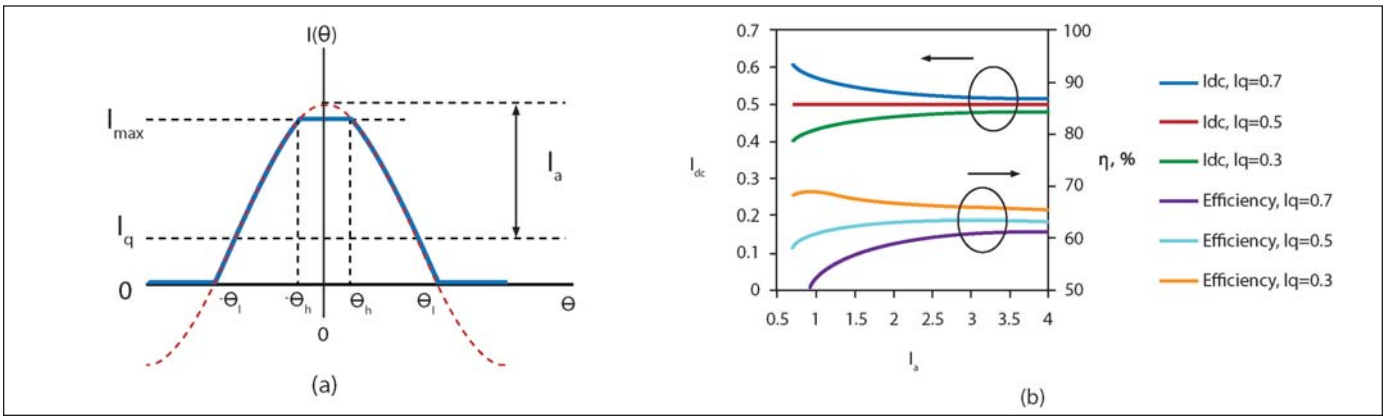


Figure 10 · Clipping effect. (a) Dashed line: undistorted waveform, sine wave plus DC; Solid line: the waveform is limited to the range (0, I_{max}); (b) DC component, I_{dc} and efficiency, η of the waveform in (a) as a function of amplitude, I_a for three I_q values. I_{max} is normalized to 1.

performance parameters of output power, drain current and efficiencies are measured as a function of input power at different quiescent currents for the three load conditions discussed in the previous section. Figure 9(a) and (b) show the results for high efficiency and high power load conditions respectively {1}.

A noticeable feature shown in Figure 9(a) is that for the case of high efficiency load condition all curves for each parameter measured virtually collapse into one at high input power levels, indicating the independence with the quiescent current (or conduction angle). In Figure 9(b) the efficiency is somewhat dependent on the quiescent current, but in an opposite way from what the theory of reduced conduction angle operation predicts: at high driving levels the efficiency actually goes up as the quiescent current increases. These observations provide strong evidence that the measured high efficiencies are not achieved from conduction angle reduction. This seeming contradiction between the theory and measured data can be explained by the fact that in theory the current waveform (truncated sine wave) is assumed to be free from distortion at the top portion of the RF cycle, whereas in actual circuits some distortion or clipping effects occur during the upper swing of the drain current once the driving level reaches a certain level. The fact that the DC currents at high quiescent current conditions are actually pushed down at high input powers, as shown in Figure 9, confirms the occurrence of the clipping effect.

Clipping used in this article refers to an effect that limits the drain current on the upper half swing. Other terms such as *overdriven* and *saturating* are also used in the literature for the same concept [3, 4]. Figure 10(a) shows a waveform that is originally a sinewave plus a DC offset and is clipped at the top due to a hard limit at I_{max}. It is straightforward to see how the clipping effect can increase the efficiency in certain conditions. Consider a case where the drain current is limited to a range between 0 and I_{max} and the quiescent current I_q is set at 1/2 I_{max} (the red curve in Figure 10(b)). At low driving levels, the waveform remains undistorted.Once the current

reaches I_{max} (and 0 at the same time in this case) clipping occurs. Further increasing the driving level widens the clipping region. Clearly, the fundamental amplitude increases with the driving level while the DC level is fixed at 1/2 I_{max}. Thus, the efficiency can be continuously increased after clipping. For a general condition, the waveform after clipping as shown in Figure 10(a) is described by:

$$I = \begin{cases} I_{\max} & |\theta| < \theta_h \\ 0 & \theta_l < |\theta| < \pi \\ I_a \cos\theta + I_q & \theta_l < |\theta| < \theta_l \end{cases} \quad (1)$$

where Ia is the amplitude of the undistorted current waveform and the condition $I_a + I_q > I_{max}$ needs to hold for the clipping at the top to happen. Fourier analysis of Eq. 1 yields the DC and fundamental components, I_{dc} and I_1. As in the standard analyses of class AB amplifiers, the voltage swing, V_1 is assumed to be the same as V_{dc}. Then the efficiency is simply, $\eta = V_1 I_1 / 2V_{dc} I_{dc} = I_1 / 2I_{dc}$. Figure 10(b) shows how I_{dc} and η vary with I_a at three I_q conditions. It can be seen that the DC current converges to 1/2 I_{max} and the efficiency converges to 63%, both are expected because they are the values for square waveform, which is the limiting case for Eq. 1.

While the simple model for the clipping effect described by Eq. 1 captures certain features observed in the experiments, the relevance of this model, which is characterized with three parameters, I_q, I_a and I_{max}, to the actual circuits still needs to be examined. Among the model parameters, I_q is obviously related to a parameter in experiments. Accurate mapping of I_a to the input power, which is known in the experiments, is nontrivial .It involves conversions of the input power to the gate voltage and the gate voltage to the drain current with each conversion depending on the input power itself. Nevertheless, I_a still can be used as an input power parameter in the analysis to show the general tread of the circuit behavior as a function of the input power. The origin of the current limit I_{max} is worth a more detailed discussion. In the literature I_{max} is often cited as being imposed by the device physics. In reality the drain current of a transistor indeed reaches saturation at a certain point for a variety of reasons. A detailed account for the saturation current was provided by Jang et al. [8] for LDMOS transistors. But usually the drain current approaches to saturation in a more gradual manner rather than a sharp limit. Furthermore, perhaps more relevant, manufacturers usually do not provide the saturation drain current as a data sheet spec; instead the maximum current rating is listed. The maximum rating is mainly from the consideration of device reliability rather than performance characteristics. For example, the maximum current rating for NE5511279A is 3A, but the actual current can significantly exceed this max rating. For these reasons the saturation current observed in a PA circuit is often determined by the load line selection where the current swing is limited by the limit on the voltage swing rather than the intrinsic saturation drain current.

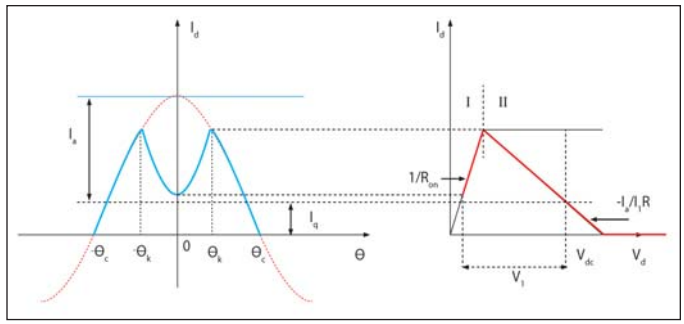


Figure 11 · Drain current saturation model. The left is the waveform derived from the ideal I-V curve on the right and Eq. 4-6. The parameters are: I_a = 3; I_q = 1; V_{dc} = 7.5 V; R_{on} = 1Ω; R = 5Ω. The red line on the right is the trajectory in the (I_d, V_d) plane for one RF cycle.

Due to the complicated nature of the interaction between the drain current and voltage once nonlinear effects are included, it is difficult to work out an analytical solution on the clipping effect. An attempt was made in a significantly simplified model [1]. In this article the same formulation is followed with some changes on notations. The numerical results are presented in a different way to make it more relevant to the discussion in this article. Only the outline of the analysis is provided, and the detailed algebra is left out.

In this model, the drain current I_d can be divided into two regions, region I and II (called linear and saturation regions respectively in the literature) as shown in Figure 11. In the region II, I_d is controlled only by V_g and is independent on V_d. If a constant transconductance is assumed the drain current in this region can be written as :

$$I_d = I_a \cos\theta + I_q = I_a(\cos\theta - \cos\theta_c) \quad (2)$$

where I_q is the quiescent current and θ_c is the conduction angle. They are related by

$$I_q = -I_a \cdot \cos\theta_c$$

In the region I, I_d is solely determined by V_d. Under the assumption that the load at fundamental frequency is R and all harmonics are shorted, V_d is simply:

$$V_d = V_{dc} - V_1 \cos\theta \quad (3)$$

where V_1 is the amplitude of the fundamental.

This simplification allows the drain current to be written as an explicit function of θ with θ_c, θ_k, V_{dc}, V_1, R_{on} and I_a as parameters:

$$I_d(\theta) = \begin{cases} \dfrac{V_{dc} - V_1 \cos\theta}{R_{on}} & 0 < |\theta| < \theta_k \\ I_a(\cos\theta - \cos\theta_c) & \theta_k < |\theta| < \theta_c \\ 0 & \text{elsewhere} \end{cases} \quad (4)$$

The Fourier analysis of Eq. 6 yields the fundamental component, I_1 as:

$$I_1 = \frac{2}{\pi}\int_0^{\pi} I_d(\theta)\cos\theta\, d\theta = I_1(\theta_c, \theta_k, V_{dc}, V_1, R_{on}, I_a) \quad (5)$$

Because θ_k is the boundary between the two regions, we have

$$\frac{V_{dc} - V_1\cos\theta_k}{R_{on}} = I_a(\cos\theta_k - \cos\theta_c) \quad (6)$$

Thus, V_1 can be written as an explicit function of θ_c, θ_k, V_{dc}, I_a, and R_{on}.

$$V_1 = V_1(\theta_c, \theta_k, V_{dc}, I_a, R_{on}) \quad (7)$$

And Ohm's law requires

$$I_1 = \frac{V_1}{R} \quad (8)$$

Substituting Eq. 7 into Eq. 5 and 8 and letting them be equal leads to an equation that has terms of θ_c, θ_k, V_{dc}, R, R_{on}, and I_a. Among these variables θ_k is unknown and the rest are either known or can be estimated. Therefore, θ_k can be solved from this equation. Because the equation has both θ_k and $\cos\theta_k$ terms, θ_k cannot be written in a close form. A numerical solution is required for θ_k. The actual process is a little tedious and purely algebra, and therefore will not be presented here.

Once θ_k is solved, the DC current, I_{dc} and the efficiency can be calculated by:

$$I_{dc} = \frac{1}{\pi}\int_0^{\pi} I_d(\theta)\, d\theta = I_{dc}(\theta_c, V_{dc}, R, R_{on}, I_a) \quad (9)$$

and

$$\eta = \frac{I_1 V_1}{2 I_{dc} V_{dc}} = \eta(\theta_c, V_{dc}, R, R_{on}, I_a) \quad (10)$$

respectively. The numerical results for a set of parameters

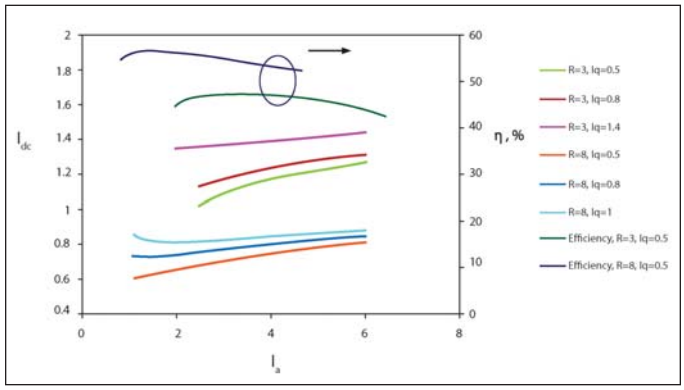


Figure 12 · I_{dc} vs I_a from numerical analysis of the saturation model at two load conditions of R = 3 and 8. The starting points of I_a are different because the region where the model is valid varies.

that are chosen to be the same as those in the real case are shown in Figure 12, where the DC current, I_{dc} and efficiency η vs. the driving level, I_a for two I_q and R conditions are plotted. The range for I_a is estimated to be representative of the reality. The results show that high load resistance (R = 8) yields lower DC currents and higher efficiencies, which is consistent with experimental observations. Also can be seen is the initial drop in DC current at high I_q condition for R = 8 case as in the hard limit case. On the other hand, unlike the hard limit model described in Eq. 1, this model does not predict the convergence of the DC currents with different I_q conditions. Overall, this model explains the occurrence of the clipping effect in a more natural way, but the actual circuit behavior seems to be more resembling to the prediction by the hard limit model, indicating that the current in the real circuit is more severely limited than this model predicts. Inspection of the actual I-V curves shown in Figure 1 reveals that the drain current actually slowly decreases when the voltage swings towards to 0 V, and the transition from the saturation region (region II) to the linear region (region I) occurs significantly earlier than assumed in the model. Both can result in a stronger clipping effect in actual device.

Another interesting result from this analysis is that once into saturation, even in this highly simplified model, the load-line slope is no longer the convention value of $-1/R$. This can be seen as follows. Substitution of Eq. 3 into Eq. 2 to cancel the cosθ term yields:

$$I_d = I_q + \frac{I_a}{I_1 R}(V_{dc} - V_d) \quad (11)$$

Here Eq. 8 is used. Eq. 11 represents a straight line on the plane of (I_d, V_d). It passes through the point of (I_q, V_{dc}) and has slope of $-I_a / I_1 R$. Thus, the load-line slope is not

a constant anymore because of the additional factor of I_a / I_1, and it cannot be determined prior to the completion of the numerical analysis. The trajectory in the (I_d, V_d) plane for a complete RF cycle is shown in Figure 11.

In summary, the observed independence of conduction angle or quiescent current of DC current and efficiency at high driving levels is an indication of the existence of a strong clipping effect on the drain current. The hard limit model predicts a tread that is in a reasonably good agreement with the measured data in this regard. But the efficiency based on this model converges around mid 60% instead of mid 80% as measured on the real circuit. So the clipping effect alone does not provide a full account for the measured high efficiencies.

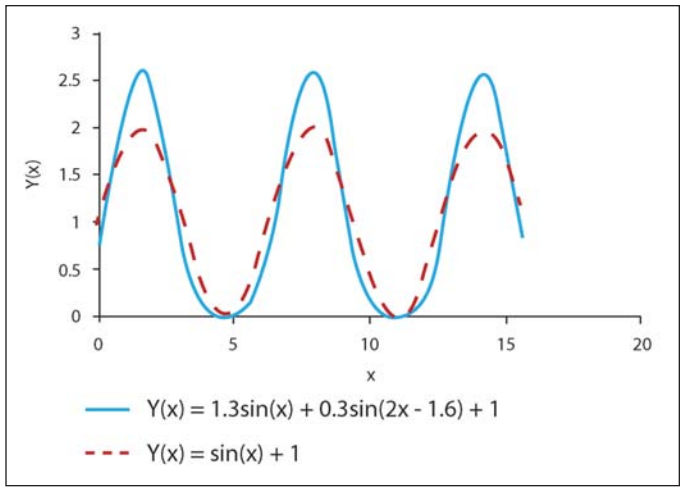


Figure 13 · Second harmonic effect.

Efficiency Boost from Harmonic Tuning

Another major category of high efficiency PAs is class F or inverse class F amplifiers. There are some variations in the definition of this class of PAs in the literature, but the basic idea is the same, that is, to manipulate the waveforms by adding harmonic components in such a way that the fundamental amplitude can be increased for the same maximum swing allowed by the circuitry. Between these two classes of amplifiers, the truncated sine wave is assumed for the drain current in the class F analysis, which is clearly inconsistent with the experimental data shown in the last section. On the other hand, the square wave is the waveform used in the inverse class F for current. The independence with the quiescent current observed in experiments comes about naturally with this kind of waveform. Hence, the inverse class F is the focus of analysis in this section. The mechanism for the efficiency boost in this class amplifier is the flattening effect associated with the addition of a second harmonic component to the fundamental waveform. The concept is illustrated in Figure 13, where the quantity in question, Y, is assumed to be limited to the region of $Y > 0$. For a given DC level of Y_{dc}, the waveform $Y(x)$ is first assumed to only consist of the fundamental and DC components, that is $Y_1(x) = Y_a \sin(x) + Y_{dc}$. In this case the maximum possible fundamental amplitude is $Y_a = Y_{dc}$. In the second case, if a second harmonic component is added to the waveform it can be shown that within a certain range of phase angle the maximum swing at the bottom portion is reduced, thus allowing the fundamental amplitude to be further increased. In Figure 13, a waveform of $Y_2(x) = 1.3 \sin(x) + 0.3 \sin(2x - 1.6) + 1$ along with $Y_1(x) = 1 \sin(x) + 1$ is shown. Thus, for the second case, the maximum fundamental amplitude is about 30% higher than that in the first case. Because the DC level stays the same this increase in fundamental amplitude directly translates into efficiency gain.

To investigate this mechanism for the observed efficiency improvement, the drain voltage was probed on the actual circuit board using an oscilloscope with the sampling rate of 8 GS/s. Some small but noticeable loading effects were observed. The probe also has some frequency-dependence. Apparently the operating frequency is a lit-

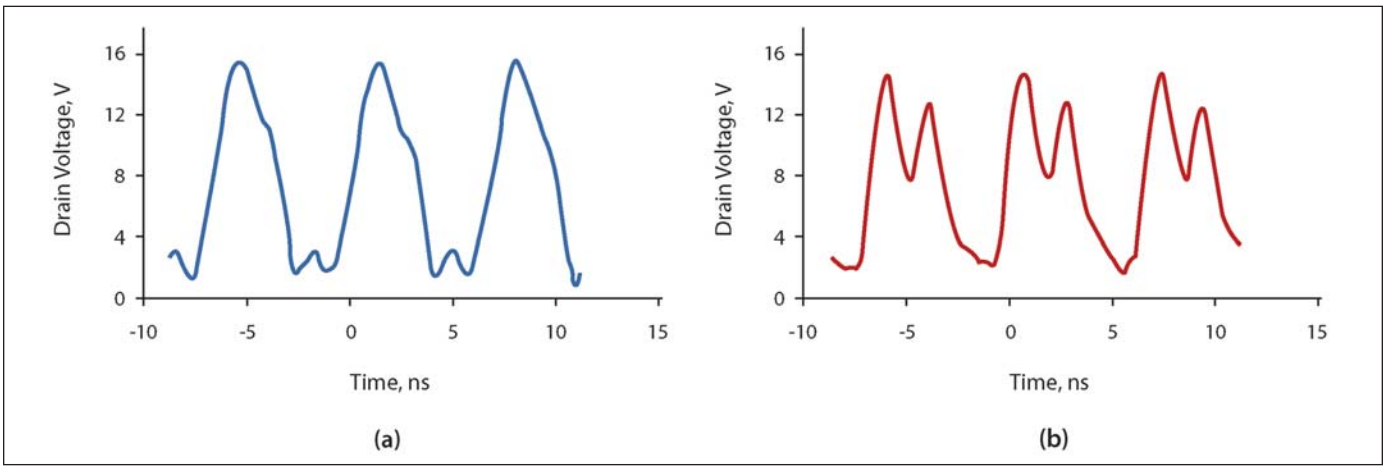


Figure 14 · Measured waveforms of: (a) high efficiency circuit and (b) high power circuit.

tle too high for this technique to provide a perfectly accurate measure of the actual waveform. Nevertheless, at the moderate RF frequency of 150 MHz this measurement still reveals the basic features of the waveforms measured. Figure 14 shows two measured waveforms for the high efficiency circuit and high power circuit used in this article (Figures 2 and 6). It can be seen that the waveform of the high efficiency circuit has a relatively flat bottom (near 0 V), which closely resembles the waveform shown in Figure 13 when the second harmonic is added. The Fourier analysis of the captured waveforms indicates significant existence of the second and third harmonic components in both cases. The second harmonic amplitude is actually about one-third of the fundamental. The measured waveform of the high efficiency circuit appears to have the same shape as that illustrated in Figure 13, which suggests the phase angel between the fundamental and second harmonic is about right for the efficiency improvement. In fact, the Fourier analysis shows that harmonic amplitudes have no significant difference between the two cases. Apparently the high efficiency circuit has a more favorable phase angle, resulting in a favorable waveform for high efficiency operation. So, the second harmonic tuning is expected to improve the efficiency by more than 30% in this case. This amount of increase boosts the efficiency from mid 60% to mid 80%. Thus, the observed convergence of DC current and 85% efficiency can be accounted for by the combination of clipping effect and second harmonic tuning.

Second harmonic tuning is the essence of the inverse class F amplifiers. It is often stated in the literature that the load needs to be infinity (open circuit) at the second harmonic for inverse class F amplifiers. This requirement actually comes about from a mathematical necessity for formulae manipulation when the drain current is idealized as an independent (on the drain voltage) square wave. Because the square wave does not have even harmonic components (that is, $I(2f_0) = 0$), the load at the second harmonic, $Z(2f_0)$ must be infinite to support a finite voltage at $2f_0$ so that the Ohm's law, $V(2f_0) = Z(2f_0) \cdot I(2f_0)$ still holds. In an actual circuitry even at moderate driving levels the drain current and voltage are highly interactive, and nonlinearity effects are expected to generate significant amount of harmonic components in the current. As a result, relatively high drain voltages at the harmonic frequencies can be supported with a finite second harmonic impedance such as the case demonstrated in Figure 7. In fact, the phase angle of the second harmonic component with respect to the fundamental amplitude seems to be more critical for achieving high efficiency than the amplitude itself. It is speculated that the increased load resistance not only reduces the knee voltage, as explained earlier, but also generates a more favorable phase condition for the second harmonic tuning. This design scheme clearly will break down at higher frequencies where the output capacitance provides a short at harmonics. On the other hand, at the relatively low RF frequency of 150 MHz, the conventional inverse class F design approach using multiple sections of transmission line [6] to realize the open condition at $2f_0$ becomes difficult to implement because of the unrealistic physical size for achieving the required electrical length.

Finally, it is worth noting the following observation. Even though at the device drain the voltage has a considerable amount of second and third harmonic components with respect to the fundamental amplitude, the actual powers dissipated in the 50-ohm termination at the harmonic frequencies are relatively low. The measurement indicates that the sum of powers of all harmonics at the termination is less than 0.5% of the power of the fundamental frequency. Hence, the benefit of having a second harmonic component in the drain voltage (allowing the increase of the fundamental amplitude) significantly outweighs the cost (power dissipation at the second harmonic frequency) in terms of efficiency enhancement. This can be understood by observing that the matching network between the 50-ohm load and the transistor drain functions as a step-up transformer at the fundamental frequency and as a low pass filter at harmonic frequencies. As a result, the fundamental amplitude at the 50-ohm termination is increased from the value at the drain, while the harmonic amplitudes are reduced. An AC simulation of the actual matching network at the fundamental and second harmonic frequencies yields a result that is in good agreement with the measurement.

Conclusion

A high efficiency of 87% has been achieved with a 5 W, 150 MHz power amplifier using conventional matching circuits. The measured data show the observed high efficiencies are independent of the quiescent current or conduction angle. The second harmonic tuning, in combination with the clipping effect, is claimed to be responsible for the high efficiency. This mechanism is similar to that in an inverse class F amplifier, but the circuit does not have the open load at $2f_0$ as is usually required for the inverse class F amplifier. The type of matching circuits used in this work is common in practical amplifiers and is particularly suitable for applications in the low RF range where the usage of multiple transmission lines with phase angles of a few tens of degrees is often impractical. The high efficiency of this work is achieved at increased load resistance, which reduces the output power and gain. In principle, the device power capability is not fully utilized in this mode of condition. But with the advances in device design and manufacturing technology the cost of RF power devices is continuously decreasing. This is particularly true for devices of less than 10 W and in the sub-

GHz frequency range for which the wattage is no longer the sole deciding factor for pricing. Additionally, in this frequency range, RF transistors usually have plenty of gain. Hence, trading the power output capability and gain for efficiency might be an acceptable trade-off in practical designs.

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Note

{1} The high bias conditions are only for investigation purpose and might not be appropriate for actual circuit operations.

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