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Design Method for the Fastest Settling Type 2 Phase Lock Loop: Part 2

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The author shows that mapping the denominator of the closed loop PLL transfer function to the Gaussian function results in the fastest settling time

This article is continued from last month, with analysis of higher-order loop filters.

4th Order Type 2 Fastest Settling PLL

I started the analysis of 4th order with the loop filter shown in Figure 9. Basically, additional pole due to R_{p2} and R_{p2} are added at the output of the op amp increase the order from 3rd to 4th. After some lengthy analysis, which will not be shown here, I found out that it is impossible to match the denominator of the CL(s) to the Gaussian LPF since this require the pole due to R_{p2} and R_{p2}, to be the complex conjugate of the pole due R_z, C_p and C_z as in (30). Both of these pole can only be real so this loop filter topology will not work.

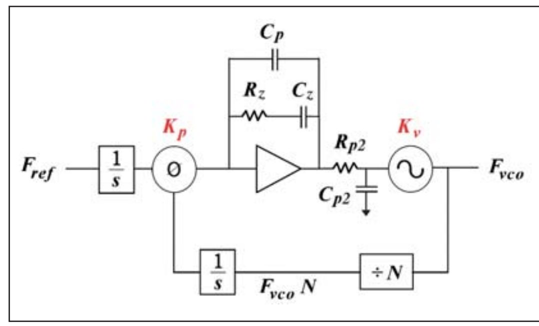

Figure 9 · Initial 4th order type 2 PLL.

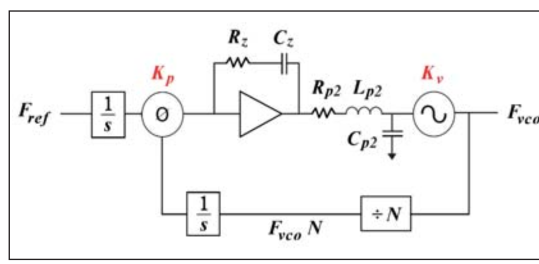

Figure 10 · Final 4th order type 2 PLL.

To solve this problem, the loop filter topology shown in Figure 10 needs to be used. By using this topology, the two poles created by L_p and C_p will definitely be complex conjugate of each other, and R_p can be used to further define the placement of the complex pole.

We start with the 4th order Gaussian low pass filter, whose values normalized are listed in Table 1 (in Part 1). Figure 11 shows the corresponding schematic. The transfer function of the circuit in Figure 11 can be shown to be of Equation (44).

Next is to calculate the *OL(s)* of the 4th order PLL in Figure 10. The *OL(s)* will be the *OL(s)* of the 2nd order as in (12), but multiply with the transfer function due to R_{p2}, C_{p2} and L_{p2}. The transfer function due to R_{p2}, C_{p2} and L_{p2} is shown in (45),

$$LF2(s) = \frac{1}{s^2 L_{p2} C_{p2} + R_{p2} C_{p2} s + 1} \qquad (45)$$

(45) is of 2nd order and for a 2nd order system, it can be completely represented in terms of the damping factor ξ and the natural fre-

$$H(s) = \frac{1}{L_4 C_3 L_2 C_1} \frac{1}{s^4 + \frac{s^3}{L_4} + \frac{L_2 C_1 + L_4 C_1 + L_4 C_3}{L_4 C_3 L_2 C_1} s^2 + \frac{C_3 + C_1}{C_3 C_1} s + \frac{1}{L_4 C_3 L_2 C_1}} \qquad (44)$$

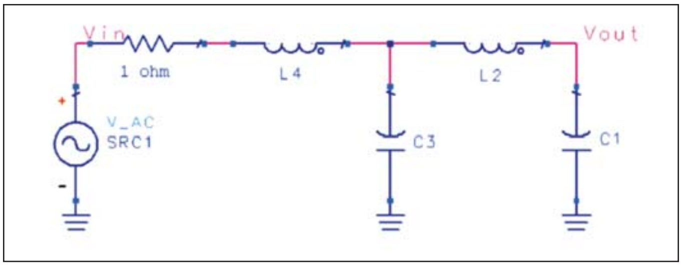

Figure 11 · 4th order low pass filter circuit.

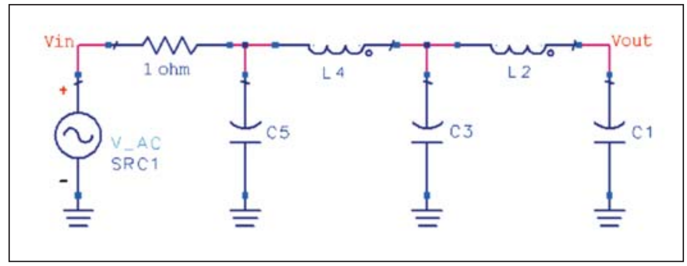

Figure 12 · 5th order low pass filter circuit.

quency ω_n, as shown in (46). These 2 constants, ξ and ω_n, completely describe the 2nd order circuit, so the value of R_{p2}, C_{p2} and L_{p2} can be calculated, if these two values are known. The OL(s) can be written as in (47).

$$LF2(s) = \frac{1}{\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n} s + 1} \tag{46}$$

$$OL(s) = \frac{K_p}{sC_z}\left(1 + \frac{s}{\omega_z}\right) \frac{1}{\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n} s + 1} \frac{K_v}{Ns} \tag{47}$$

The ω_0 is calculated from (47) by setting the *OL* gain to 1 and $s = j\omega_0$, as shown in (48). A new variable X_{on}, which is a ratio of ω_0 to ω_n, is defined in (49). X_{on} is also a constant that needs to be solved simultaneously in order for the denominator of the close loop transfer function to be of Gaussian.

$$\omega_o^2 = \frac{K_p}{C_z} \sqrt{1 + X_{oz}} \frac{1}{\sqrt{(1 - X_{on}^2)^2 + (2\xi X_{on})^2}} \frac{K_v}{N} \tag{48}$$

$$X_{on} = \frac{\omega_o}{\omega_n} \tag{49}$$

The *CL(s)* can now be calculated, and after substituting X_{oz}, X_{on}, we have the finalized *CL(s)* shown in (50). M4 in (51) is to simplify *CL(s)*

$$CL(s) = \frac{1}{\omega_z (C_z)} \frac{K_p K_v (\omega_z + s) \omega_n^2 \omega_p}{s^4 + 2\xi \frac{\omega_o}{X_{on}} s^3 + \left(\frac{\omega_o}{X_{on}}\right)^2 s^2 + \frac{\omega_o^3 X_{oz}}{X_{on}^2} M_4 s + \frac{\omega_o^4}{X_{on}} M_4} \tag{50}$$

$$M_4 = \frac{\sqrt{(1 - X_{on}^2)^2 + (2\xi X_{on})^2}}{\sqrt{1 + X_{oz}^2}} \tag{51}$$

Now we can equate the denominator of (51) to the denominator of (45). As before, we are interested to find the X_{of}, rather than just ω_o. Therefore we have the following set of equations,

$$2\xi \frac{X_{of}}{X_{on}} = \frac{1}{L_{4N}} \tag{52}$$

$$\left(\frac{X_{of}}{X_{on}}\right)^2 = \frac{L_{2N}C_{1N} + L_{4N}C_{1N} + L_{4N}C_{3N}}{L_{4N}C_{3N}L_{2N}C_{1N}} \tag{53}$$

$$\frac{X_{of}^3 X_{oz}}{X_{on}^2} M_4 = \frac{C_{3N} + C_{1N}}{C_{3N}C_{1N}} \tag{54}$$

$$\frac{X_{of}^4}{X_{on}} M_4 = \frac{1}{L_{4N}C_{3N}L_{2N}C_{1N}} \tag{55}$$

Solving (52) to (55) simultaneously, the value of X_{op}, X_{oz} and X_{of} can be calculated.

$$X_{oz} = 2.5647 \tag{56}$$

$$X_{on} = 0.3337 \tag{57}$$

$$X_{of} = 1.3222 \tag{58}$$

$$\zeta = 0.7695 \tag{59}$$

From (47), the phase margin can be calculated as follows,

$$PM = phase\left(1 + j\frac{\omega_o}{\omega_z}\right) - phase\left(\left(1 - \frac{\omega_o^2}{\omega_n^2}\right) + j\frac{\omega_o}{\omega_n} 2\xi\right)$$

$$PM = 38.669$$

The phase margin for 4th order is a little bit small at 38.669. Nevertheless, at this phase margin, the loop is still stable, and it is not uncommon to find a PLL with such a phase margin. Another point to note is that, the X_{off} is smaller than of the 3rd order, which indicates that 4th order PLL is faster than 3rd order, for a given ω_0.

5th Order Type 2 Fastest Settling PLL

By now, we should have seen the trend that the higher the order, the faster will the settling time of the PLL. The penalty that we have to pay is that, the PM gets smaller with increasing order. Lower PM will cause a bump around LBW, on the close loop response. This bump will translate into a bump on the phase noise at the output, so precaution need to be taken and proper simulation of phase noise need to be carried out.

We start with the 5th order Gaussian low pass filter, whose normalized values are listed in Table 1. Figure 12 shows the corresponding schematic. The transfer function of the circuit in Figure 12 is in (60), see below.

The PLL circuit for 5th order is the extension of 4th order PLL, where there is additional capacitor C_p around the op amp. This is shown in Figure 13.

The corresponding *OL(s)* is shown in (61). As per 4th order analysis, ξ and ω_n describes the 2nd order circuit due to R_{p2}, L_{p2} and C_{p2}, as in (46)

$$OL(s) = K_p \frac{(1+\frac{s}{\omega_z})}{s(1+\frac{s}{\omega_p})(C_z+C_p)} \frac{1}{\frac{s^2}{\omega_n^2}+\frac{2\xi}{\omega_n}s+1} \frac{K_v}{Ns} \tag{61}$$

The ω_o can be calculated from (61) by substituting s with $j\omega_o$ and set the gain to 1. The corresponding equation to calculate ω_o is in (62). X_{oz}, X_{op} and X_{on} were defined previously

$$\omega_0^2 = \frac{K_p K_v \sqrt{1+X_{oz}^2}}{N(C_z+C_p)\sqrt{1+X_{op}^2}\sqrt{(1-X_{on}^2)^2+(2\xi X_{on})^2}} \tag{62}$$

The *CL(s)* can now be calculated, and the final equation is shown in (63), see below. M5 in (64) is to simplify *CL(s)*.

$$M_5 = \frac{\sqrt{1+X_{op}^2}\sqrt{(1-X_{on}^2)^2+(2\xi X_{on})^2}}{\sqrt{1+X_{oz}^2}} \tag{64}$$

Now we can equate the denominator of (64) to the denominator of (60). We are interested in X_{of} rather than

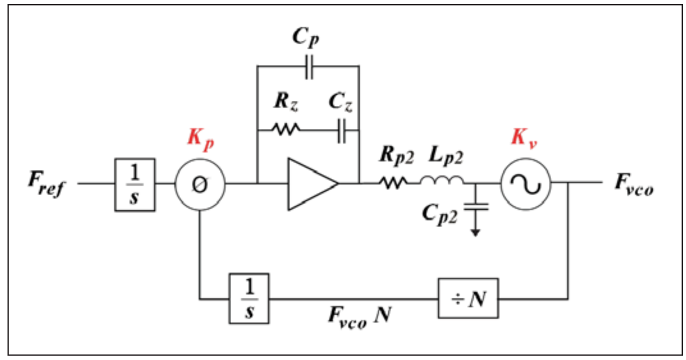

Figure 13 · 5th order Type 2 PLL.

ω_o, therefore we have the followings sets of equations to be solved simultaneously.

$$(2\xi\frac{X_{of}}{X_{on}}+\frac{X_{of}}{X_{op}}) = \frac{1}{C_{5N}} \tag{65}$$

(66), see below

$$\frac{X_{of}^3}{X_{op}X_{on}^2} = \frac{L_{2N}C_{1N}+L_{4N}C_{1N}+L_{4N}C_{3N}}{C_{5N}L_{4N}C_{3N}L_{2N}C_{1N}} \tag{67}$$

$$\frac{X_{of}^4 X_{oz} M_5}{X_{op}X_{on}^2} = \frac{C_{5N}+C_{3N}+C_{1N}}{C_{5N}L_{4N}C_{3N}L_{2N}C_{1N}} \tag{68}$$

$$\frac{X_{of}^5 M_5}{X_{op}X_{on}^2} = \frac{1}{C_{5N}L_{4N}C_{3N}L_{2N}C_{1N}} \tag{69}$$

Solving (66) to (70) simultaneously, the value of X_{op}, X_{oz}, X_{on}, X_{of} and ξ can be calculated.

$$X_{oz} = 2.5439 \tag{70}$$

$$X_{op} = 0.2611 \tag{71}$$

$$X_{on} = 0.3228 \tag{72}$$

$$H(s) = \frac{1}{C_5L_4C_3L_2C_1} \frac{1}{s^5+\frac{s^4}{C_5}+\frac{C_3L_2C_1+C_5L_2C_1+C_4L_4C_1+C_5L_4C_3}{C_5L_4C_3L_2C_1}s^3+\frac{L_2C_1+L_4C_1+L_4C_3}{C_5L_4C_3L_2C_1}s^2+\frac{C_5+C_3+C_1}{C_5L_4C_3L_2C_1}s+\frac{1}{C_5L_4C_3L_2C_1}} \tag{60}$$

$$CL(s) = \frac{1}{\omega_z(C_z)} \frac{K_pK_v(\omega_z+s)\omega_n^2\omega_p}{s^5+(2\xi\frac{\omega_o}{X_{on}}+\frac{\omega_o}{X_{op}})s^4+(\frac{2\xi\omega_o^2}{X_{op}X_{on}}+\frac{\omega_o^2}{X_{on}^2})s^3+\frac{\omega_o^3}{X_{op}X_{on}^2}s^2+\frac{\omega_o^4X_{oz}M_5}{X_{op}X_{on}^2}s+\frac{\omega_o^5M_5}{X_{op}X_{on}^2}} \tag{63}$$

$$(\frac{2\xi X_{of}^2}{X_{op}X_{on}}+\frac{X_{of}^2}{X_{on}^2}) = \frac{C_{3N}L_{2N}C_{1N}+C_{5N}L_{2N}C_{1N}+C_{4N}L_{4N}C_{1N}+C_{5N}L_{4N}C_{3N}}{C_{5N}L_{4N}C_{3N}L_{2N}C_{1N}} \tag{66}$$

$$X_{of} = 1.1326 \tag{73}$$

$$\xi = 0.508 \tag{74}$$

From (61), the phase margin can be calculated as follows,

$$PM = phase(1 + j\frac{\omega_o}{\omega_z}) - phase(1 + j\frac{\omega_o}{\omega_p}) - phase((1 - \frac{\omega_o^2}{\omega_n^2}) + j\frac{\omega_o}{\omega_n}2\xi))$$

$$PM = 33.799$$

As far as stability is concerned, the phase margin of 33.799 is quite small but still stable. Because of the small phase margin as well, proper calculation and simulations need to be carried out to ensure that the PLL is stable over the whole operating frequency. Some LBW compensation circuitries might need to be in place.

6th Order Type 2 Fastest Settling PLL

There are still extra PM left before the loop goes unstable, so it is still doable to solve for 6th order. I'm going to cut short the analysis for 6th order (and for 7th order after this) since it basically follows the same steps shown before, and it would take a lot of area to write the equations. Instead of trying to solve for the transfer function of the 6th order LPF similar in Figure 11, I'll just provide the coefficients of the denominator. The 6th order LPF will have a transfer function shown in (75)

$$H(s) = \frac{g_0}{s^6 + g_5 s^5 + g_4 s^4 + g_3 s^3 + g_2 s^2 + g_1 s + g_0} \tag{75}$$

For Gaussian LPF, values of each coefficients are listed below, for ω_{3dB} = 1 rad/s

g_5 = 10.19368
g_4 = 47.60398
g_3 = 128.789374
g_2 = 210.709533
g_1 = 196.100192
g_0 = 80.573668

For the 6th order PLL circuit, we have two choices, either to use the circuit in Figure 14 or the circuit in Figure 15. I considered Figure 16 initially but found out that there will be no solutions since there can only be one non-zero passive pole. PLL in Figure 16 has two non-zero pasive poles, one due to R_z, C_z and C_p, and the other one due to R_{pd} and C_{pd}. Figure 14 requires 3rd order circuit at the output of the op amp, and this is not so convenient since there are no specific 3 parameters to completely define a 3rd order network. Figure 15 has two 2nd order networks before the op amp and after the op-amp. This

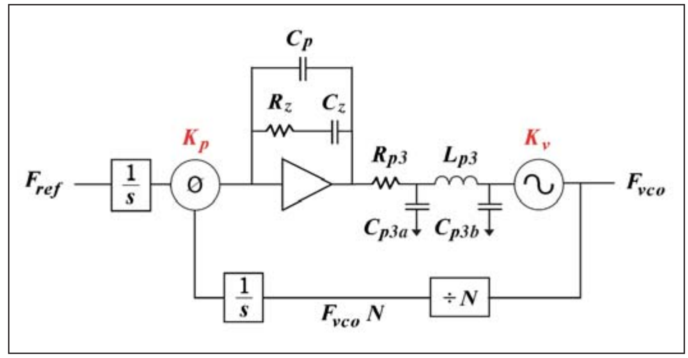

Figure 14 · Option 1 for 6th order PLL.

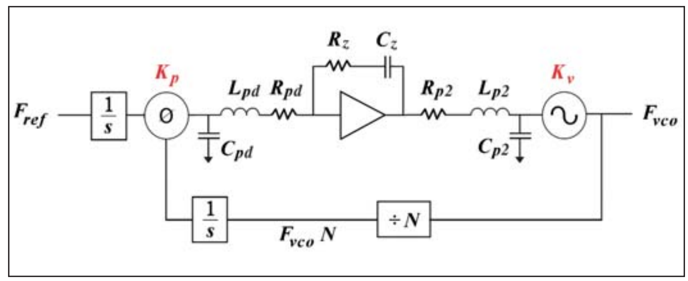

Figure 15 · Option 2 for 6th order PLL.

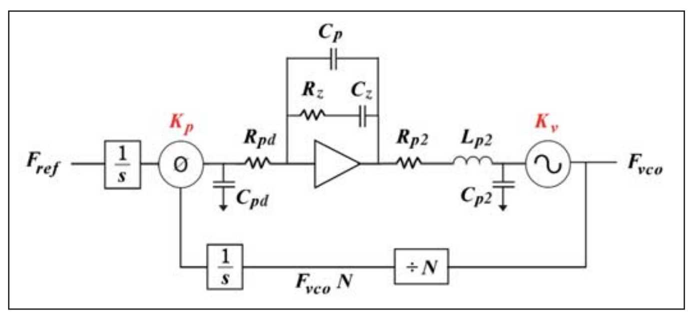

Figure 16 · 6th order PLL that will not generate fastest settling PLL.

will be easier to solve and hence will be used for the analysis. The *OL(s)* of the PLL shown in Figure 15 is in (76)

$$OL(s) = \frac{K_p K_v}{s^2 N C_z} \frac{1 + \frac{s}{\omega_z}}{\frac{s^2}{\omega_{npd}^2} + \frac{2\xi_{pd}}{\omega_{npd}} s + 1} \cdot \frac{1}{\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n} s + 1} \tag{76}$$

The ξ_{pd} and ω_{npd} are for the 2nd order network before the op amp. A new ratio X_{onpd} will have to be defined,

$$X_{onpd} = \frac{\omega_o}{\omega_{npd}} \tag{77}$$

The ω_o can be calculated or solved by using (76). (76) is also used to calculated the required K_p to get the required ω_o.

$$\omega_0^{\ 2} = \frac{K_p K_v \sqrt{1+X_{oz}^{\ 2}}}{NC_z\sqrt{(1-X_{onpd}^{\ 2})^2+(2\xi_{pd}X_{onpd})^2}\sqrt{(1-X_{on}^{\ 2})^2+(2\xi X_{on})^2}} \qquad (78)$$

The $CL(s)$ will also not be shown here as it is too long but the coefficients in the denominator will be included, and equate it to g_5 to g_0.

$$2\xi\frac{X_{of}}{X_{on}} + 2\xi_{pd}\frac{X_{of}}{X_{onpd}} = g_5 \qquad (79)$$

$$4\xi_{pd}\xi\frac{X_{of}^{\ 2}}{X_{onpd}X_{on}} + \frac{X_{of}^{\ 2}}{X_{on}^{\ 2}} + \frac{X_{of}^{\ 2}}{X_{onpd}^{\ 2}} = g_4 \qquad (80)$$

$$2\frac{X_{of}^{\ 2}}{X_{onpd}X_{on}}(\xi_{pd}\frac{X_{of}}{X_{on}} + \xi\frac{X_{of}}{X_{onpd}}) = g_3 \qquad (81)$$

$$\frac{X_{of}^{\ 4}}{(X_{onpd}X_{on})^2} = g_2 \qquad (82)$$

$$\frac{X_{of}^{\ 5}X_{oz}}{X_{on}^{\ 2}X_{onpd}^{\ 2}}M_4M_6 = g_1 \qquad (83)$$

$$\frac{X_{of}^{\ 6}}{X_{on}^{\ 2}X_{onpd}^{\ 2}}M_4M_6 = g_0 \qquad (84)$$

M_4 was defined before in (52) and M_6 is defined in (85). Both are used to simplify the equations.

$$M_6 = \sqrt{(1-X_{onpd}^{\ 2})^2 + (2\xi_{pd}X_{onpd})^2} \qquad (85)$$

Solving (79) to (84) simultaneously, the value of X_{onpd}, X_{oz}, X_{on}, X_{of}, ξ and ξ_{pd} can be calculated.

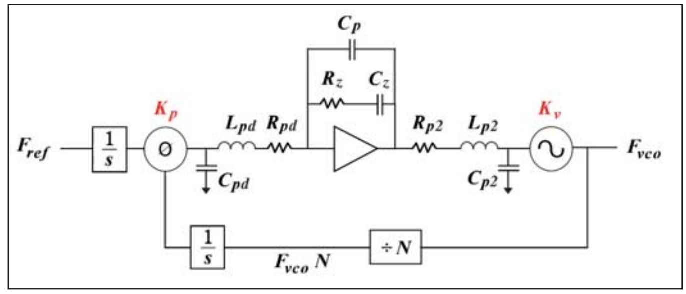

Figure 17 · 7th order type 2 PLL.

$$X_{oz} = 2.5424 \qquad (86)$$

$$X_{on} = 0.3179 \qquad (87)$$

$$X_{onpd} = 0.2364 \qquad (88)$$

$$X_{of} = 1.0446 \qquad (89)$$

$$\xi = 0.3271 \qquad (90)$$

$$\xi_{pd} = 0.9104 \qquad (91)$$

The phase margin can be calculated from (76), as in the top equation below.

$PM = 30.989$ deg

7th Order Type 2 Fastest Settling PLL

The 6th order LPF has the transfer function:

$$H(s) = \frac{g_0}{s^7 + g_6s^6 + g_5s^5 + g_4s^4 + g_3s^3 + g_2s^2 + g_1s + g_0} \qquad (92)$$

$$PM = phase(1 + j\frac{\omega_o}{\omega_z}) - phase((1-\frac{\omega_o^{\ 2}}{\omega_n^{\ 2}}) + j\frac{\omega_o}{\omega_n}2\xi)) - phase((1-\frac{\omega_o^{\ 2}}{\omega_{npd}^{\ 2}}) + j\frac{\omega_o}{\omega_{npd}}2\xi_{pd}))$$

$$\omega_0^{\ 2} = \frac{K_p K_v\sqrt{1+X_{oz}^{\ 2}}}{N(C_z+C_p)\sqrt{1+X_{op}^{\ 2}}\sqrt{(1-X_{onpd}^{\ 2})^2+(2\xi_{pd}X_{onpd})^2}\sqrt{(1-X_{on}^{\ 2})^2+(2\xi X_{on})^2}} \qquad (94)$$

$$4\xi_{pd}\xi\frac{X_{of}^{\ 2}}{X_{onpd}X_{on}} + \frac{X_{of}^{\ 2}}{X_{on}^{\ 2}} + \frac{X_{of}^{\ 2}}{X_{onpd}^{\ 2}} + 2\xi\frac{X_{of}^{\ 2}}{X_{op}X_{on}} + 2\xi_{pd}\frac{X_{of}^{\ 2}}{X_{op}X_{onpd}} = g_5 \qquad (96)$$

$$X_{of}^{\ 3}\frac{X_{onpd}^{\ 2} + X_{on}^{\ 2} + 4\xi_{pd}\xi X_{on}X_{onpd} + 2\xi X_{on}X_{op} + 2\xi_{pd}X_{onpd}X_{op}}{X_{on}^{\ 2}X_{op}X_{onpd}^{\ 2}} = g_4 \qquad (97)$$

$$PM = phase(1 + j\frac{\omega_o}{\omega_z}) - phase(1 + j\frac{\omega_o}{\omega_p}) - phase((1-\frac{\omega_o^{\ 2}}{\omega_n^{\ 2}}) + j\frac{\omega_o}{\omega_n}2\xi)) - phase((1-\frac{\omega_o^{\ 2}}{\omega_{npd}^{\ 2}}) + j\frac{\omega_o}{\omega_{npd}}2\xi_{pd}))$$

For Gaussian LPF, values of each coefficients are listed below, with $\omega_{3dB} = 1$ rad/s

$g_6 = 12.4533$
$g_5 = 172.476871$
$g_4 = 252.870805$
$g_3 = 566.484058$
$g_2 = 809.023329$
$g_1 = 678.141182$
$g_0 = 256.114957$

The PLL circuit to be used is shown in Figure 17. Figure 17 is leveraged from Figure 15, with additional C_p across the op amp to create one more pole/order.

The OL(s) of the PLL shown in Figure 17 is in (93)

$$OL(s) = \frac{K_p K_v}{s^2 N C_z} \cdot \frac{1+\frac{s}{\omega_z}}{1+\frac{s}{\omega_p}} \cdot \frac{1}{\frac{s^2}{\omega_{npd}^{\;2}} + \frac{2\xi_{pd}}{\omega_{npd}} s + 1} \cdot \frac{1}{\frac{s^2}{\omega_n^{\;2}} + \frac{2\xi}{\omega_n} s + 1} \quad (93)$$

The ω_o can be calculated or solved by using (94, see below). The *CL(s)* will also not be shown here as it is too long, but the coefficients in the denominator will be included, and equate it to g_6 to g_0.

$$\frac{X_{of}}{X_{op}} + 2\xi \frac{X_{of}}{X_{on}} + 2\xi_{pd} \frac{X_{of}}{X_{onpd}} = g_6 \quad (95)$$

(96), see pg. 52

(97), see pg. 52

$$X_{of}^{\;4} \frac{X_{op} + 2\xi_{pd} X_{onpd} + 2\xi X_{on}}{X_{on}^{\;2} X_{op} X_{onpd}^{\;2}} = g_3 \quad (98)$$

$$\frac{X_{of}^{\;5}}{X_{op}(X_{onpd} X_{on})^2} = g_2 \quad (99)$$

$$\frac{X_{of}^{\;6} X_{oz}}{X_{op} X_{on}^{\;2} X_{onpd}^{\;2}} M_5 M_6 = g_1 \quad (100)$$

$$\frac{X_{of}^{\;7}}{X_{op} X_{on}^{\;2} X_{onpd}^{\;2}} M_5 M_6 = g_0 \quad (101)$$

M_5 and M_6 were defined in (64) and (85). Solving (95) to (101) simultaneously, the value of X_{onpd}, X_{oz}, X_{on}, X_{of}, X_{op}, ξ and ξ_{pd} can be calculated.

$X_{oz} = 2.5447$ (102)
$X_{op} = 0.206$ (103)
$X_{on} = 0.3149$ (104)
$X_{onpd} = 0.2228$ (105)
$X_{of} = 0.9611$ (106)
$\xi = 0.206$ (107)
$\xi_{pd} = 0.7568$ (108)

The phase margin can be calculated from (93), as in the bottom equation on pg. 52.

$PM = 29.1758$ deg.

Design Example

Let's say a fastest settling PLL with the following parameters needs to be designed. To avoid confusion, all frequencies variable will be in rad/s.

Order = 7th
$\omega_o = 100$k rad/s
$F_{out} = 5$G rad/s
$F_{ref} = 10$M rad/s
$K_v = 100$M rad/s/v
K_p = Tunable from 10 µA/rad to 3 mA/rad

Solution: The circuit in Figure 17 is the one that we want to design. For 7th order, listed below are the con-

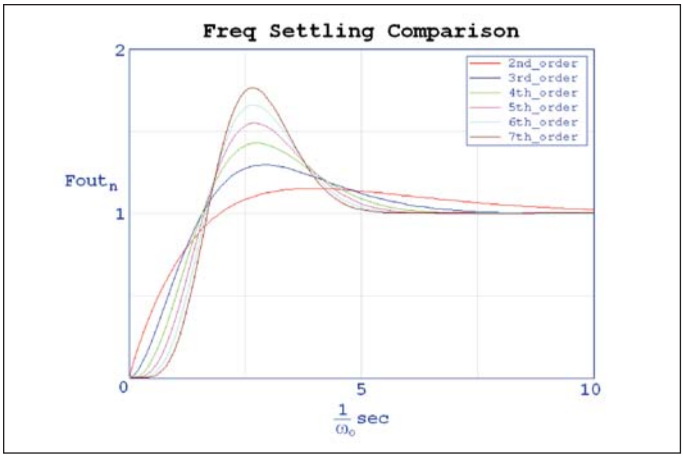

Figure 18 · The frequency settling time of fast settling PLL for varying orders.

stant that need to be used. These were from (102)-(108).

$X_{oz} = 2.5447$
$X_{op} = 0.206$
$X_{on} = 0.3149$
$X_{onpd} = 0.2228$
$X_{of} = 0.9611$
$\xi = 0.206$
$\xi_{pd} = 0.7568$

We start by solving ω_z, R_z and C_z first.

$$\omega_z = \frac{\omega_o}{X_{oz}} = 39.2974\ krad/s$$

R_z can be independently selected and a smaller value is preferred so to minimize phase noise contribution. On an additional note, we don't want R_z to be too small such that the C_z will be relatively huge. It is preferable to use COG capacitor for C_z to avoid dielectric absorption, and COG is hard to find for high capacitance. Dielectric absorption will cause the PLL to settle really slow, which would defeat our objective of designing fast settling PLL.

$R_z = 316\ ohm$

$$C_z = \frac{1}{\omega_z R_z} = 80.529\ nF$$

Next, ω_p and C_p can be solved. C_p is solved using (29)

$$\omega_p = \frac{\omega_o}{X_{op}} = 485.393 krad/s$$

$$C_p = \frac{C_z}{\omega_p R_z C_z - 1} = 7.0939\ nF$$

Next is to solve for ω_n, R_{p2}, L_{p2} and C_{p2}.

$$\omega_n = \frac{\omega_o}{X_{on}} = 317.6034\ krad/s$$

R_{p2} can be selected independently and again a small value is preferable to minimize noise.

$R_{p2} = 31.6\ ohm$

(46) and (47) are used to solve for L_{p2} and C_{p2}.

$$C_{p2} = \frac{2\xi}{R_{p2}\omega_n} = 41.056\ nF$$

$$L_{p2} = \frac{1}{C_{p2}\omega_n^{\ 2}} = 241.462\ uH$$

Same calculations need to be carried out of the 2nd order network before the op-amp. R_{pd} can be selected independently and again a small value is preferable to minimize noise.

$R_{pd} = 31.6\ ohm$

(45) and (46) are used to solve for L_{pd} and C_{pd}.

$$C_{p2} = \frac{2\xi}{R_{p2}\omega_n} = 106.707\ nF$$

$$L_{p2} = \frac{1}{C_{p2}\omega_n^{\ 2}} = 46.504\ uH$$

The feedback ratio N can be calculated from F_{out} and F_{ref},

$$N = \frac{F_{vco}}{F_{ref}} = 500$$

Finally, K_p can be calculated by using (94)

$$K_p = \frac{\omega_0^{\ 2} N(C_z + C_p)}{K_v} M_5 M_6 = 1.5016\ mA/rad$$

M_5 and M_6 were defined in (64) and (85). Even though the example is for 7th order, knowing how to design 7th order will enable ones to design lower orders easily.

Settling Speeds and Phase Noises Comparisons

The time domain response was calculated by first multiplying the *CL(s)* with a step response $\Delta Fref/s$. $\Delta Fref$ is calculated from (6). Then inverse Laplace transform is carried out to convert from frequency domain to time domain.

The settling speeds of type 2 PLLs with varying orders from 2nd to 5th are shown in Figure 14. The x-axis is in second and is scaled by ω_o. This is so that the settling of each order could be correctly compared. Normalizing the x-axes to ω_o will also give ones some rough ideas of the settling time, for a given ω_o. For example, let's say the ω_o is designed at 1Mrad/s. The unnormalized x-axis would then read 2us, 4us, up to 10us. The y-axis is the F_{out} and is normalized to the equivalent frequency step at the output. Referring to Figure 14, it can be seen that the higher the order, the faster the settling, for the same ω_o. And also, as the denominator is of Gaussian, the time domain response will just overshoot (due to ω_z of type 2), and then just settle with no more undershoot or overshoot.

Figure 14 illustrate the settling time roughly. In some application, it is critical to know how long it take for Fout to settle to within some percentage, and one example is in a network analyzer design. In a network analyzer, the source and LO frequencies are tuned so that they are offset by the IF frequency. This IF will then has to go through a digital filter center around IF, and with a bandwidth that could be as small as 10 Hz. The source and the LO has to settle within half the IF bandwidth, before measurement can take place. If measurement is done without waiting for either the source or the LO to settle, then the IF will not be at the center of the filter and we end up measuring noise. On a different scenario whereby we wait much longer than the actual settling time, then the sweep speed performance of the network analyzer will be impacted.

Table 2 listed down the normalized settling time for different PLL order and for different frequency settling %. Let's do a quick example on how to use the table. Let's say we have 5th order fast settling PLL and the ω_0 is designed at 500 krad/s. The VCO or F_{out} has to be stepped by 100 krad/s, and we would like to find the settling time after the F_{out} has settle to within 0.001% of the step F_{out}.

From Table 2, the normalized settling time for 0.001% settling and for 5th order is shown below.

$$t_{sN} = 11.1231$$

	Settling Time (1/wo) sec					
Freq Settling(%)	2nd_order	3rd_order	4th_order	5th_order	6th_order	7th_order
10	6.1584	5.2350	4.8831	4.6680	4.5083	4.3837
1	11.4576	7.4269	6.3026	5.7580	5.4305	5.2112
0.1	14.9915	8.6055	7.0042	6.3244	5.9957	5.8555
0.01	17.0357	12.1503	9.1119	9.0145	7.8919	7.0597
0.001	25.9160	15.7699	12.0804	11.1321	9.6953	8.5423
0.0001	29.8545	18.0728	14.9728	12.1371	11.6238	10.2928
0.00001	32.3717	19.1536	16.0071	14.4563	13.2773	11.7340
0.000001	40.2169	23.2161	18.6249	16.3762	14.6894	13.1986

Table 2 · Normalized settling time for different frequency settling %.

	Design Constants							
Order	PM(deg)	Xonpd	ξ pd	Xoz	Xop	Xon	ξ	Xof
2nd	74.26			3.5476				2.6735
3rd	48.70			2.6811	0.3807			1.6287
4th	38.69			2.5647		0.3337	0.7695	1.3222
5th	33.79			2.5439	0.2611	0.3228	0.5080	1.1326
6th	30.99	0.2364	0.9104	2.5424		0.3179	0.3271	1.0446
7th	29.18	0.3149	0.2060	2.5447	0.2060	0.2228	0.7568	0.9611

Table 3 · Design constants summary for 2nd, 3rd, 4th, 5th, 6th and 7th order fast settling PLL.

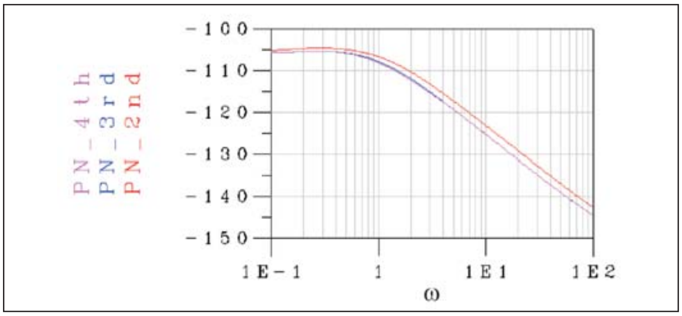

Figure 19 · Phase noise comparison between 2nd, 3rd and 4th order PLL.

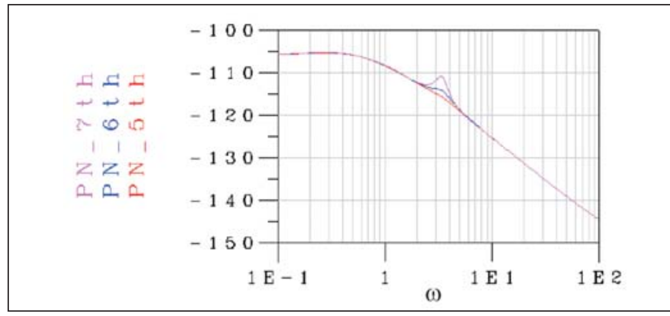

Figure 20 · Phase noise comparison between 5th, 6th and 7th order PLL.

The actual settling time is simply,

$$t_s = \frac{t_{sN}}{\omega_o} = 22.246\, us$$

As mentioned in the previous section, the PM will be lower for higher order. For 7th order, the PM is as small as 29.1758 degree so it is a good idea to check the phase noise since low PM could lead to a bump on phase noise around ω_0. Figure 18 shows the phase noise plot for 2nd order, 3rd order and 4th order, whereas Figure 19 is for 5th order, 6th order and 7th order. The phase noise from the divider N dominates the overall phase noise below ω_0 and the phase noise from the VCO dominate the overall phase noise above ω_0. From Figure 18, only phase noise of the 2nd order is quite high, and the phase noise of 3rd, and 4th order are pretty much similar. On top of that, no bump can be observed.

As we increase the order to 5th, a bump start to appear on the phase noise plot, as can be seen in Figure 19. This bump is at the ω_n of the 2nd order network due to small PM. The bump on the phase noise plot increase in magnitude as we increase the order to 6th and 7th order, since the PM of the 2nd order network reduces with increasing order.

Let say a 7th order settling performance and good phase noise without a bump are required. This can be achieved by switching different values of R_{pd}, R_z, and R_{p2}, and shorted out L_{pd} and L_{p2}, once F_{out} has settled to required value. Shorting out L_{pd} and L_{p2} will change both the 2nd order network to 1st order network so there will be no peaking. On top of that, switching L_{p2} and L_{pd} will not cause any transient since it is memoryless as far as voltage is concern. C_{pd}, C_{p2} and any capacitor in general should not be switched as this will cause additional transient. Figure 20 compare the phase noise of the 7th order PLL, before and after switching R_{pd}, R_z, R_{p2}, L_{p3} and L_{p2}. Both R_{pd} and R_{p2} were reduced by 50% and R_z was increased by 12.67%. The ω_0 remains the same but the PM improves to 44.4 degrees.

Summary

It was proven that if the denominator of the *CL(s)* is of Gaussian, then the type 2 PLL will settle the fastest. A step response of type 2 PLL, whose denominator is of Gaussian, is equivalent of the sum of impulse response and step response of Gaussian LPF.

The design parameters or constants for fast settling PLL have been derived for 2nd, 3rd, 4th, 5th, 6th and 7th order. The tabulated values are shown in Table 3. Refer to Figure 1, Figure 7, Figure 10, Figure 13, Figure 15 and Figure 17 for 2nd, 3rd, 4th, 5th, 6th and 7th order PLL circuit.

A table that listed down the normalized settling time for a given frequency settling % is included. This table is useful in finding an accurate settling time. The typical phase noise plot is also included and no phase noise bump can be observed.

Part 1 of this article appear in the June 2010 issue, and is available online in the Archives section of www.highfrequencyelectronics.com

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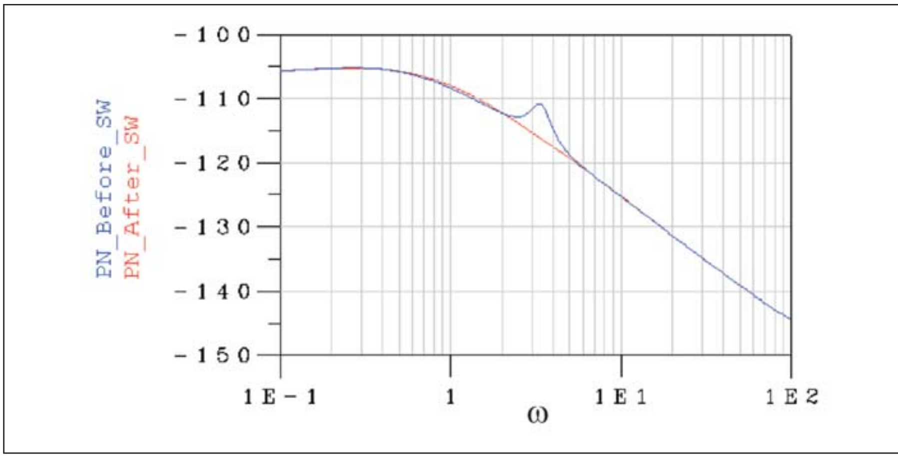

Figure 21 · Phase noise improvement on 7th order PLL after switching few components.

Author Information

Akmarul Ariffin Bin Salleh is an RF/microwave R&D engineer, focusing mainly on high performance PLL designs. Akmarul joined Agilent Technologies in 2000 as a Product Engineer taking care of Network Analyzer. He joined R&D in 2005 and has delivered products to the market, including the N9912A Network Analyzer/Spectrum Analyzer combo and the N9923A Handheld VNA. Akmarul graduated from Vanderbilt University with a B.E. in Electrical Engineering and also majoring in Mathematics.