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Optimize Thermal Contact for RF Transistors

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This article presents the results of heat transfer tests on various common methods for mounting power transistors to heat sinks, to determine which has the best thermal performance

The case-to-heatsink interface is a significant contributor to the overall thermal resistance from semiconductor junction to heatsink dissipation for transistors with low junction-to-case thermal resistance. This contact thermal resistance is comprised of surface irregularities of the transistor flange and heatsink, the interface medium, and contact pressure.

Good thermal conduction will occur only at the points of intimate contact, because the surface contact area of the transistor and heatsink is not perfectly flat. Thermal conductivity can be improved, however, by optimization of both the mounting pressure and the application of a thermally conductive medium, such as thermal joint compound.

A study was recently conducted on STMicroelectronics' new high voltage, high power DMOS transistors, the SD3931-10 and the SD3933. Both devices utilize a thermally enhanced, full braze BeO package to maximize heat transfer surface area from the semiconductor junction to case. The SD3931-10 is housed in a 0.500 in. diameter, 4-lead package, and the SD3933 is housed in a 0.550 in. diameter, 4-lead package. The junction to case thermal resistance ($R\theta_{j\text{-}c}$) of the devices is 0.45°C/W and 0.27°C/W, respectively.

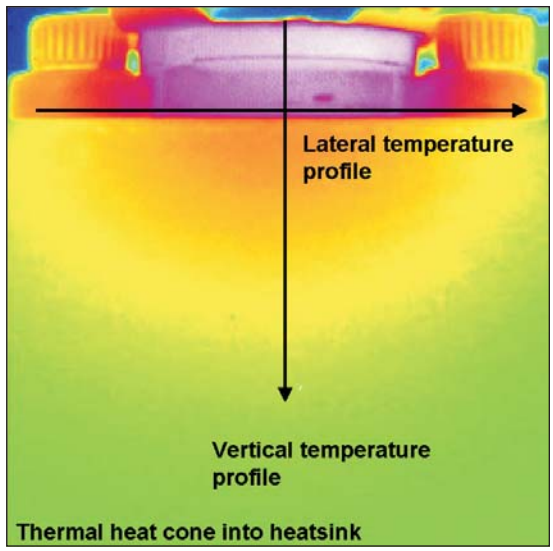

Figure 1 · Temperature map of an active SD3931-10 device.

Description of the Trials

Experiments were performed with various interface mediums and their relationship to contact thermal resistance. Measurements were taken at specific screw torque force in order to determine the effect of contact pressure. The following four trials were performed:

1. *Dry:* No thermal compound.
2. *Razored flange:* Thermal compound applied to flange only, excess removed with a razor blade.
3. *Mound:* Thermal compound applied to center of flange, mounded.
4. *Razored flange and heatsink:* Thermal compound applied to both the flange and heatsink, excess removed with a razor.

All trials used 4-40 UNC mounting screws and Wakefield 120 series thermal compound. Measurements were taken at areas of the device where the thermal properties of the materials are stable for the test temperature

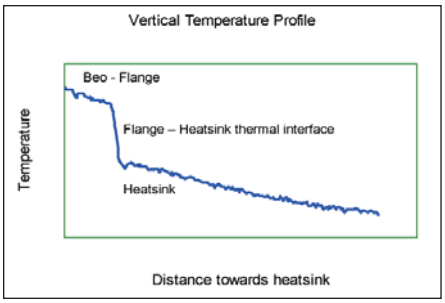

Figure 2 · Vertical temperature profile from BeO insulating substrate to heatsink.

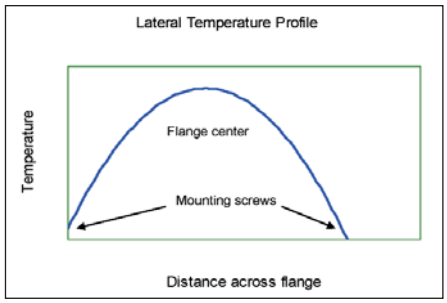

Figure 3 · Lateral temperature profile across the device flange.

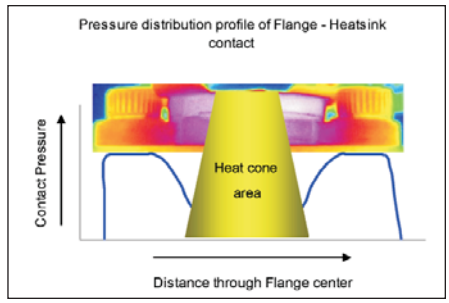

Figure 4 · Contact pressure across a device flange for end-screw mounting.

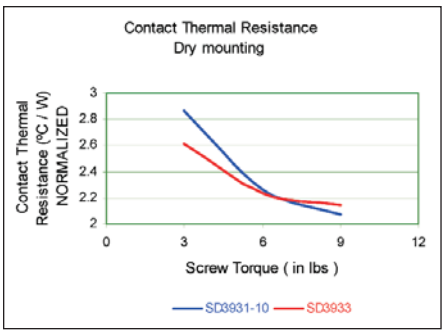

Figure 5 · The contact thermal resistance of each device mounted as indicated by Trial 1.

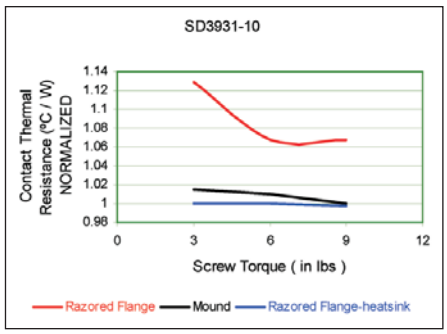

Figure 6 · The normalized contact thermal resistance of SD3931-10 mounted as indicated by Trials 2, 3 and 4.

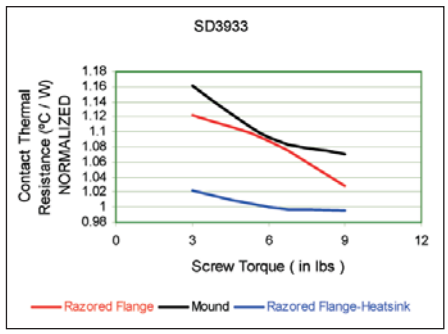

Figure 7 · The normalized contact thermal resistance of SD3933 mounted as indicated by Trials 2, 3 and 4.

range. Each contact thermal resistance chart is normalized to the respective device's characteristic at 6 in-lbs screw torque and razored flange-heatsink mount (Trial 4). The heatsink is of arbitrary surface flatness.

A temperature map of an active SD3931-10 device is shown in Figure 1. The thermal heat cone enters the heatsink at the device center (note the lateral, screw to screw, temperature profile). Figure 2 shows a vertical temperature profile from BeO to heatsink. The flange-heatsink contact is a contributor to the overall semiconductor junction to heatsink thermal resistance. Figure 3 charts a lateral temperature profile across the device flange. The screw-to-screw temperature distribution will indicate the uniformity of the mounting method. The contact pressure across a device flange for end-screw mounting [1] is depicted in Figure 4. The maximum contact pressure is at the screw areas, and the pressure decreases toward the center of the device. The heat cone is centered where the contact pressure is less. Figure 5 shows the contact thermal resistance (normalized as previously described) of each device mounted as indicated by Trial 1. The thermal resistance is a strong function of the pressure provided by the mounting screw torque. Air is the interface medium for the flange and heatsink mounting surfaces.

Figure 6 shows the normalized contact thermal resistance of SD3931-10 mounted as indicated by Trials 2, 3 and 4. The contact thermal resistance is not a significant function of pressure in the case of Trial 4. This is due to the use of thermal compound as an interface medium on both mounting surfaces. The excess is wiped clean from the intimate surface areas where metal to metal contact is ideal. Figure 7 shows the normalized contact thermal resistance of SD3933 mounted as indicated by Trials 2, 3 and 4. The contact thermal resistance is a slight function of pressure in Trial 4 until six inch pounds of screw torque is reached.

Figures 8 and 9 compare each mounting approach. Trial 4 yielded the best result for both devices, therefore the mounting recommendation would be 6 inch-pounds minimum of screw torque with thermal compound applied to both the flange and the heatsink, and excess removed with a razor. Trials 2, 3 and 4 would all have greater contact thermal resistance distribution than Trial 1, due to the thermal compound thickness, mounting torque, mounting surface finish and package type.

Each semiconductor device package style and associated mounting method must be evaluated to ensure the contact thermal resistance is optimum for the particular

SD3931-10 Relative Contact Thermal Resistance (°C / W)

Screw torque in-lbs	Trial 1	Trial 2	Trial 3	Trial 4
3	2.86	1.13	1.01	1.00
6	2.26	1.07	1.01	1.00
9	2.07	1.07	1.00	1.00

Figure 8 · Trial results for SD3931-10.

SD3933 Relative Contact Thermal Resistance (°C / W)

Screw torque in-lbs	Trial 1	Trial 2	Trial 3	Trial 4
3	2.61	1.12	1.16	1.02
6	2.23	1.09	1.09	1.00
9	2.15	1.03	1.07	1.00

Figure 9 · Trial results for SD3933.

system and application. The best junction-heatsink thermal resistance ($R\theta_{j\text{-}hs}$) using a thermal compound interface will always be reached by imitating Trial 4.

References

1. "Thermal aspects of flange-mounted r.f. power transistors, " Philips technical note 141.

Author Information

John C. Pritiskutch received a degree in Electrical Engineering Technology from Penn State University in 1982. His prior employment includes Winegard Electronics, Alpha Microelectronics, American Electronic Labs and Acrodyne Communications with design experience relating to solid state power amplifiers. He is a Staff Engineer specializing in Power RF DMOS and LDMOS devices at STMicroelectronics' RF Product Development and Characterization group. He has co-authored three technical papers and recently celebrated his 17th year with ST. He can be reached at: john.pritiskutch@st.com

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