From February 2010 *High Frequency Electronics*

Driving High-Speed ADCs in Wideband Applications

By Marjorie Plisch
National Semiconductor Corporation

Here are examples of input circuit selection for three applications using an analog-to-digital converter for signal processing following an analog front end

A data capture and conversion core, which consists of an analog-to-digital converter (ADC), ADC clock generator and amplifier, is a powerful tool for capturing signals and delivering them for processing. This subsystem can be leveraged to many different applications, depending upon how the analog front-end is configured. This article looks at three different configurations and provides application examples for a communications system, oscilloscope and light detection and ranging (LIDAR) system. Each system requires a selection of AC or DC coupling and a different input frequency range. A block diagram and setup tips are given for each configuration, along with performance results including effective number of bits (ENOB), signal-to-noise ratio (SNR) and spurious-free dynamic range (SFDR). The pros and cons of choosing an amplifier or balun are also explored.

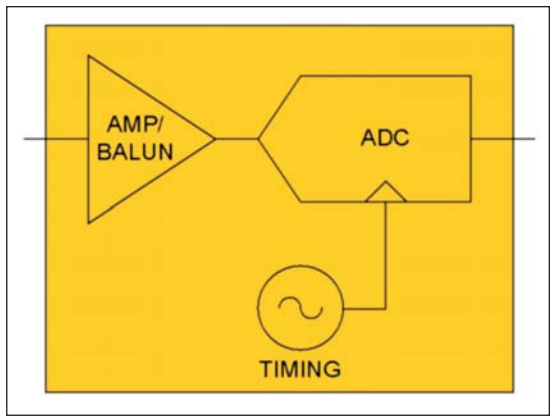

Figure 1 · Block diagram of a data capture and conversion core.

System Core, Configurations and Applications

The basic data capture and conversion core is shown in Figure 1. It includes the ADC, sampling clock for the ADC, and either an amplifier or balun for the ADC input. This core is the analog front-end "workhorse" of

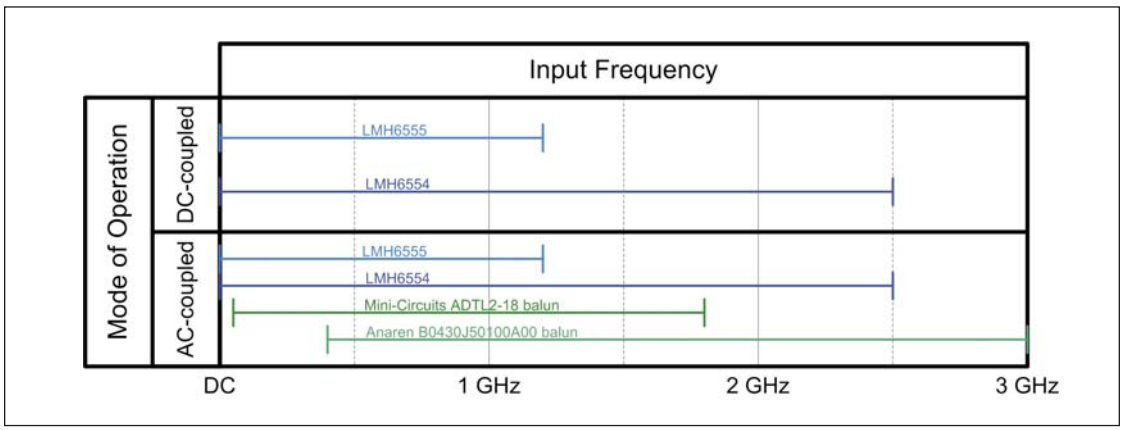

Figure 2 · Front-end configuration selection chart.

many wideband applications.

This same core may be configured for different applications, depending upon the specific system requirements. Two basic requirements of a wideband system are AC/DC-coupling and input bandwidth. Based upon these two, there are three possible system configurations: balun in AC-coupled mode, amplifier in DC-coupled mode and amplifier in AC-coupled mode.

A balun in DC-coupled mode is not a possible configuration because a balun is an inherently high-pass component and does not function down to DC. Figure 2 provides some examples of amplifiers and baluns that are suitable for wideband applications. Note that the given bandwidth is for individual components, but it is necessary to consider system requirements such as ADC bandwidth.

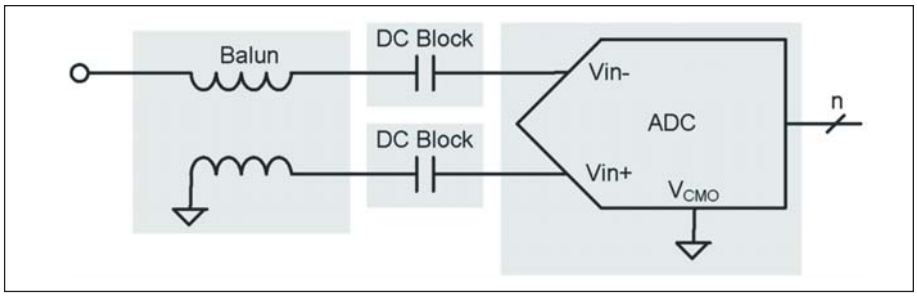

Figure 3 · Balun in AC-coupled configuration.

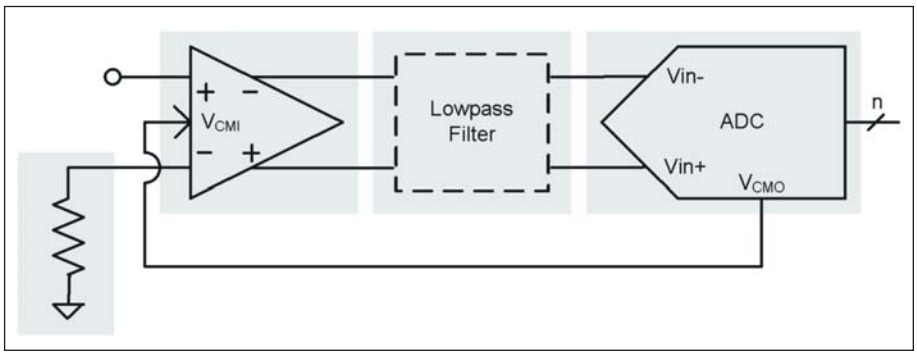

Figure 4 · Amplifier in DC-coupled configuration.

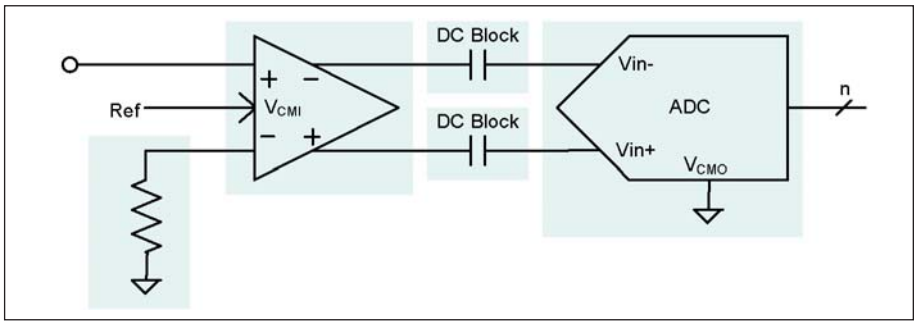

Figure 5 · Amplifier in AC-coupled configuration.

Balun in AC-Coupled Mode

One configuration is with the input signal AC-coupled to the ADC via a balun (see Fig. 3). The balun accomplishes single-ended-to-differential conversion. DC blocks in the signal path ensure that the signal is strictly AC when reaching the ADC analog input. The ADC itself has a control signal to configure it for an AC-coupled input signal; in this example, by grounding the V_{CMO} pin.

An ideal application for this configuration is a wideband communication system. Such systems typically do not require DC in the signal path, so it is not a problem that the balun cannot pass DC. In a typical wideband system, many narrow-band channels are stacked up and transmitted in one wideband signal. For this system, the electrical properties of the balun are important because it must perform consistently across frequency, so that no channel is degraded.

A high-quality balun has good phase and amplitude matching at its outputs; poor matching will result in increased second harmonic distortion because the ADC receives a signal that is not an ideal differential signal. The SFDR performance of the ADC itself is a key metric for this application. This is because a spur generated by the ADC will degrade the ability to distinguish the actual signal in a particular channel.

Amplifier in DC-Coupled Mode

In another configuration, the ADC is driven by an amplifier and DC-coupled (see Fig. 4). The amplifier accomplishes single-ended-to-differential conversion (instead of the balun), and the output is connected directly to the ADC. An ADC typically has an ideal common-mode input voltage, with a certain tolerance for variation. An increasing deviation from the ideal will cause an increasing degradation of performance and, outside the guaranteed range, functional failure.

In DC-coupled mode, the output common-mode of the amplifier provides the input common-mode for the ADC. In this example, the ADC provides a common-mode voltage to the amplifier. Therefore, the V_{CM} from

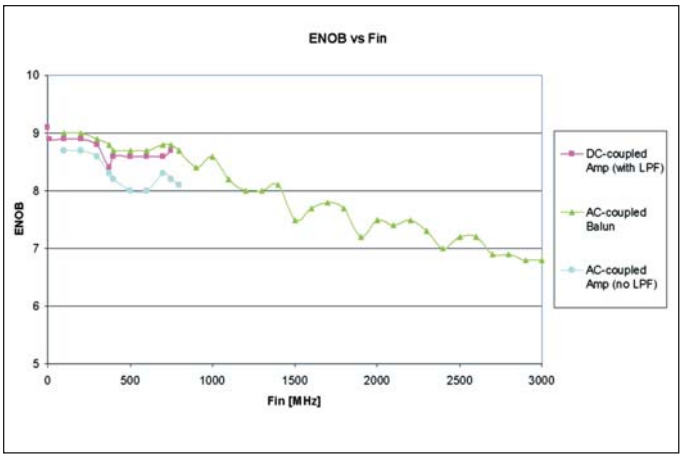

Figure 6 · ENOB typical performance.

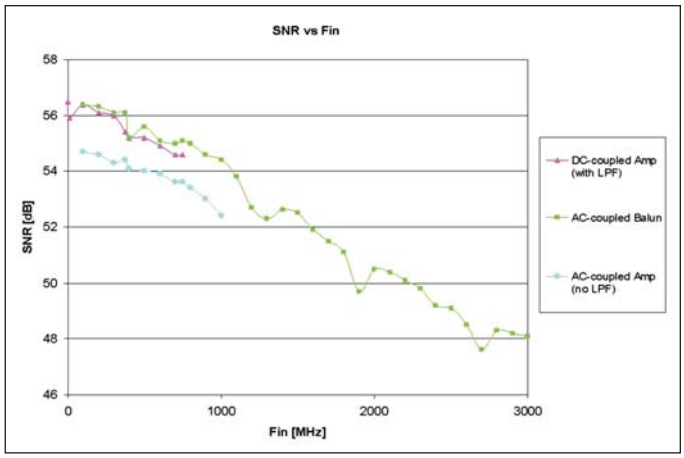

Figure 7 · SNR typical performance.

the amplifier will track the ideal common-mode input voltage of the ADC over temperature and other factors.

Certain test and measurement equipment, such as an oscilloscope, must be DC-coupled so that a probe can measure the DC component of a signal. For this application, the SNR is a key metric, as better system SNR results in a more clear trace. When using an amplifier to drive the ADC (AC- or DC-coupled), it is recommended to use a low-pass filter post-amplifier to bandwidth limit the signal, reduce noise and increase system performance.

Amplifier in AC-Coupled Mode

In the last configuration, an amplifier drives the ADC in AC-coupled mode (hence the DC blocks) similar to the balun in the AC-coupled configuration (see Fig. 5). For this ADC example, the V_{CMO} pin controls are grounded, whether the ADC receives an input common-mode bias externally or generates its own, so it is not possible to use this pin to bias the amplifier. An independently generated bias must be used instead for the amplifier common-mode input.

This configuration can be used for the core of a LIDAR application, which does not typically require DC in the signal path but does need high bandwidth for measurement accuracy. An amplifier in the signal path provides necessary gain, but also creates harmonics and adds noise, which can degrade the overall system SFDR and SNR.

Depending upon the application, these trade-offs must be considered and the best option chosen. This configuration was tested with a high bandwidth amplifier and ADC and the results follow.

Performance Results

The performance for each data capture and conversion core configuration may be independently evaluated to show how that core will affect each application's system performance. The results include ENOB, SNR and SFDR.

Effective Number of Bits

The typical ENOB performance for all three application examples is shown in Figure 6. These results are acquired using the LMH6554 2.5GHz amplifier, Anaren B0430J50100A00 balun and ADC10D1500 10-bit dual 1.5 GSPS ADC. The performance of the DC-coupled amplifier configuration with a low-pass filter (f_c = 800 MHz) is almost as good as that of the AC-coupled balun configuration in the first Nyquist zone (up to 750 MHz). Examining the SNR and SFDR reveals the source of the difference in ENOB performance.

Signal-to-Noise Ratio

The typical SNR performance for all three application examples is shown in Figure 7. Once again, the performance of the DC-coupled amplifier configuration with a low-pass filter is almost as good as that of the AC-coupled balun configuration in the first Nyquist zone.

The performance of the amplifier and data converter are not affected when they are configured for either AC- or DC-coupled mode, but the absence of a low-pass filter reduces the SNR by approximately 1.5 dB. This is because the bandwidth of the amplifier is greater than the first Nyquist zone of the data converter. The data converter folds noise from the amplifier from above the first Nyquist zone back down into it. This out-of-band noise increases the average noise floor and thereby reduces the SNR.

Spurious-Free Dynamic Range

The typical SFDR performance for all three application examples is shown in Figure 8. The performance of the amplifier is on par with the balun up to approximately 250 MHz. Although performance with the amplifier in AC-coupled configuration falls off above that frequency, the DC-coupled amplifier configuration continues to per-

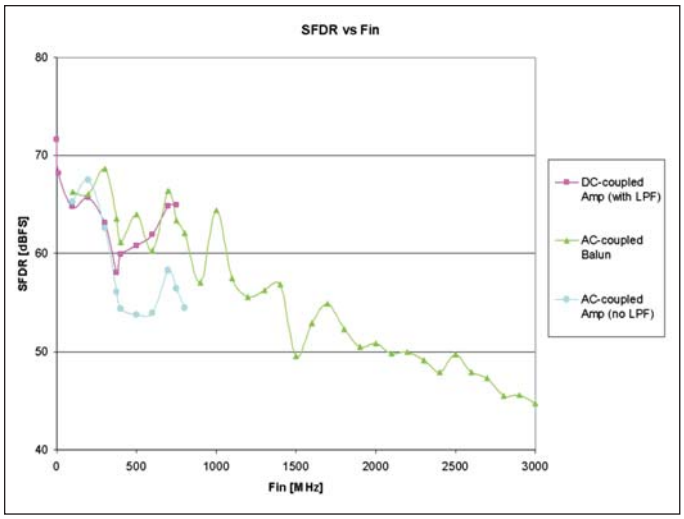

Figure 8 · SFDR typical performance.

form on par with the balun for input frequencies above which the second harmonic is filtered out by the low-pass filter (at 400 MHz),

Conclusion

The same data capture and conversion core can be configured for many different wideband applications. Each system architecture has a set of requirements that lead to specific design choices and trade-offs. By optimally configuring the amplifier, ADC and clock generator, design engineers can easily and quickly build a powerful analog front-end for their wideband system.

Author Information

Marjorie Plisch is an applications engineer in the High-Speed Signal Path Group at National Semiconductor Corporation. She received her BSEE from the University of Illinois, Champaign-Urbana in 2001, a MAPS degree from Multnomah University in 2005, and an MSEE degree from Oregon State University in 2007. Her interests include engineering education, testing and analysis of high-speed ADCs and high-speed ADC applications.