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Generalized Resistive Power Divider Design

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This article presents a design method to achieve unequal power division at the output ports of a two-way resistive power divider

The resistive two-way power splitter, which divides an RF input signal equally between its two output ports, is well documented. This basic divider uses the topology of Figure 1, with all three resistors having a value of $Z_0/3$ [1].

The unequal divider of Figure 2 splits the input power unequally between its two output ports. Design equations have been published for this splitter, where ports 1, 2 and 3 are all matched to the same impedance Z_0 [2].

A power splitter with the same topology as Figure 2 can be designed so that port 3 is matched to some impedance other than Z_0. There are two reasons to design the resistor network for a different impedance at port 3. First, it may be convenient in applications where, for instance, both 50 ohm and 75 ohm outputs are desired. Second, when the resistor network is designed for a port 3 impedance higher than Z_0, there will be less attenuation at port 3, resulting in unequal power at the output ports as well as different impedances.

For instance, if the splitter is designed for 3 dB loss at port 2, with all ports matched to 50 ohms, the attenuation at port 3 will be 15 dB. If we raise the port 3 impedance to 85 ohms, the attenuation at port 3 will only be 8.5 dB. If extreme bandwidth isn't needed, a reactive network can be used to transform the port 3 impedance back to 50 ohms if desired.

Using the circuit topology of Figure 2, resistor values may be chosen so that port 3 is matched to any impedance up to some maximum value. When the maximum allowable output impedance is chosen, the value of resistor R_u becomes infinite, so that the network degenerates to the topology of Figure 1.

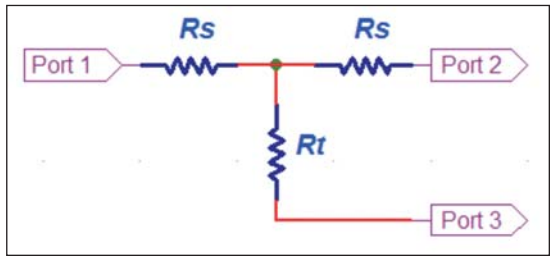

Figure 1 · Resistive power splitter.

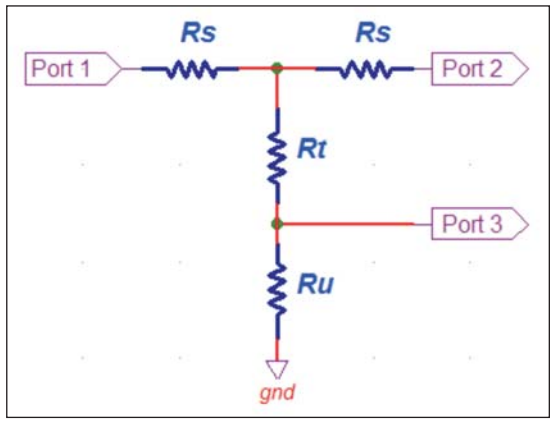

Figure 2 · Unequal resistive power splitter.

Design equations will be presented for an unequal power splitter where the port 3 impedance Z_1 takes on any chosen value between zero and the maximum allowable value Z_{max}.

Design Procedure

Step 1:

Choose a value of attenuation, no greater than 6 dB, for output 1, and design the Tee

attenuator of Figure 3 for that attenuation value, where

Z_0 is the characteristic impedance.
dB_{21} is the attenuation.
α is the voltage gain. $(0.5 < \alpha < 1)$

Given the value of S_{21}(dB), and normalizing Z_0 to unity, we can solve for the resistor values R_s and R_p.

$$Z_0 = 1$$

$$\alpha = A \cdot \mathrm{Log}\left(\frac{S_{21}(dB)}{20}\right) \quad (1)$$

$$A = \left(\frac{1-\alpha}{1+\alpha}\right) \quad (2)$$

$$E = \left(\frac{1-A^2}{2 \cdot A}\right) \quad (3)$$

$$R_s = A \cdot Z_o \quad (4)$$

$$R_p = E \cdot Z_o \quad (5)$$

Step 2:

At this point, we need to choose Z_0, the impedance at output port 2. Any value may be chosen up to a maximum, Z_{max}. We'll compute Z_{max} later.

Step 3:

Now, for R_p, we'll substitute the resistance of R_t, plus the parallel combination of R_u with the Port 3 load impedance Z_1. We require that the resistance of this network, from the top of R_t to ground, be equal to R_p. We also require that when ports 1 and 2 are terminated in Z_0, the resistance seen looking into port 3 be equal to Z_1. These two conditions are represented by two equations, which can now be solved for the two variables R_t and R_u. The following procedure will give the values of R_t and R_u.

$$A = R_s / Z_o \quad (6)$$

$$D = Z_1 / Z_o \quad (7)$$

$$E = R_p / Z_o \quad (8)$$

$$F = E - (A+1)/2 \quad (9)$$

$$G = \frac{D \cdot A + D}{4} + \frac{E \cdot (D - A - 1)}{2} \quad (10)$$

$$T = \frac{-F + \sqrt{F^2 - 4 \cdot G}}{2} \quad (11)$$

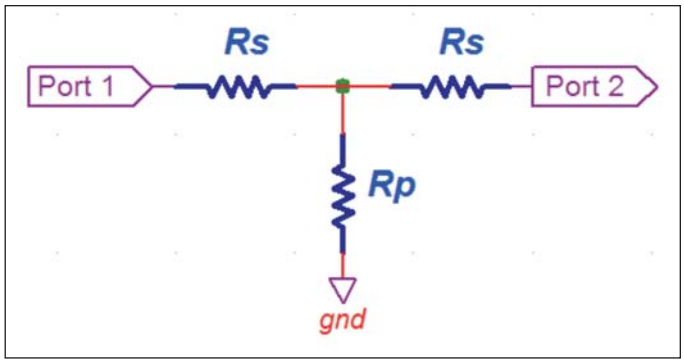

Figure 3 · Tee attenuator circuit, designed according to equations 1-5.

$$U = \frac{1}{\frac{1}{E-T} - \frac{1}{D}} \quad (12)$$

$$R_s = Z_o \cdot A \quad (13)$$

$$R_t = Z_o \cdot T \quad (14)$$

$$R_u = Z_o \cdot U \quad (15)$$

At this point, we have chosen values R_s, R_t and R_u, which satisfy the conditions for a desired attenuation value from Port 1 to Port 2, and for all ports to be matched to the desired impedances Z_0 and Z_1.

It remains to solve for Z_{max}, the maximum allowable value of Z_1, and to find out what attenuation we are left with from Port 1 to Port 3.

Step 4:

It remains to find the maximum allowable value of Z_1. Recall that $D = Z_1/Z_0$, so we'll be solving for the maximum value of D. From Equation 11, we see that the expression under the radical

$$F^2 - 4 \cdot G$$

must be greater than or equal to zero, if R_t and R_u are to have real values.

Z_1 will have its maximum allowable value (Z_{max}) and the attenuation from Port 1 to Port 3 will have its minimum possible value when

$$F^2 - 4 \cdot G = 0 \quad (16)$$

Since the variables F and G are functions of A, D and E alone, we can solve Equation 16 for the value of D, knowing only A and E, which were determined in step 1.

This results in;

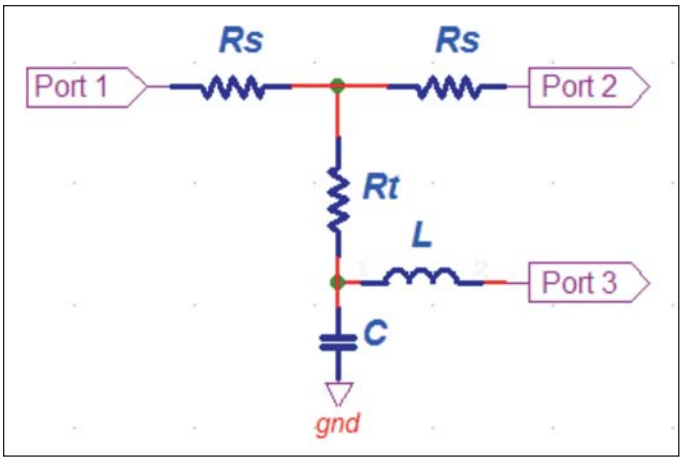

Figure 4 · Power splitter with an additional matching circuit on port 3. This can be used when a limited bandwidth is acceptable at port 3.

$$D_{max} = Z_{max} / Z_o = \frac{E^2 + E \cdot A + E + \frac{(A+1)^2}{4}}{A + 1 + 2 \cdot E} \quad (17)$$

S_{21}(dB)	S_{31}(dB) ($Z_1 = Z_0$)	S_{31}(dB) ($Z_1 = Z_{max}$)	Z_0	Z_{max}
1	–24.7758	–12.646487	50	229.887
2	–18.6824	–9.9209966	50	121.5529
3	–15.0135	–8.3775801	50	85.60054
4	–12.2482	–7.3958399	50	67.74285
5	–9.80391	–6.6125321	50	57.12214
6	–6.45451	–6.0339142	50	50.11901

Table 1 · Comparing S_{31} loss for $Z_1 = Z_0$ vs. $Z_1 = Z_{max}$.

Step 5:

Finally, we solve for dB_{31}, the attenuation from Port 1 to Port 3.

$$H = \frac{1}{\frac{1}{E} + \frac{1}{A+1}} \quad (18)$$

$$J = \frac{1}{\frac{1}{C} + \frac{1}{D}} \quad (19)$$

$$\beta = \frac{H}{(H + A) \cdot \frac{J}{J + T}} \quad (20)$$

$$S_{31}dB = 10 \cdot \log\left(\frac{^2 \cdot Z_1}{Z_1} \right) \quad (21)$$

A couple of examples will illustrate the results that can be obtained:

Example 1: Unequal power splitter with 1 dB loss between ports 1 and 2, and all ports matched to 50 ohms:

Z_0 = 50 ohms
Z_1 = 50 ohms
S_{21} = –1 dB
S_{31} = –24.78 dB
R_s = 2.87 ohms
R_t = 406.8 ohms
R_u = 56.52 ohms

Example 2: Unequal splitter with 1 dB loss between ports 1 and 2, Z_0 = 50 ohms and Z_1 = 75 ohms.

Notice that the loss at port 3 ($-S_{31}$) is 2 dB lower than that of Example 1.

Z_0 = 50 ohms
Z_1 = 75 ohms
S_{21} = –1 dB
S_{31} = –22.72 dB
R_s = 2.87 ohms
R_t = 392 ohms
R_u = 91.37 ohms

Example 3: Unequal splitter with 1 dB loss between ports 1 and 2, and let Z_1 have the maximum allowable value, to minimize the loss at port 3.

Notice that the loss at port 3 now has its lowest possible value at 12.56 dB.

Z_0 = 50 ohms
Z_1 = 229.8 ohms
S_{21} = –1 dB
S_{31} = –12.64 dB
R_s = 2.87 ohms
R_t = 203 ohms
R_u = Open Circuit

As illustrated in Figure 4, a simple L/C matching circuit can be added to the splitter of Example 3, to transform the 229.8 ohm impedance down to 50 ohms at port 3. This results in a splitter with equal impedance outputs, but with much less loss at port 3 than the splitter in example 1. The trade off is that this circuit only works over a limited bandwidth. To transform 229.8 ohms to 50 ohms, the inductor would have a reactance of 95 ohms and the capacitor would have a reactance of 121 ohms at the operating frequency.

Table 1 compares the port 3 loss of the resistive network with all three ports matched to 50 ohms, versus a similar network with port 3 matched to the maximum allowable value of Z_1. It shows that when the S_{21} loss is small, the S_{31} loss can be reduced dramatically by increasing Z_1. When the S_{21} loss is close to 6 dB, little improvement in S_{31} can be achieved.

Note: A convenient "calculator" program can be found online at www.flambda.com, to design power dividers according to the procedure above.

References:

1. D. Pozar, *Microwave Engineering*, John Wiley & Sons 1998, page 361.

2. D. Adams, "Designing Resistive Unequal Power Dividers," *High Frequency Electronics*, March 2007.

Author Information

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