From December 2006 *High Frequency Electronics*

Simulation Results of Phase Noise of PLL Functional Blocks in 0.35 µm SiGe Technology

By M. Ain Rehman
Signal Processing Group

When the necessary performance data could not be found, the author ran his own simulations to obtain PLL phase noise performance on the desired SiGe RFIC process

This brief article presents results obtained from simulation for the phase noise of the following common blocks in a PLL used for a 6.525 GHz fixed frequency source circuit. The simulation was done using the Advanced Design System from Agilent Technologies and based on a 0.35 µm, BiCMOS 60 GHz, SiGe process that provides HBTs and CMOS transistors. Results of the work are presented in a graphical format. From these results the phase noise of the overall PLL was estimated [1]. Phase noise was analyzed from the center to 1000 kHz offset frequency.

The functional blocks that were analyzed include:

(1) The input frequency reference source circuit.
(2) The phase frequency detector.
(3) The VCO and frequency divider chain.

Brief descriptions of the functional blocks:

(1) The input frequency reference functional block consists of a bipolar (HBT) single ended to differential converter that converts a –15 dBm single ended signal into a differential signal used as a clock. Following the single ended to differential converter is a CMOS block that converts the voltage levels from bipolar levels to CMOS levels (3.3 V). The reference frequency is at 10 MHz.
(2) The phase frequency detector uses two D-Type flip-flops, with their D inputs connected to V_{CC} (positive power supply at 3.3 V), their clock inputs connected to the reference frequency input and the feedback divided frequency output. The reset

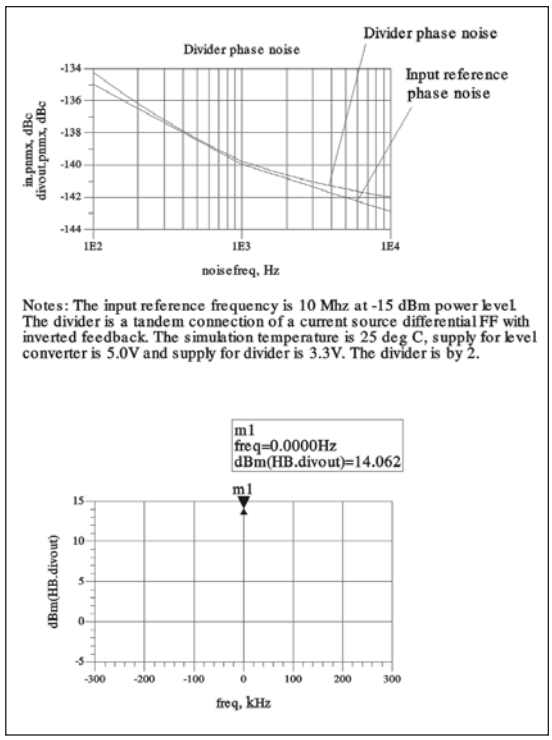

Figure 1 · Reference frequency divider phase noise analysis. The reference output level at 5 MHz is shown in the lower figure. The phase noise at the output is the upper of the two traces in the phase noise plot. The lower trace in the phase noise plot is the reference input phase noise. The upper trace shows the additional noise from the reference divider.

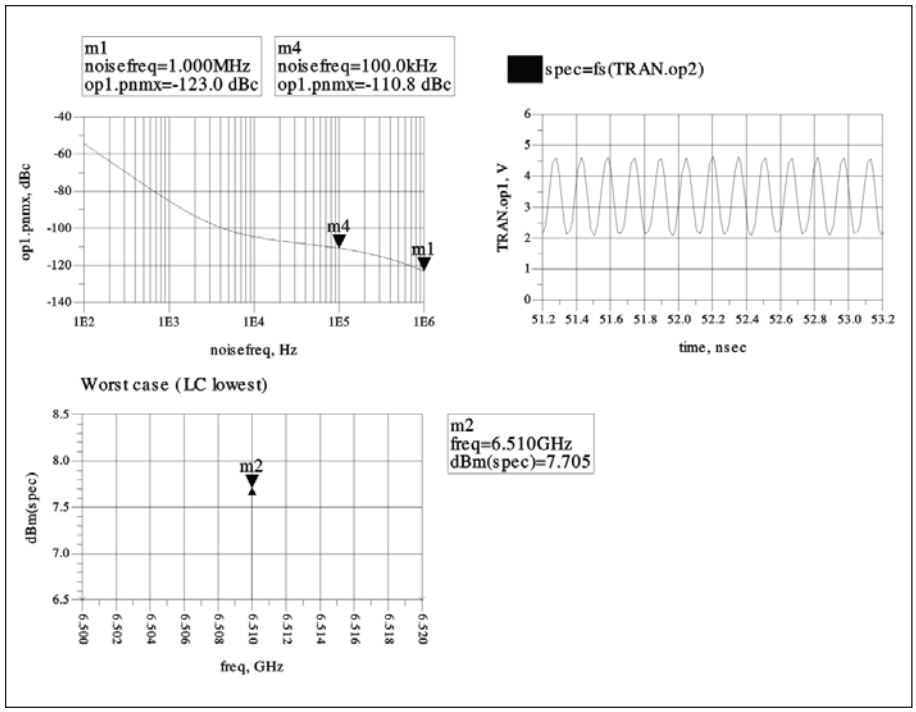

Figure 2 · VCO phase noise as LC tank product swings to the lowest value.

inputs are connected together and connected to a delayed signal from a NAND gate with inverter delays [2]. In order to carry out a reasonable harmonic balance simulation the reset was simulated as a feed-forward signal using one extra tone offset from the clocks by 30 degrees.

(3) The VCO is a cross-coupled LC oscillator [3]. The frequency divider consists of a chain of high speed HBT dividers [4] followed by a CMOS dual-modulus divider. The VCO nominal center frequency is 6.525 GHz.

Results

Figure 1 shows the reference divider phase noise compared to the input phase noise.

Figure 2 includes three plots that show the phase noise characteristic of the VCO under the conditions described. This simulation was done on Agilent ADS using the harmonic balance tool. In this tool the recommended settings of the options for phase noise were: Fundamental Oversample = 4. Order =7.

Figure 3.0 shows the results of the phase frequency detector simulations. The conditions of simulation were as defined above. The frequency of lock is 5 MHz.

Conclusions and Disclaimers

These simulation results are being presented as a source of information only, and are not represented as a thoroughly rigorous analysis. When I was looking for information such as this I had a really difficult time finding it, and proceeded to develop the data for my own needs. The simulations were done using an up-to-date process parameter set on a running commercial process freely available from the vendor.

Since I am a practicing engineer, the article is brief. I welcome questions (and especially comments) within reasonable limits and will respond to them.

Author Information

M. Ain Rehman has been in the industry since 1976, when he graduated with a Masters degree. He worked for Plessey, ITT, GTE and Intel and was one of the founders of Signal Processing Group Inc., in Dec 1987. He has been working as a senior design engineer since. His primary interests are in RFIC/MMIC and analog signal processing techniques. He may be contacted at: Signal Processing Group Inc., Suite 171, 561 E. Elliot Road, Chandler, Arizona 85225; tel: 480-892-1399; e-mail: spg@signalpro.com.

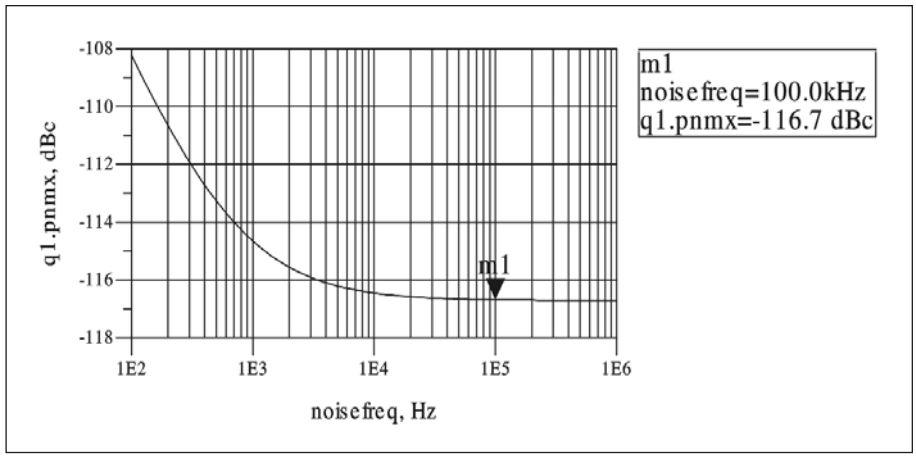

Figure 3 · The phase frequency detector is locked with the delay to get rid of the dead zone.

References

1. Mike Curtin and Paul O'Brien, "Phase locked loops for high frequency receivers and transmitters—Part 2," *Analog Dialogue,* Vol. 33, No. 5, May 1999.

2. Alan B. Grebene, *Bipolar and MOS Analog Integrated Circuit Design,* John Wiley and Sons.

3. Emad Hegazi, Jacob Rael, Asad Abidi, *The Designers Guide to High Purity Oscillators,* Kluwer Academic Publishers.

4. Li Wang, Yao-Ming Sun, Johannes Borngraeber, Andreas Thiede and Rolf Kraemer, "Low Power Frequency Dividers in SiGe: C BiCMOS Technology," *Proc. of the 6th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems* (SiRFIC 2006), San Diego, CA, Jan. 2006, pp. 357-360.