Systemizing the Design of Broadband Class-A RF Power Amplifiers

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This article is the design case history of a broadband medium-power amplifier operating in the 225 to 400 MHz band, including the design methods for obtaining wide bandwidth matching

In the design of broadband microwave amplifiers, there are two techniques that are typically used to achieve gain-flatness across the frequency band of interest. The first technique is done through selective mismatch at lower frequencies of the band where the power gain is significantly higher. This can be achieved by degrading the VSWR at input or output at the low frequency band edge. The second technique is implemented by adding dissipative compensating networks. The input matching network is first designed to achieve minimum VSWR over the full band, and the required gain leveling is then done by adding the lossy equalizing circuit. This network is a constant resistance network and must have a roll-up insertion loss characteristic to compensate the inherent roll-off gain characteristic of the RF transistor over the entire frequency band.

The second technique has been implemented to design a class-A linear power amplifier to operate within the frequency band from 225 MHz to 400 MHz and to deliver 20 dBm output power with more than 12 dB power gain over this communication band. The design strategy will be presented in a systematic manner in this article.

Device Characterization

The available RF power device was the transistor V575. Device characterization includes selecting the optimum bias point and measuring the *S*-parameters at this point. Since linear operation is assumed, the *S*-parameter technique is a powerful tool for modeling the behavior of the selected microwave transistor.

Selection of the Bias Point

The test setup used to select the optimum bias point that ensures safe operation with good linearity is shown in Figure 1.

The transistor is mounted in a broadband 50-ohm system with a means of easily adjusting the bias voltage and current. The signal generator output power is adjusted such that the transistor output power is kept constant. The level of second harmonic power relative to the fundamental power is measured with the aid of a spectrum analyzer and plotted as the bias voltage and current are varied. This process is repeated at several frequencies in the band to check the distortion level over the full operating bandwidth. No attempt was made to match the device for optimum load impedance
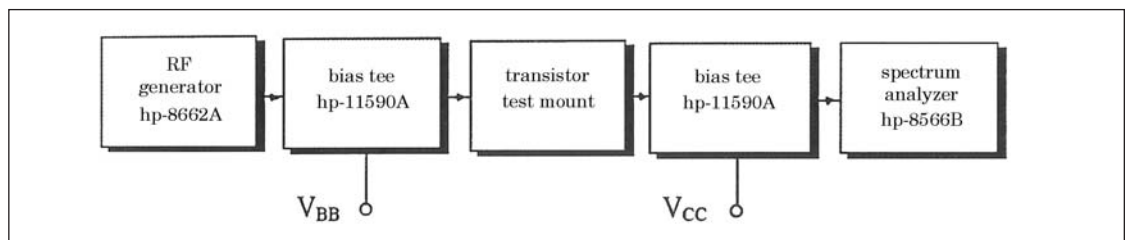

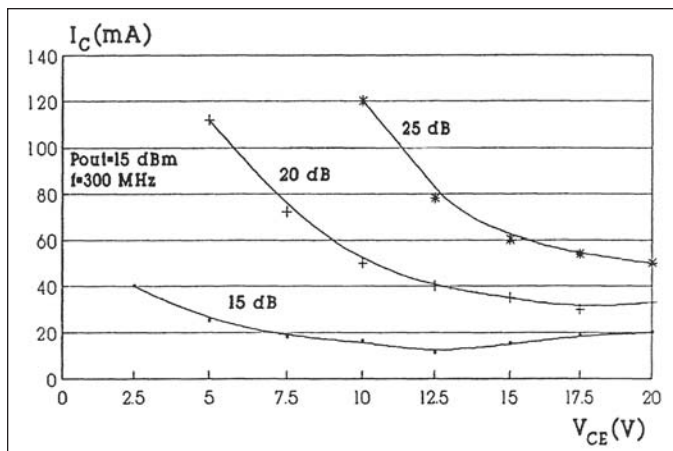**Figure 1 · Test setup to measure the second harmonic level at a given bias point.**

Figure 2 · Contours of 2nd harmonic distortion as a function of I_C and V_{CE}.
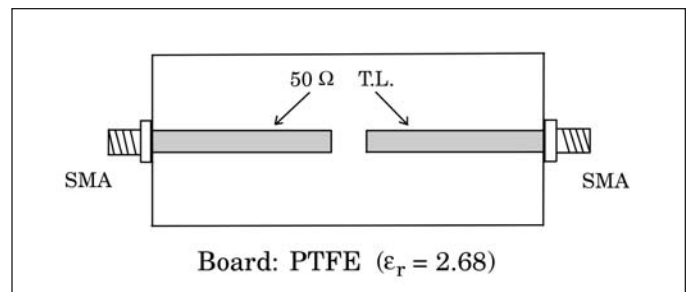

Figure 3 · The test fixture used for measuring the S-parameters of the RF transistor V575.

Figure 4 · Measurement setup to obtain the device S-parameters.

and, for this reason, the contours in Figure 2 are shown for a +15 dBm output power and a test frequency of 300 MHz.

Since the gain is very low, trying to deliver more power into an unmatched load will only cause the transistor to be driven excessively hard. This, in turn, will generate non-linearities within the transistor that may give a misleading picture of its normal operating characteristics. Since distortion in a transistor is also a function of collector load impedance and power level, the distortion contours in Figure 2 should not be considered absolute, but rather as a good first order approximation of the device distortion sensitivity to the quiescent point. The selected bias point was $V_{CE} = 15$ V, and $I_C = 60$ mA.

S-parameter Measurement

After selecting the optimum bias point, the device S-parameters should then be measured at this bias point. For doing this measurement, a transistor fixture was first designed and is shown in Figure 3.

The fixture was built using a high quality PTFE fiberglass board that has minimum losses and can be used at frequencies up to several gigahertz. This test fixture consists also of two 50-ohm microstrip lines and SMA type connectors for signal feeding. The device, which has the hermetic stripline package, was then mounted between the two 50-ohm lines with its case soldered to the ground (bottom) side of the board to ensure good heat transfer.

The measurement setup is shown in Figure 4. The bias tees shown in this figure have the function of isolating the DC biasing circuit from the RF signal and also for blocking the DC current from the network analyzer.

Figure 5 presents a plot of the measured S_{21} and S_{12} parameters, while Figure 6 shows S_{11} and S_{22} plotted on a polar plot and also on the Smith chart.

Note from these plots the –6 dB/octave roll-off in S_{21}

with frequency and the relatively high value of S_{11} that may increase the complexity of the input matching network. The parameters are plotted with a sweep from 100 to 500 MHz.

Design of the Diplexer Network

Gain compensation passive networks can be used to equalize the roll-off in amplifier's gain with frequency and in the same time maintaining low VSWR. These compensating networks are actually constant resistance networks having input impedance independent of frequency. One configuration of such networks is shown in Figure 7 [1]. A possible realization of this network is shown in Figure 8 and is known as the diplexer network [2].

The circuit of Figure 8 can be designed to achieve resonance at the upper band edge f_H. This will ensure that the insertion loss of the network is 0 dB at f_H. It can be shown that the voltage transfer ratio of the diplexer network is given by [2]:

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{1}{1 + j(\omega L_2 / R - 1/\omega C_2 R)} \tag{1}$$
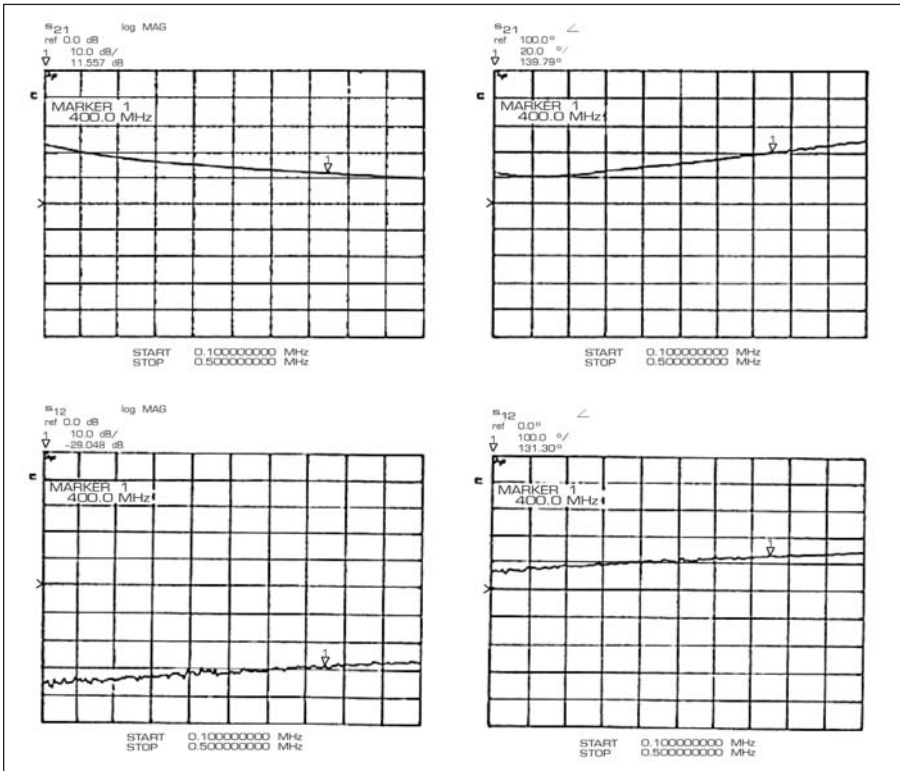$$= \frac{1}{1 + jQ\left(\frac{\omega}{\omega_H} - \frac{\omega_H}{\omega}\right)}$$
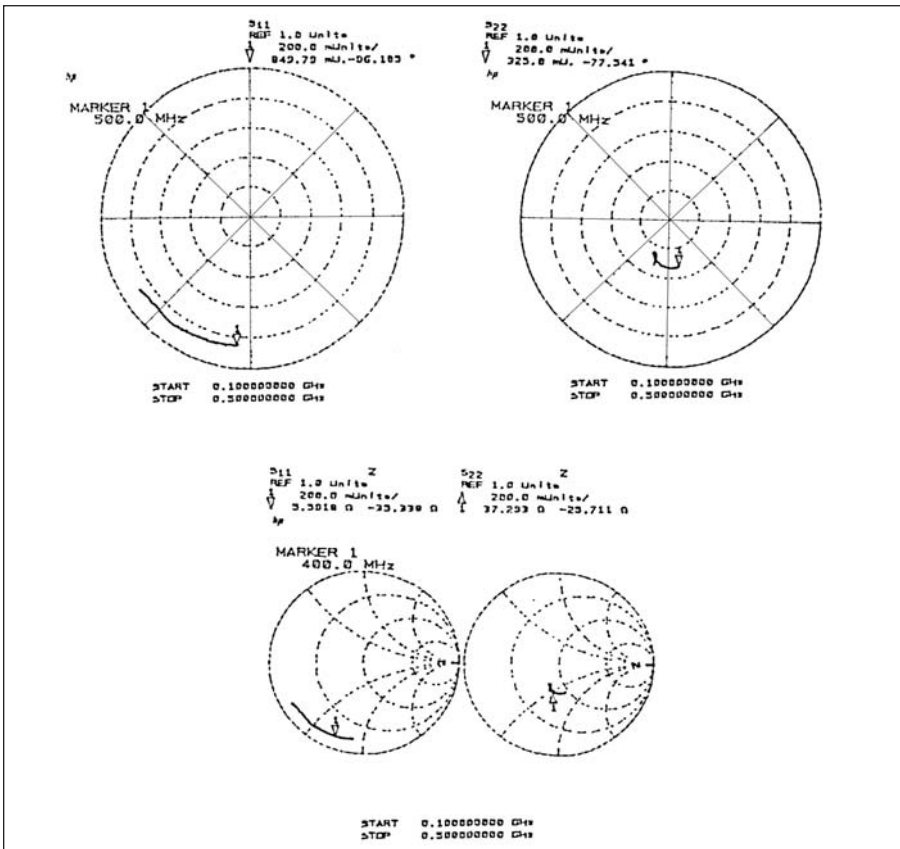
Figure 5 · Measured values of S_{21} and S_{12}.

Figure 6 · Measured values of S_{11} and S_{22}.

where

$$Q = \omega H . L_1 / R = \omega H . R . C_2$$

The insertion loss of the network can be expressed as:

$$IL(\omega) = 10 \log \left| \frac{V_o(j\omega)}{V_i(j\omega)} \right|^2 \qquad (2)$$

$$= 10 \log \frac{1}{1 + \left[Q . \left(\frac{\omega}{\omega_H} - \frac{\omega_H}{\omega} \right) \right]^2}$$

The desired diplexer network insertion loss at f_L is thus given by:

$$IL_d = 10 \log \frac{1}{1 + \left[Q . \left(\frac{f_H{}^2 - f_L{}^2}{f_H \cdot f_L} \right) \right]^2} \qquad (3)$$

Evaluating equation (3) for Q yields:

$$Q = \frac{f_H f_L \left(10^{IL_d/10} - 1 \right)^{1/2}}{f_H{}^2 - f_L{}^2} \qquad (4)$$

The element values of the network are given by:

$$C_2 = 1/(Q.\omega_H.R) \qquad (5)$$

$$L_2 = 1/\left(\omega_H{}^2.C_2\right) \qquad (6)$$

$$L_1 = R/(Q.\omega_H) \qquad (7)$$

$$C_1 = 1/\left(\omega_H{}^2.L_1\right) \qquad (8)$$

where R = 50 Ω.

Design of the Matching Networks

Using the computer program Touchstone, the device was found to be unconditionally stable ($K > 1$) across the full operating band. The input and output matching networks
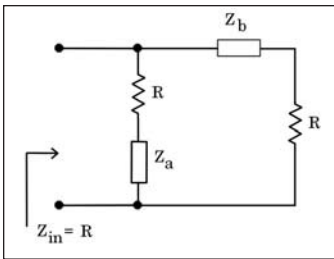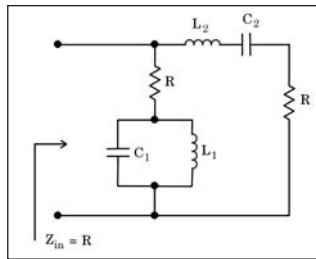
Figure 7 · Constant resistance network.
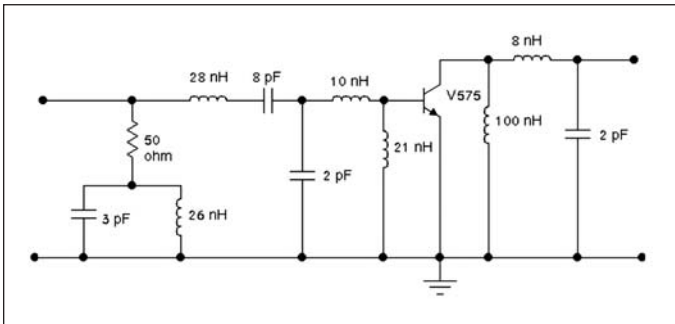

Figure 8 · The diplexer network.

Figure 10 · Simulated power gain versus frequency plot.

Figure 9 · AC schematic diagram of the optimized amplifier circuit.

Figure 11 · The optimized input and output VSWR.

were synthesized to achieve maximum power gain and minimum input and output VSWR. The diplexer network was first designed analytically from the equations presented in section 3 and then optimized with Touchstone. This network was added at the amplifier's input in order to obtain a flat gain response over the entire band. The circuit file written for designing the amplifier is presented in the Appendix and the optimized amplifier circuit is shown in Figure 9. Figure 10 shows the simulated power gain of the synthesized amplifier circuit over the entire band, while Figure 11 presents the input and output VSWR plotted from Touchstone's windows.

DC Bias Network Design

The biasing network must be able to hold the operating point constant over variations in temperature and device parameters. The active bias circuit of Figure 12 was selected for this task. The bias point (15 V, 60 mA) can be maintained constant by adjusting the values of resistors R1, R2 and R3. This active bias circuit is actually a feedback loop that senses the collector current of the RF transistor and adjusts the base current to hold the collector current fixed [3].

The network element values are calculated as follows. The resistor R3 is given by:

$$R_3 = \frac{V_{CC} - V_{CE1}}{\left(1 + 1/h_{FE1}\right)I_{C1}}$$
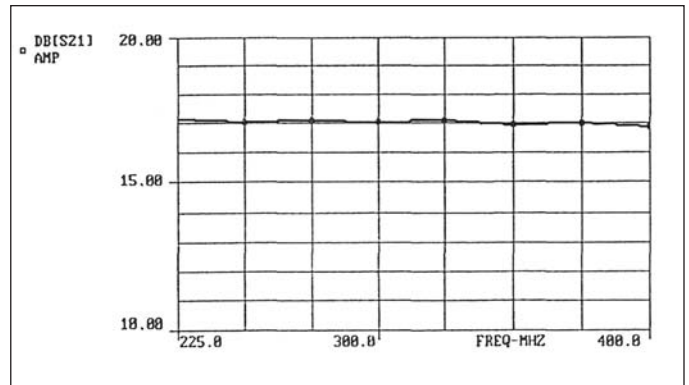

Figure 12 · The active bias network used in the amplifier circuit .
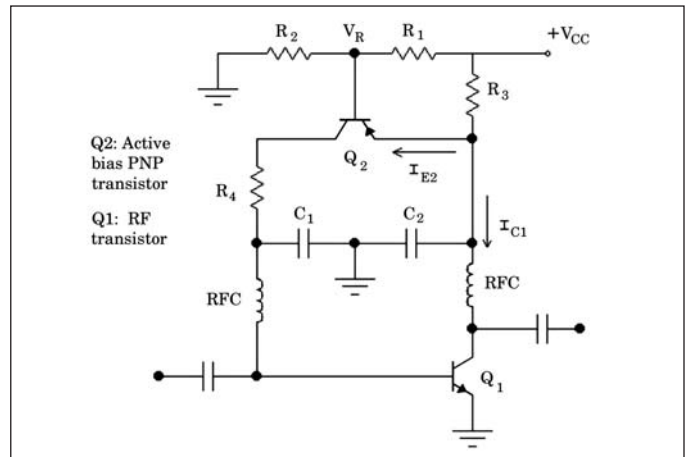
With V_{CC} = 18.5 V and h_{FE1} = 40, R3 = 57 ohms. A standard 56 ohm, 1-watt resistor was used.

The reference voltage V_R is:
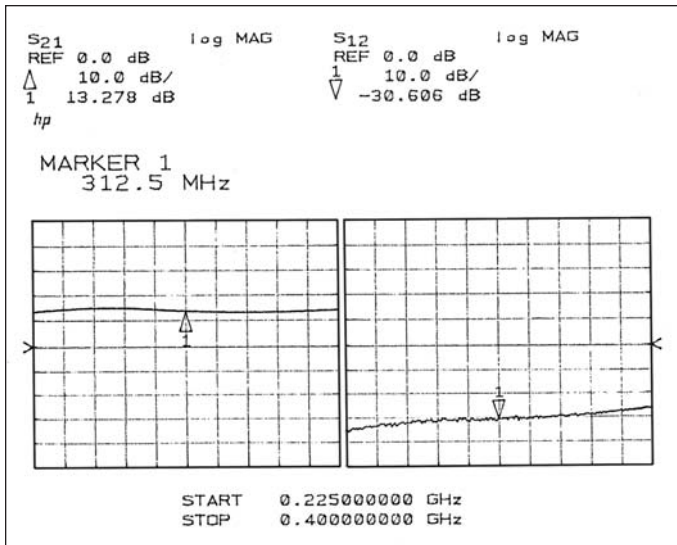
$$V_R = V_{CE1} - V_{EB2} = 15 - 0.7 = 14.3V$$

Figure 13 · S_{21} and S_{12} of the practical circuit measured by the network analyzer.

Figure 14 · Measured input and output VSWR versus frequency .

This voltage is set by:

$$V_R = \frac{R_2}{R_1 + R_2} V_{CC}$$

Then, selecting R_2 = 9.1 kohm gives R_1 = 2.7 kohm. These are standard 1/4-watt resistors.

The low frequency parasitic oscillations of this biasing circuit can be suppressed using suitable bypass capacitors.

Practical Implementation and Results

The amplifier circuit was built on a PTFE fiberglass board. The RF power device was mounted on the board by soldering its case to the lower side ground plane. Other
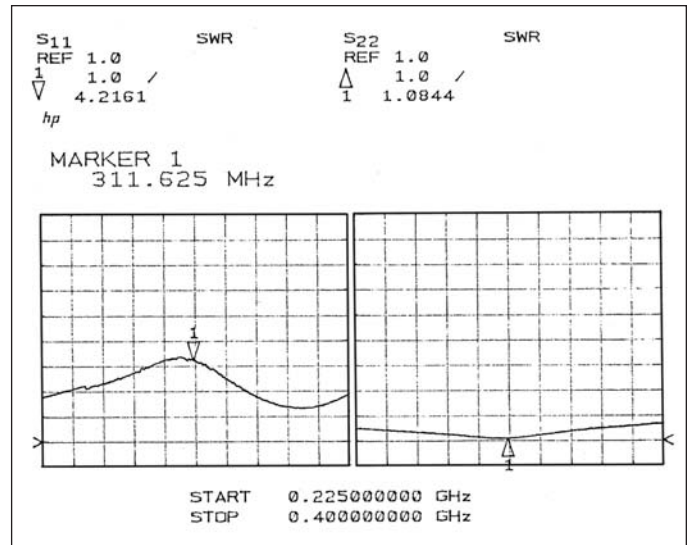

Figure 15 · Output spectrum for input power of 8 dBm and frequency of 313 MHz.

components were placed on the upper side and the necessary ground connections were made through small silver pads. The behavior of each component was checked with the aid of the network analyzer before fixing it on the board. The RF connectors used for signal feeding were of SMA type. In Figure 13, the power gain and the reverse isolation (S_{12}) are plotted by the network analyzer. It is seen that the power gain is 13 ±0.5 dB and the isolation is better than 27 dB at any frequency within the band.

Figure 14 presents the input and output VSWRs drawn in a similar manner. The output VSWR is less than 1.75 and the input VSWR is less than 4.5. The flatness in power gain was obtained at the expense of degrading the input VSWR.

Figure 15 presents the output harmonic levels measured at a fundamental frequency of 313 MHz and input signal power of 8 dBm using the network analyzer. The resulting 2nd harmonic distortion level was found to be better than 35 dB across the full band.

Conclusion

A systematic design procedure for broadband class-A linear power amplifiers has been described and confirmed. The design technique begins by selecting the proper RF device and measuring its S-parameters. IN this example, dissipative broadband matching networks were used to achieve power gain flatness. The computer program Touchstone has been used to synthesize the matching networks and to achieve the desired specifications. This approach is valid as long as linear operation is assumed. Proper mounting and construction techniques should carefully be adopted to implement the practical circuit.
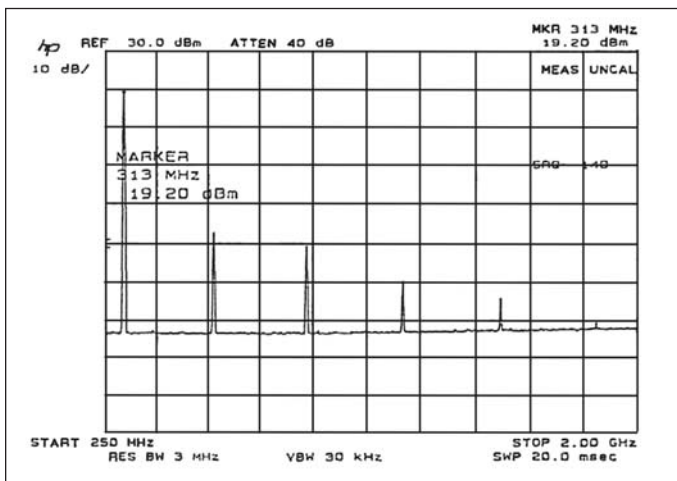
References

1. F.F. Kuo, *Network Analysis and Synthesis*, New York, Wiley, 2nd edition, 1966.

2. A.N. Riddle and R.J. Trew, "A Broadband Amplifier Output Network Design," *IEEE Trans. MTT,* Vol. MTT-30, No. 2, February 1982, pp. 192-196.

3. T.T. Ha, *Solid State Microwave Amplifier Design*, New York, Wiley-Interscience, 1981, Chapter 3.

Author Information

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Appendix

The Touchstone circuit file written for the design of the amplifier circuit is shown below.

```
DIM
        FREQ    MHz
        CAP     pF
        IND     nH
        RES     OH
CKT
!       DIPLEXER     NETWORK
        RES 1 2 R = 50
        IND 2 0 L#10 26 35
        CAP 2 0 C#3 3 20
        IND 1 3 L#8 28 40
        CAP 3 4 C#2 8 30
        DEF2P 1 4 DIPLEXER
        CAP 1 0 C#2 2 30
        IND 1 2 L#2 10 40
        IND 2 0 L#10 21 50
        S2PA 2 3 0 V575
        IND 3 0 L#10 100 120
        IND 3 4 L#8 8 50
        CAP 4 0 C#2 2 30
        DEF2P 1 4 CCT
        DIPLEXER 1 2
        CCT 2 3
        DEF2P 1 3 AMP

OUT
        AMP DB[S21] GR1
        AMP VSWR1 GR2
        AMP VSWR2 GR2
        AMP DB[S12] GR3
        AMP K
FREQ
        SWEEP 225 400 25
GRID
        RANGE 225 400 25
        GR1 10 20 1
        GR2 0 5 1
        GR3 –35 –15 5
OPT
        RANGE 225 400
        AMP VSWR1 < 1.5
        AMP VSWR2 < 1.2
        AMP DB[S21] = 17
```

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