An Electrical-Thermal Coupled Solution for SiGe Designs

By Mike Heimlich

A fast and easy way to co-simulate to reveal the impact of heat on the performance of a circuit.

Introduction

Identifying thermal "hot spots" is becoming an increasingly important task as the design of high-power devices such as microwave monolithic integrated circuits (MMIC)s, modules, and flip chips becomes more complex. The performance of the models in an electrical simulation is heavily influenced by operating temperature, and performing coupled electrical-thermal simulations throughout the design process helps to ensure that once fabricated, the end product will operate as desired.

AWR provides an excellent solution for thermal analysis through AWR Connected™ that combines AWR's Microwave Office® circuit design software with CapeSym's SYMMIC™ thermal analysis software tool. The solution is a fast and easy way to co-simulate in order to reveal the impact of heat on the performance of the circuit in question's phase, gain, efficiency, noise, and intermodulation distortion.

The AWR/CapeSym solution gives designers the ability to do a more temperature-aware design that takes into account not only thermal effects, but also enables designers to detect how hot the device is getting and bring that information back into their electrical simulation to actually see how it is going to affect the performance of the device.

SiGe Design Considerations

Designing in silicon is significantly different from designing in GaAs. In a typical gallium arsenide (GaAs) heterojunction bipolar transistor (HBT), the issue of thermal runaway involves each cell running away with the current if it gets too hot. With a multifinger HBT and center fingers getting hotter, the current can collapse if the center finger ends up taking all the current and the current in the other fingers goes to zero. In the case of silicon germanium (SiGe), the configuration is a group of very small cells that are put together to get the total current. With this configuration, the concern is that of many little heat sources in one small area. If the designer puts them too close together, the peak temperature could be too much for the silicon process to support. Other issues that are different from GaAs design include different materials, no backside metal on silicon, no thru vias, and low output impedance.

Historically, the big issue in SiGe power amplifier (PA) design flows is thermal runaway. With a GaAs HBT the designer would deal with thermal runaway issues by adding ballasting resistors on the base or the emitters to prevent that from happening. However, the issue must be dealt with differently in the SiGe process.

PA Design Considerations

This article describes the design of a Class A Bluetooth PA using SiGe HBT. The device provides 100mW at the antenna and 26 dBm at the PA output with turndown in a reasonably small die area.

The article follows a typical MMIC-style PA design flow, as shown in Figure 1, starting with IV curves to size the transistors based on PAE estimate for Pout, then doing a small signal/linear design to get the passives/bias for approximate gain, and, finally, refining the design with more sophisticated nonlinear analysis, including electro-thermal analysis to find the best bias

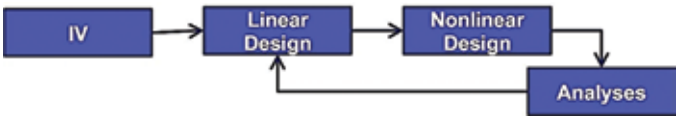

Figure 1 • The typical MMIC-style PA design, including IV curves, small signal design, and, finally, nonlinear analysis, including electro-thermal and EM.

and EM analysis of the passives/bias for optimal performance.

Assuming a 30 percent power added efficiency (PAE) with 3.3V supply, about 400 mA DC would be needed, requiring about 600 individual SiGE HBT devices, as shown in Figure 2.

Foundry PDK Considerations

This example further uses a process design kit (PDK) from the Innovations for High Performance (IHP) Microelectronics foundry, which specializes in silicon. The HBT transistor model in the foundry design kit includes self-heating effects with measurements validated by the foundry that supports arrayed devices and is accurate to 125 deg C. The PDK can be found in Microwave Office software, so it was relatively easy to begin doing the design for this. The device arrays were created that would serve as the thermal PDK.

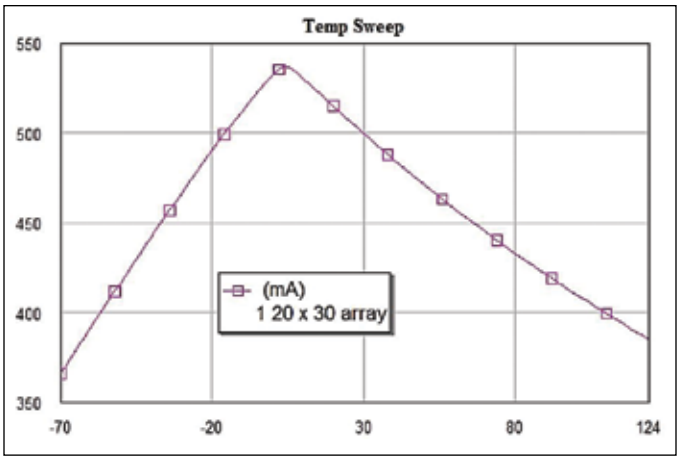

Figure 3 • Temperature sweep in Microwave Office reveals that in low temperatures there is a positive effect, but as the design heats up it produces more current and when it gets hot enough there starts to be a negative effect where the current is reduced.

Electro-Thermal Design Process

The problem is that when the initial thermal analysis was run, it was discovered that if the designer simply takes 600 cells into a 20 x 30 array, it's a pretty small area in which to dissipate over a watt of power in silicon, and the peak temperature wound up being about 180 deg C, which exceeds the maximum temperature for the process.

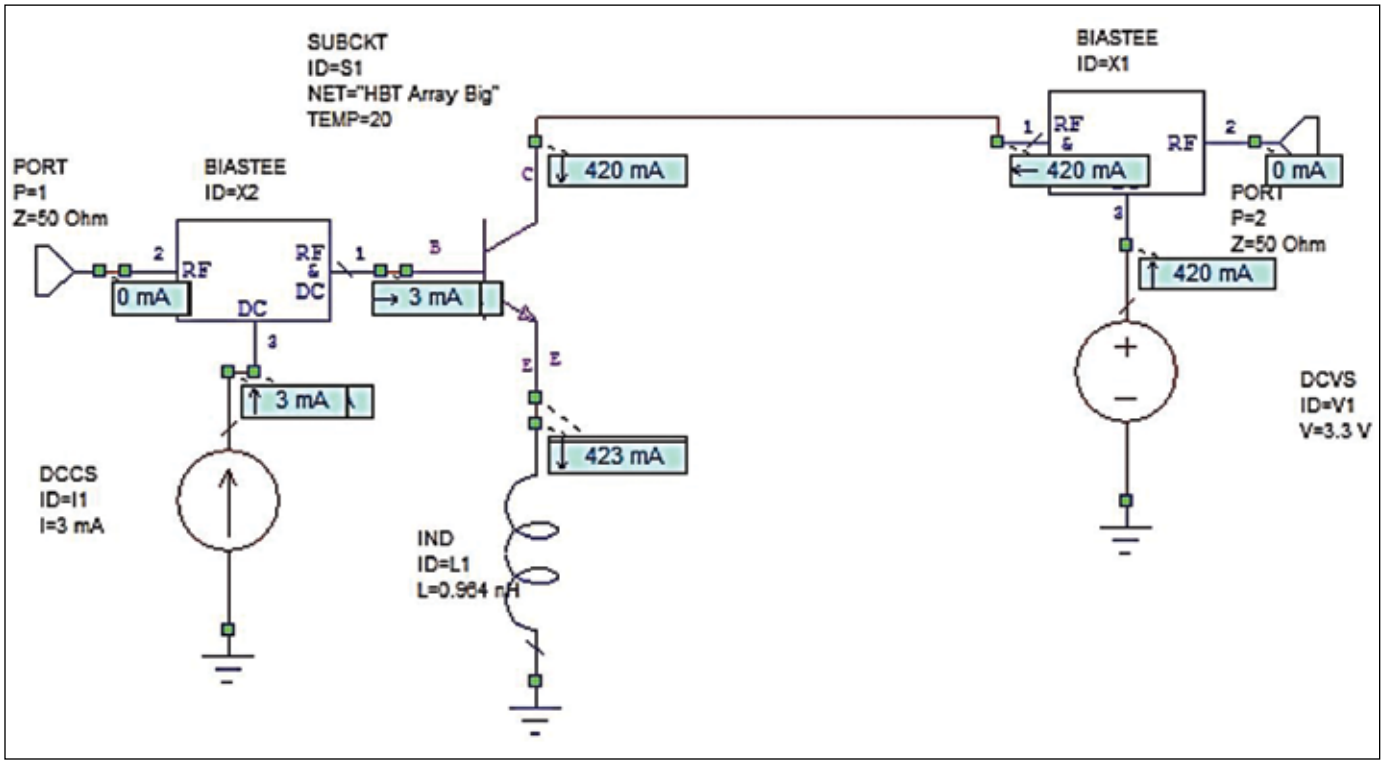

Figure 2 • For a 3.3V supply with 30 percent PAE, 400 mA DC would be needed, requiring 600 SiGe HBT devices.

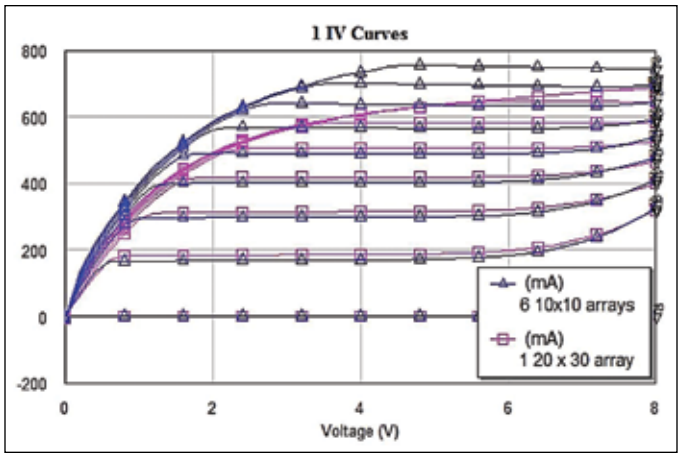

Figure 4 • For two IV curves, one for a single 20 x 30 array and the other for six device arrays, each with 100 cells, a little better DC bias results with the six arrays than with the single array.

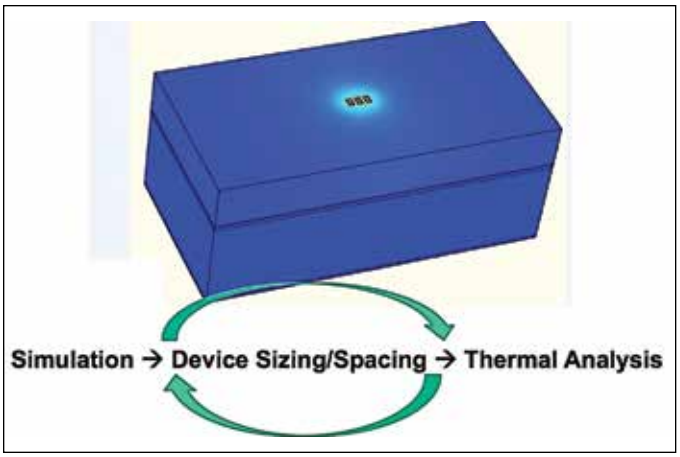

Figure 5 • You can easily evaluate different layouts for the best thermal performance by exporting the layout into SYMMIC for thermal analysis and then bringing the information back into Microwave Office.

It was pretty clear something more would have to be done other than simply making one big array.

One interesting thing to note about the thermal effects in this design was that the designers saw both positive and negative feedback. As shown in the 20 x 30 array graph in Figure 3, if a temperature sweep is done in Microwave Office, the software reveals that in low temperatures there is a positive effect, but as the design heats up it produces more current and when it gets hot enough there starts to be a negative effect where the current is reduced.

Another interesting thing to note is that as the user changes the shape of the array, the shape of the IV curve can actually be changed because of these thermal effects. Figure 4 shows two IV curves, one for a single 20 x 30 array and the other for six device arrays, each having 100 cells. It can be seen that a little better DC bias results with the six arrays than with the single array.

The Microwave Office/SYMMIC solution enables designers to easily export their layout from Microwave Office into SYMMIC, do the thermal analysis, get their temperatures and bring the information back into

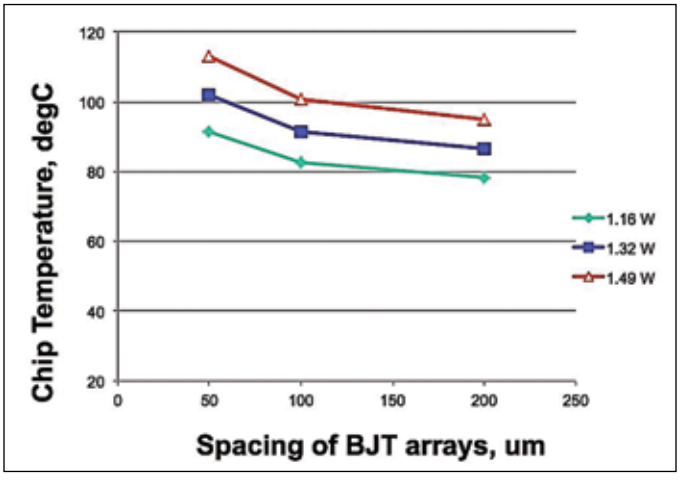

Figure 6 • A series of simulations done with SYMMIC shows how users can change the spacing between the arrays to improve performance.

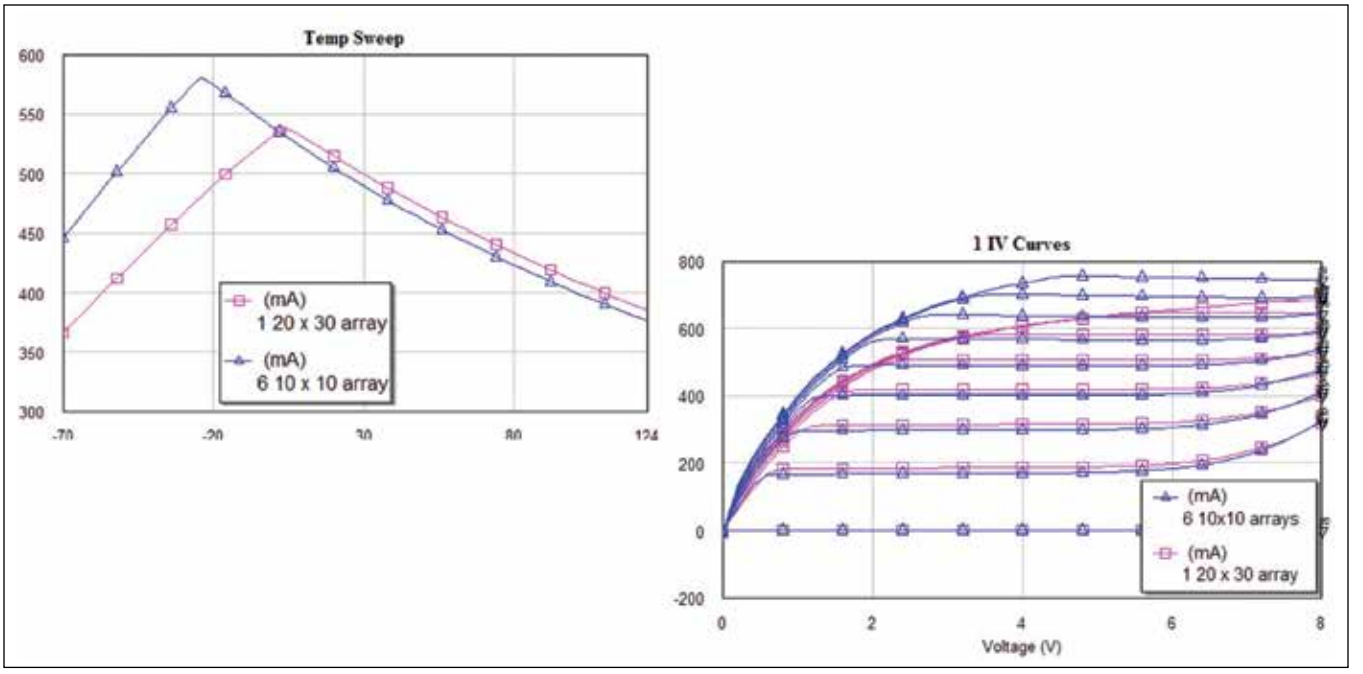

Figure 7 • When the design is done with the six smaller device arrays, designers can actually shift where the switch from positive thermal effects to negative thermal effects occurs, and they can shift down beyond the desired operating range.

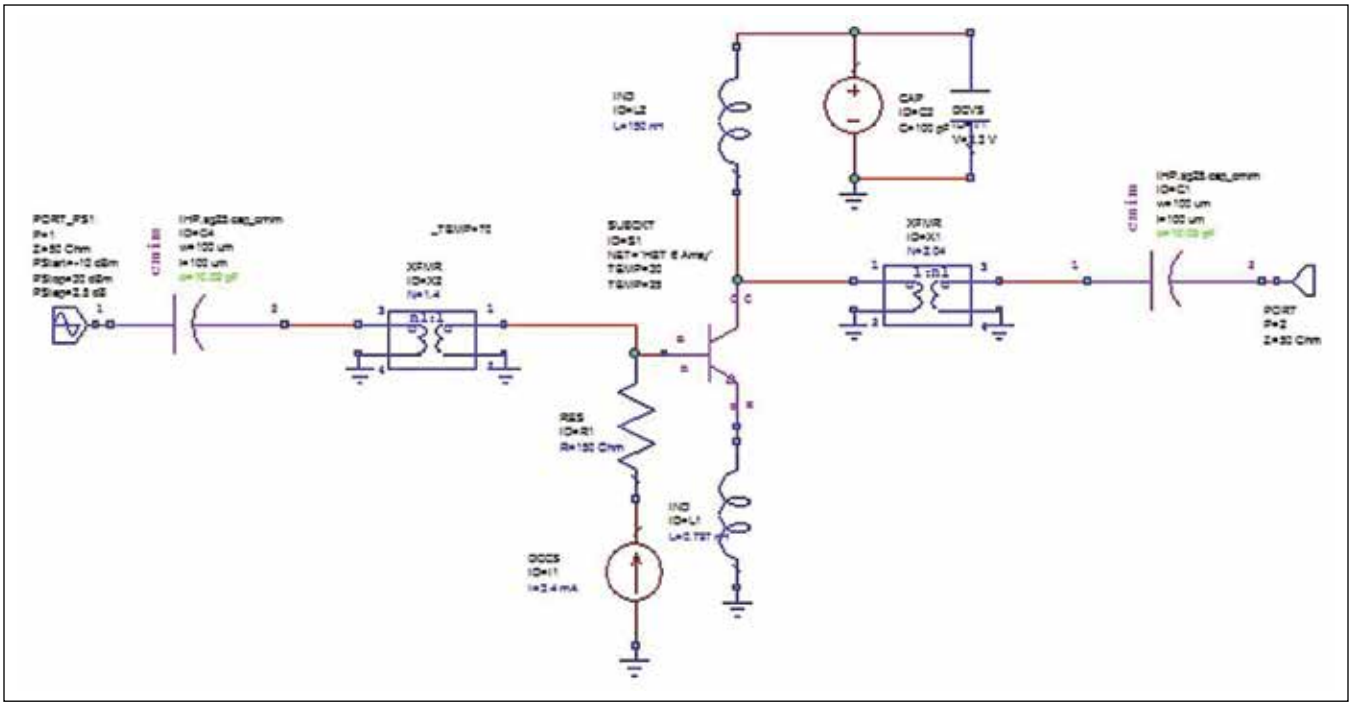

Figure 8 • Once the size and layout of the arrays is optimized and set, the linear design can be done.

Microwave Office, where the ways in which the layout of the arrays would affect thermal performance can be evaluated. You can also include interconnects such as solder bumps in that type of analysis, which can be laid out and optimized relative to the devices to improve thermal analysis (Figure 5).

Figure 6 shows a series of simulations done with SYMMIC and how users can change the spacing between the arrays to improve performance. The graph shows three different levels of total power and the peak temperature over the entire chip. As can be seen, the die size

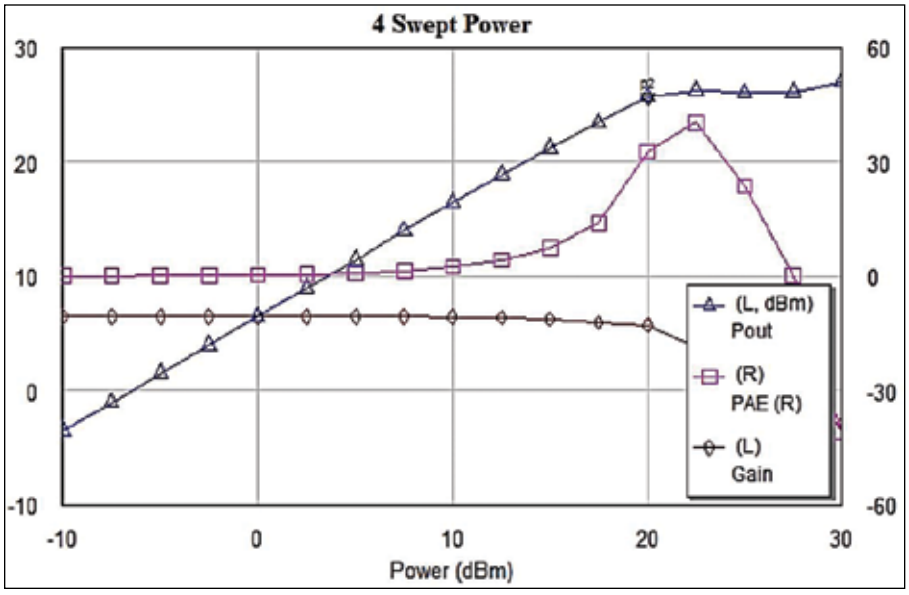

Figure 9 • The nonlinear design, actual performance in terms of PAE, output power, and gain, all showing that performance goals have been met.

of 1 x 2mm is a contributing factor, while the array position on the die is less so.

Interestingly, when the design is done with the six smaller device arrays, designers can actually shift where the switch from positive thermal effects to negative thermal effects occurs, and they can shift way down beyond their desired operating range (Figure 7). These two capabilities are key motivators for using thermal analysis to optimize the size of the device arrays and their layout BEFORE starting the design.

Once the size and layout of the arrays is optimized and set, then the linear design can be done (Figure 8). Unlike GaAs, in this SiGe design designers have to do off-chip impedance matching and inductors.

Figure 9 shows the nonlinear design, the actual performance in terms of PAE, output power, and gain, and reflects that performance goals set at the beginning of the design have been met.

Conclusion

The key learning from this application is that, while in GaAs PA design thermal analysis can be saved to the end or not done at all, in silicon thermal analysis cannot be put off until the end of the flow. It must be considered up front in order to understand and take into account how thermal considerations are going to affect the initial design. The size of the arrays and the best way to lay them out relative to the other devices on the chip are important considerations that must be determined before the linear design is started. New solutions like AWR Connected for CapeSym SYMMIC provide an integrated electro-thermal approach that simplifies the entire design process.

About the Author:

Dr. Michael Heimlich is a Concentration of Research Excellence (CORE) professor in wireless communication at Macquarie University and teaches undergraduate classes in electronic devices and systems and advanced digital and RFIC design. Prior to joining Macquarie, Dr. Heimlich was AWR's director of product marketing for Microwave Office circuit design software. Dr. Heimlich received his BSEE, MSEE and PhD from Rensselaer Polytechnic Institute.