Exploring Decimation Filters

By Arash Loloee, Ph.D.

An overview of decimation filters, along with their operation and requirements.

Introduction

Delta-sigma analog-to-digital converters (ADCs) are among the most popular converters that are suitable for low-to-medium speed and high-resolution applications such as communications systems, weighing scales and precision measurement applications. These converters use clock oversampling along with noise-shaping to achieve high signal-to-noise ratio (SNR) and, thus, higher effective number of bits (ENOB). Noise-shaping occurs when noise is pushed to higher frequencies that are out of the band of interest. When the out-of-band noise is chopped off, SNR increases. After noise-shaping, the sampling rate is reduced back to its Nyquist rate by means of decimation filters. In fact, delta-sigma converters can be partitioned into two main building blocks: modulator and decimation filters. With a good understanding of these building blocks you can arrive at a robust and efficient design. Each of these main building blocks, in turn, is made of several different building blocks themselves.

Unlike conventional converters that sample the analog input signal at Nyquist frequency or slightly higher, delta-sigma modulators, regardless of their order, sample the input data at rates that are much higher than Nyquist rate. The oversampling ratio (OSR) usually is expressed in the form of 2^m, where m=1,2,3,… The modulator is an analog block in nature that needs little accuracy in its components. Thus, the burden of design can be pushed onto the decimation filter. The most important role of a decimation filter is to decrease the sampling rate by discarding every few samples. Presented in this article is a quick overview of decimation filters, along with their operation and requirements. Their requirements are based on the order of the delta-sigma modulator used in the converter, along with the overall number of bits being output by the ADC. Also provided is a description of cascaded integrator-comb (CIC) filters, along with filter requirements for a given delta-sigma ADC.

CIC Filters

Decimation filters perform several important functions. The first is to down-sample and reduce the clock rate. The second is to remove the entire out-of-band signals and noise. In practice decimation is done in multiple stages by cascading several smaller decimation factors, such that the overall decimation factor equals the product of decimation factors of the individual decimation stages. One big advantage of multistage filtering is the power reduction made possible by making the subsequent components operate at lower sampling rates. The power reduction, along with reduction in number of filter tabs makes a multistage approach more desirable.

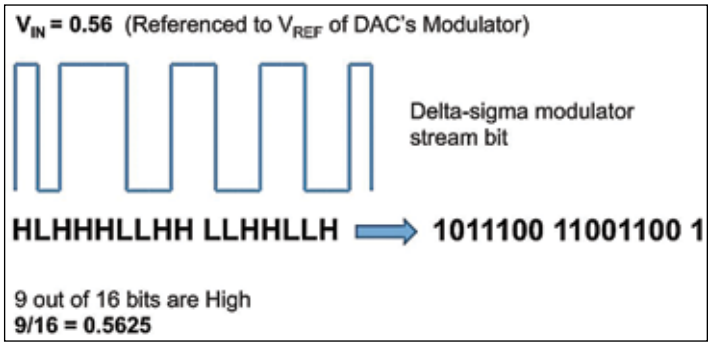

Figure 1 • A pictorial presentation of CIC filter operation.

A first-order CIC filter is made of an integrator and a Comb stage. A switch between these two stages performs the down sampling operation. To

have a better understanding how decimation filters operate, we created an example. Note that in a delta-sigma converter, the decimation filter is placed after the modulator. Assume a first-order delta-sigma modulator is used to generate a bit stream at the modulator's output (**Figure 1**).

According to Figure 1, the 16 consecutive samples obtained from the modulator are added and the sum is divided by 16 to get the average value of reconstructed input. In this example, for an input of 0.56V, 9 out of 16 bits are high. Thus, the ratio of highs to total bits constructs a value that is very close to the input signal. This example shows that in order to compute the average of D samples, we need D-1 summation and a multiplication by 1/D (which indeed is dividing the sum by D). To get the average of D samples we can write (Equation 1):

$$Y(n)=[x(n)+ x(n-1)+ x(n-2)+ x(n-3)+ x(n-4)+\ldots+ x(n-D+1)]/D \quad \text{Eq.1}$$

Equation 1 can be written in Z-Domain (Equation 2):

$$Y(z)=[X(z)+ X(z).z^{-1}+ X(z).z^{-2}+X(z).z^{-3}+\ldots+ X(z).z^{1-D}] / D \quad \text{Eq.2}$$

Now Equation 2 can be simplified to Equation 3:

$$Y(z)=X(z).[1+ z^{-1}+ z^{-2}+ z^{-3}+\ldots+ z^{1-D}] / D \quad \text{Eq. 3}$$

The transfer function H(z) can be calculated as Equation 4:

$$H(z)=\frac{Y(z)}{X(z)} \quad \text{Eq. 4}$$

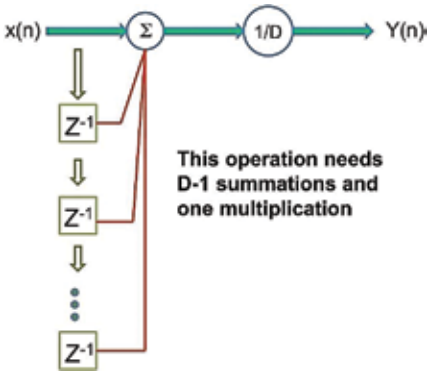

Figure 2 • Conceptual implementation of Equation 3.

Equation 4 can be simplified in the general form of Equations 5 and 6:

$$H(z)=[1+ z^{-1}+ z^{-2}+ z^{-3}+\ldots+ z^{1-D}] / D \quad \text{Eq. 5}$$

$$H(z)=\frac{1}{D}\sum_{0}^{D-1} z^{-n} \quad \text{Eq. 6}$$

To avoid D-1 summations and multiplication, commonly a CIC filter is used to achieve a similar result. A CIC filter typically is made of an integrator followed by a subtractor. Before the signal is sent to a Comb filter, it is decimated (down sampled) by a factor of M. Then the down-sampled data is passed to the Comb section. The architecture of a single-stage CIC filter is shown in **Figure 3. Figure 4** shows the diagram for a multistage CIC filter. In a CIC filter architecture, note that there is no multiplication (multiplier), as it is required if you intend to implement Equation 6 directly.

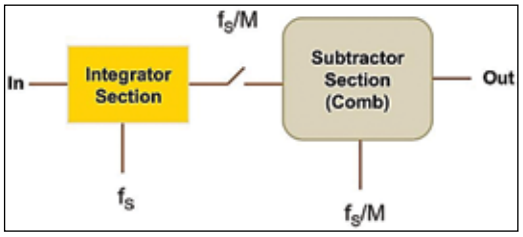

Figure 3 • Conceptual diagram for single-stage CIC filter.

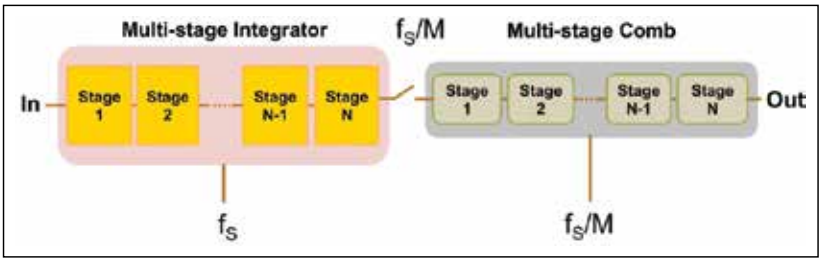

Figure 4 • Illustration of a multistage CIC filter.

In fact, the lack of need for a multiplier is an advantage of this type of filter. The transfer function of the first-order filter shown in **Figure 1** can be written as Equations 7 through 8b:

$$Y(z)(1-z^{-1}) = X(z)(1-z^{-D}) \qquad \text{Eq.7}$$

$$\frac{Y(z)}{X(z)} = \frac{1-z^{-D}}{1-z^{-1}} \qquad \text{Eq.8A}$$

$$H(z) = \frac{1-z^{-D}}{1-z^{-1}} \qquad \text{Eq.8B}$$

Looking into the transfer function of a CIC filter, the transfer function of integrator (accumulator) and subtractor (comb) is recognizable (Equations 9 – 10):

$$H_{\text{int}}(z) = \frac{1}{1-z^{-1}} \qquad \text{Eq.9}$$

$$H_{comb}(z) = 1-z^{-D} \qquad \text{Eq.10}$$

If a multistage configuration (**Figure 4**) is used to implement a CIC filter, its transfer function can be written as Equation 11:

$$H(z) = H_{\text{int}}^{K}(z)H_{comb}^{K}(z) = \frac{(1-z^{-D})^{K}}{(1-z^{-1})^{K}} \qquad \text{Eq.11}$$

where, K is the number of stages used in the filter.

As mentioned earlier, a decimation operation takes place right after the integrator stage, so this must be taken into account. For a decimation factor of M, the transfer function should be revised as Equation 12:

$$H(z) = H_{\text{int}}^{K}(z)H_{comb}^{K}(z) = \frac{(1-z^{-DM})^{K}}{M^{K}(1-z^{-1})^{K}} \qquad \text{Eq.12}$$

Note that in **Figures 3 – 4,** the integrators operate at a high sampling rate (fs), whereas the Comb filter operates at a down sampled frequency (fs/M). The CIC transfer function has the geometric series form of sum, which can be simplified as Equation 13:

$$\left(\frac{1-z^{-DM}}{1-z^{-1}}\right)^{K} \equiv \left[\sum_{0}^{DM-1} z^{-1}\right]^{K} \qquad \text{Eq.13}$$

Filter Requirements

Equation 13 implies that a CIC filter is equivalent to a cascade of K uniform FIR filter stages. It is interesting to note that despite the presence of integrators, which have infinite impulse response, the CIC filter has a rectangular impulse response. Furthermore, since all coefficients are unity and therefore symmetric, the CIC filter has a linear phase response and constant group delay. The order of the filter, K, has to be at least one higher than the order of delta-sigma modulator, as shown in Equation 14:

$$K \geq \Sigma\Delta_{order} + 1 \qquad \text{Eq.14}$$

For example, if a second order modulator is used, at least a third-order filter is needed. The number of bits generated at the output of the filter, generally referred to as output word size, is greater than that of the input to the filter. The word size is a function of decimation factor and the order of the filter itself. If B_{IN} is the size of the bit stream coming from a modulator, then the word size, P, can be calculated using Equation 15:

$$P = K \log_2 M + B_{in} \qquad \text{Eq.15}$$

where M is the decimation factor.

In architectures where the modulator generates a one-bit stream of codes, the equations are reduced to Equation 16:

$$P = K \log_2 M + 1 \qquad \text{Eq.16}$$

From Equation 16 you can see that for every added order of decimation filter, the output word size increases by a factor of $\log_2 M$. For example, if the over sampling ratio is 32, increasing the order of filter (K) from three to four increases the bus size by five additional bits. Note that the final bus size is much greater than the actual needed bit size of a delta-sigma ADC. Thus, truncation has to be done to the bus size to obtain the final number of bits indicated by an ADC converter. This truncation is achieved by discarding a certain number of unneeded least significant bits (LSB). If $P_{DISCARD}$, P_{WORD} and N are the number of bits to be discarded, the output word size and the ADC's number of bits, respectively, the number of bits to be discarded can be calculated from the Equation 17:

$$P_{DISCARD} = P_{WORD} - N \qquad \text{Eq.17}$$

The conventional way of implementing a CIC filter is to synthesize it using a register transfer level (RTL) code. For a classical and textbook approach, use a digital integrator and differentiators as the main building blocks. A digital integrator (**Figure 5**) comprises a full adder followed by a D-flip flop in a feedback loop. The digital differentiator is made of the same two components where the full adder follows the flip flop and no feedback is presented.

CIC Filter Macromodel

A full macromodel was designed for TI's ADS1278 delta-sigma ADC. The macromodel was built using a sixth-order modulator, followed by a seventh-order filter with an oversampling ratio of 512. The modulator's output was a one-bit word. Therefore, using Equation 15, the final output bus size was calculated to be 64 bits. This is a 24-bit delta-sigma ADC, so the bits need to be truncated accordingly. To achieve this, the first 40 LSBs were discarded and the remaining 24 bits used as the final output bits.

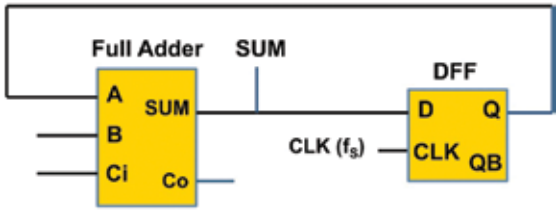

Figure 5 • Schematic of digital integrator.

Figure 7 shows the bit-stream that comes out of the delta-sigma modulator macromodel with a sixth-order modulator. A seventh-order CIC filter was modeled and used along with the modulator's macromodel. The full macromodel was simulated with a 500 Hz sine wave input signal that was sampled at various clock rates with decimation rate of 512. The final output of the delta-sigma ADC is a 24-bit bus, which is then connected to an ideal 24-bit DAC. By doing this we can reconstruct the analog

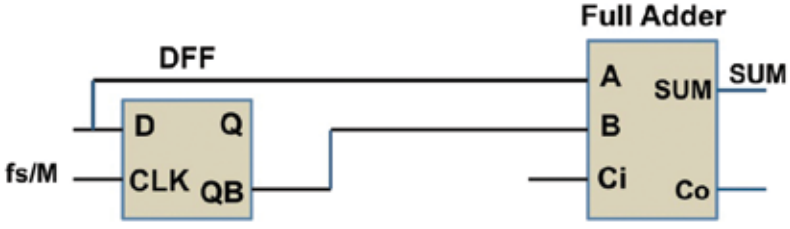

Figure 6 • Schematic of digital differentiator.

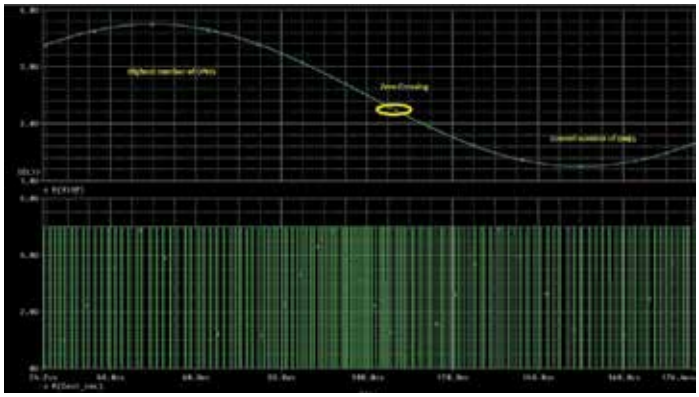

Figure 7 • The resulting bit-stream from a delta-sigma modulator macromodel.

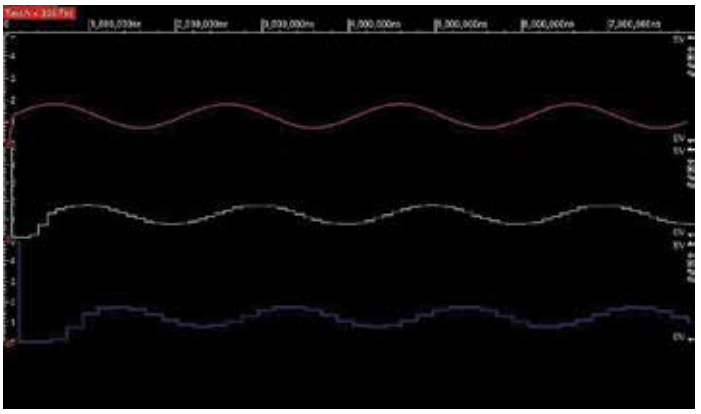

Figure 8 • Reconstruction of an input signal by passing the CIC output through an ideal DAC.

voltage representation of the output code so it could be compared to the original analog input. This approach can verify the correctness of handshaking between the blocks and validate the full operation. **Figure 8** shows the results of a simulation for sampling clock rates of 25 MHz, 5 MHz and 1.6 MHz with decimated clock rates of 48.828 KHz, 9.7656 KHz and 3.125 KHz, respectively.

An important point to keep in mind is that CIC filter operation is done in 2s complement. The modulator output is straight binary. The input to conventional digital-to-analog converters (DACs) also is binary. Thus, the modulator output needs to be converted to 2s complement prior to being passed to a CIC filter so the CIC filter can operate on the 2s complement data. In the end, the decimation filter output should be converted back to binary, if it is going to be used by other conventional blocks. Therefore, in the delta-sigma macromodel two additional blocks are inserted before and after the CIC filter. The first block performs a conversion of binary-to-2s complement, while the block at the other end converts 2s complements back to binary codes to be used with an accompanied ideal DAC. The components used in the delta-sigma macromodel are presented in **Figure 9.**

Summary

We covered the basics of decimation filters along with their building blocks. The main idea of this work is to recognize the requirement of CIC filters that follow delta-sigma modulators as a part of delta-sigma data converters. The required order of filter, number of bits to be kept and number of bits to be discarded for a given order of delta-sigma converter, and specified decimation factor are explained in detail. Also provided is a simulation result of a sixth-order 24-bit delta-

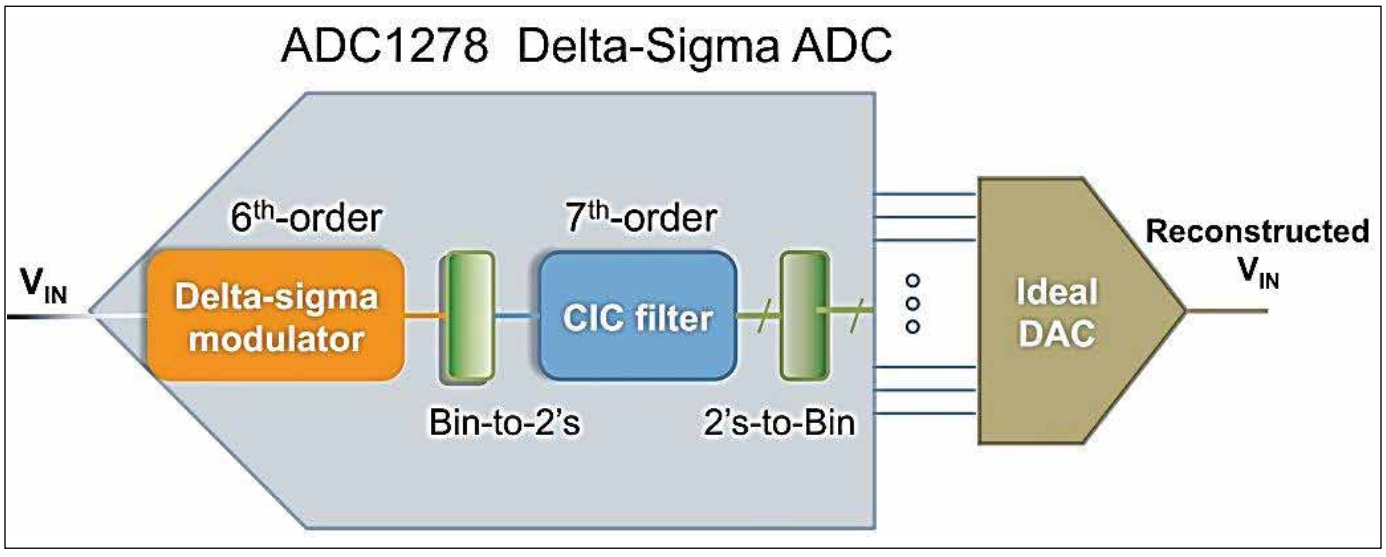

Figure 9 • A design using TI's ADC1278 24-bit ADC macromodel building blocks.

sigma ADC macromodel that depicts the reconstruction of an analog input signal for various clock frequencies and decimation rates.

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Arash Loloee is a Member of Texas Instruments' Group Technical Staff. As Senior IC Design Engineer, he has responsibilities ranging from designing transistor- to system-level projects. He received his Ph.D. in EE and MSEE from Southern Methodist University, and his B.S. in Physics from the University of North Texas. Arash has been a lecturer at the University of Texas at Dallas (2005 to 2011) where he taught various analog-related topics. He has three patents, with one pending. Arash can be reached at ti_arashloloee@list.ti.com.

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