RF Transistor Large Signal Load Stability (LSLS) Analysis Using EDA Tools

By John Pritiskutch

A method for analyzing RF device behavior during large signal operation into matched and mismatched loads, while simultaneously analyzing small signal input stability.

RF device stability can be very demanding when trying to mitigate a balance with all other aspects of a specific application. There are many device characteristics that can be separately analyzed with large and small signal EDA simulation methods. The results are then inferred on how they would interact. Eliminating this complexity requires a real world simulation tool. The age-old RF device curiosity—"if my RF device is operating in a large signal nonlinear mode into a matched or mismatched load, what does it look like everywhere else with respect to input stability?"—can be answered with a Large Signal Load Stability (LSLS) simulation tool. Agilent's Advanced Design System (ADS) will be used as the example EDA platform.

A traditional tool for stability information is S-parameter simulation using the Load Stability Circles. This means at which loads will the source become unstable. Generally, this information is used to predict large signal RF device stability, albeit small signal in nature. Another tool is the Large Signal S-parameter (LSSP) simulation which can also plot stability circles, albeit large signal in nature. These simulations describe a device with either a small or large signal excitation.

Simultaneous Analysis

To forego the usual large signal - small signal interaction discussion, it is advantageous to have an EDA tool that allows *simultaneous small and large signal analysis*. More specifically, a small signal input stability analysis while under large signal operation.

This can be accomplished by using an n-tone EDA source with frequency tones of various magnitudes, the harmonic balance controller mixing order set to zero and the proper equations written to select the interested tones.

An example Large Signal Load Stability simulation is presented. The generic LDMOS device model's 900 MHz source and load impedance has been previously determined and a second order low pass load matching circuit was chosen. The input stability will be analyzed from 10 MHz to 100 MHz, while 900 MHz large signal operation is subjected to 20:1 load mismatch at all phase angles. The LSLS instrument with generic LDMOS and load matching circuit is shown in Figure 1. The large and small signal input powers are 33 dBm and -100 dBm. The LSLS data display contains the load mismatch and phase angle shifts of the circuit and device loads, the delivered power into a matched and mismatched load and the input stability.

The load mismatch sweep is made to complete all phase angles at the large signal frequency. The mismatch is broadband while the phase angle variation is specific to the large signal frequency.

Figure 2 shows a 20:1 mismatch 360 degree phase angle shift at 900 MHz and its subsequent mismatch and angle shift at the small signal frequencies. The 100 MHz shift is shown, all lower frequency phase shifts are less and cannot be seen due to being overwritten by the sweep output.

Figure 3 shows the device's matched and mismatched load impedance and large signal delivered power.

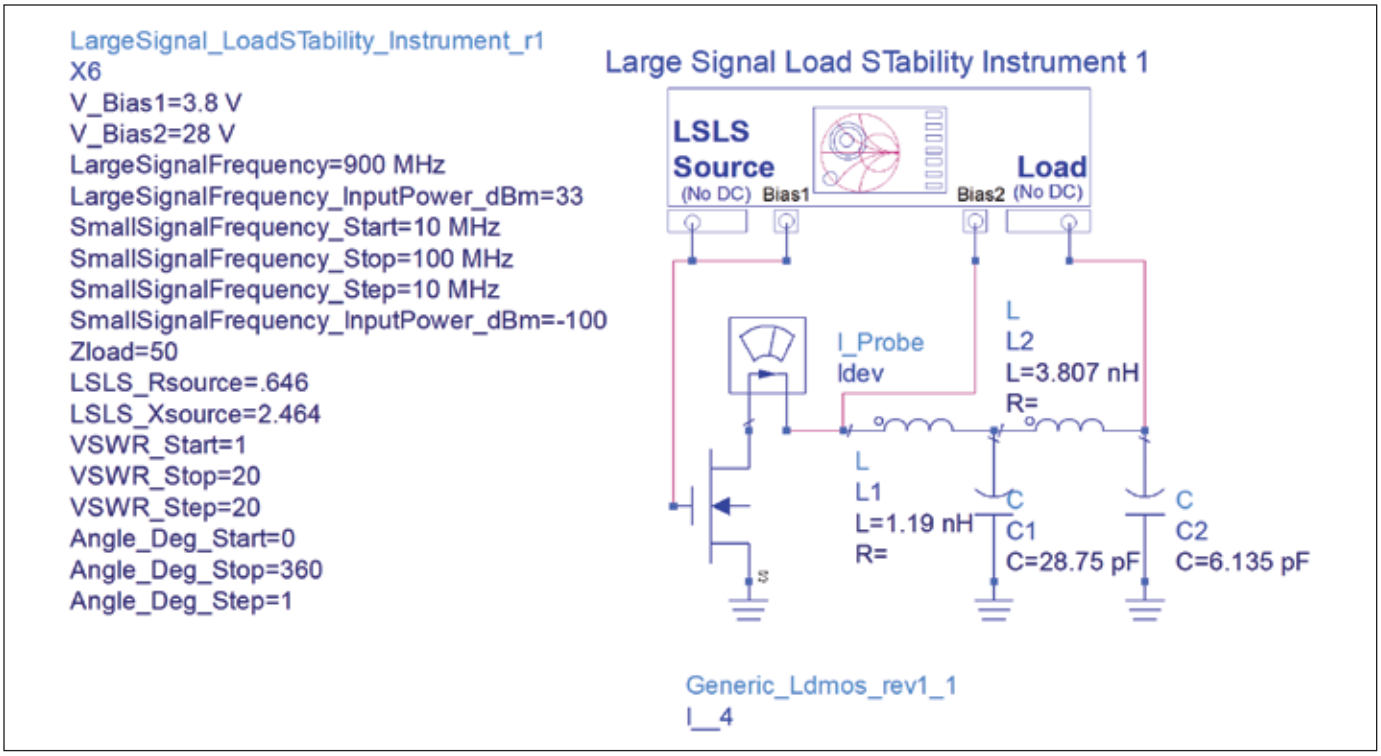

Figure 1 • The LSLS instrument with generic LDMOS and load matching circuit is shown.

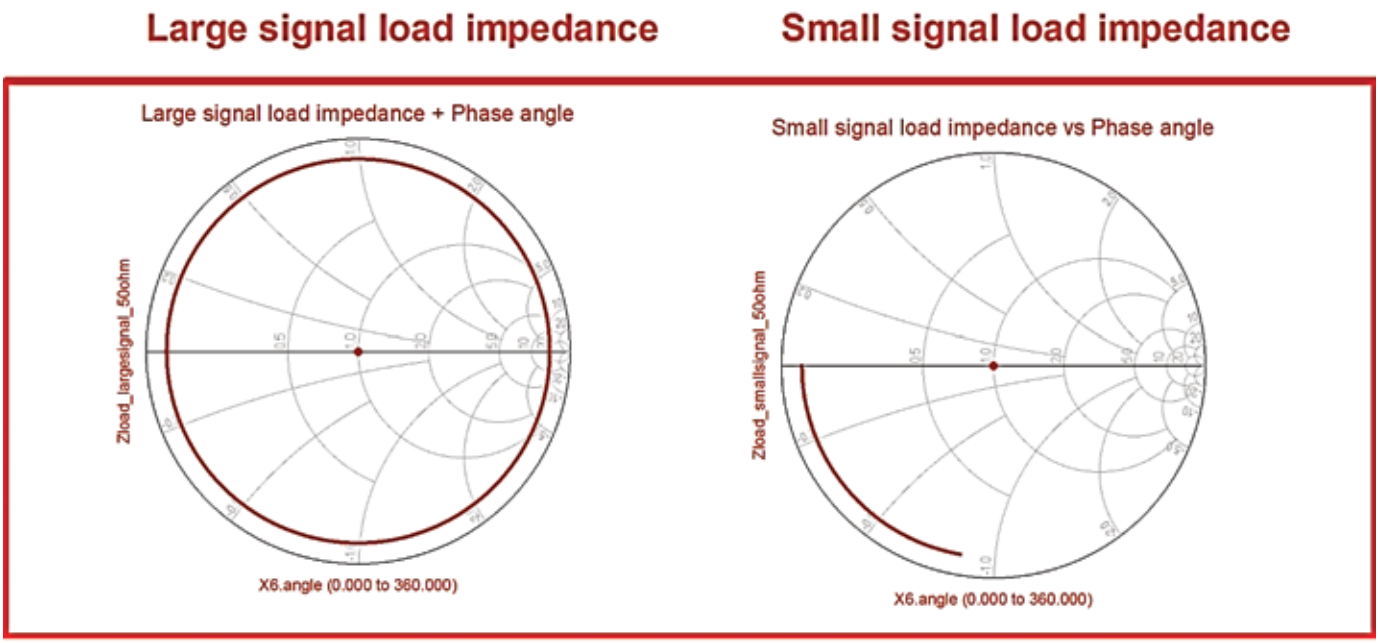

Figure 2 • A 20:1 mismatch 360 degree phase angle shift at 900 MHz and its subsequent mismatch and angle shift at the small signal frequencies.

Figure 4 plots the input stability in terms of magnitude (plotted as a Max value) and the input impedance. Magnitudes greater than 1 or impedance outside the 1:1 impedance chart indicate negative resistance (unstable).

The result of the LSLS simulation using the generic LDMOS model indicates stability concerns with the particular load matching circuit. Stabilization techniques can be added and analyzed for a particular application goal.

This paper presented a method to show how a simultaneous small and large signal analysis can be constructed with EDA components. The input stability is shown at

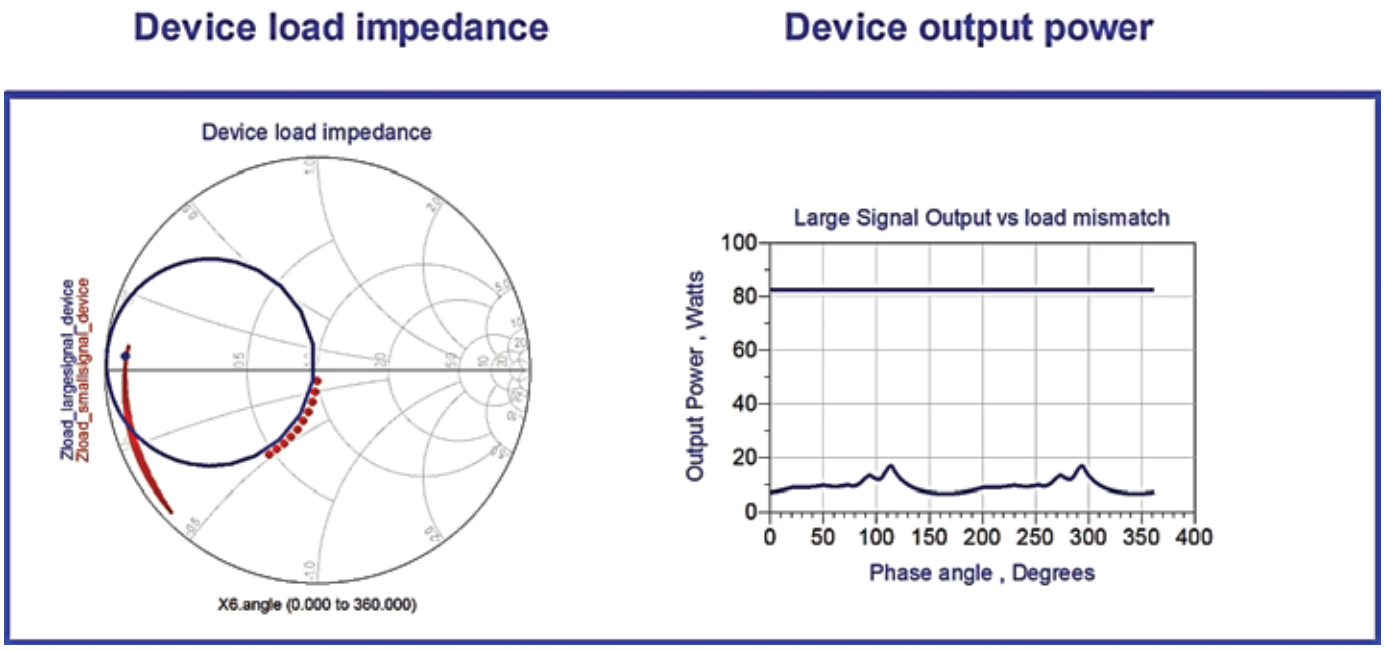

Figure 3 • The device's matched and mismatched load impedance and large signal delivered power.

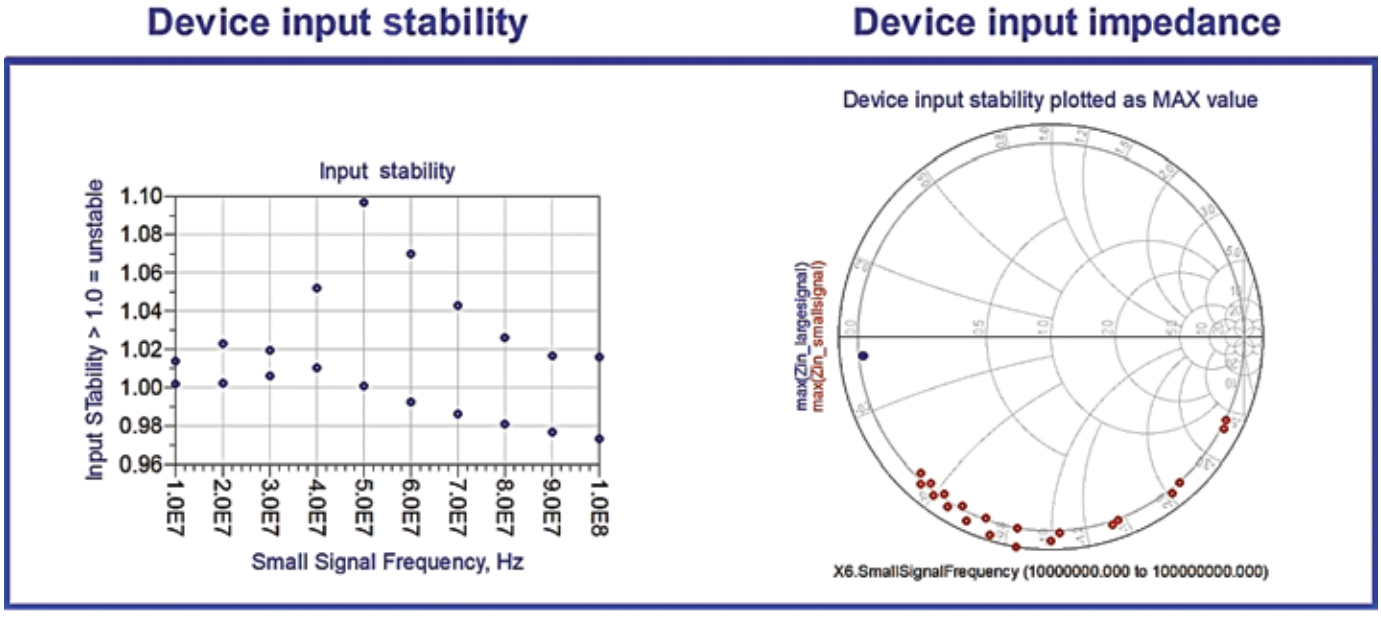

Figure 4 • This figure plots the input stability in terms of magnitude (plotted as a Max value) and the input impedance.

the device's exact large signal operation into a specific load matching network.

About the Author:

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