EMC Simulation of Consumer Electronic Devices

By Andreas Barchanski

Describing a workflow for the EMC simulation of a wireless router, using techniques that can be applied to a wide range of consumer electronic devices.

To ensure safe and reliable operation, all electronic devices must meet EMC standards. By including EMC compliant design at an early stage, additional costly design iterations can be avoided later on down the line. This article describes a workflow for the EMC simulation of a wireless router, using techniques that can be applied to a wide range of consumer electronic devices. A number of EMC considerations are shown and discussed, including board-level EMC analysis, the effect of the device's enclosure, cable entry susceptibility, and the use of segmentation to study how a component affects the larger system.

Introduction

The flow of currents within electronic devices generates electromagnetic fields. When multiple devices operate in a shared environment, these fields can couple between them, and this can affect their performance or even lead to failures.

To reduce the risk of electromagnetic compatibility (EMC) problems, regulatory limits restrict the emissions that devices can produce, and the design process must take these specifications into account. However, the effects that give rise to EMC problems, such as resonances, couplings and field leakage, are complicated and often hard to calculate, and so traditionally EMC engineering was associated with measurement.

This meant that EMC testing was carried out late in the design process, after a prototype had been constructed. Constructing a prototype represents a considerable investment in development, in terms of time, labor and capital, and troubleshooting EMC problems at this late stage can require considerable effort. In a complex electronic system, it was often prohibitively difficult to locate the source of an EMC problem, and instead all the engineer can do is fight the symptoms.

With simulation, the EMC properties of a design can be checked at any stage of the development cycle. In particular, the results of simulation can influence the design, allowing multiple possible configurations – for example, the alignment of a board or the position of a component – to be tested comparatively quickly and cheaply.

The example used in this article is a wireless router, kindly provided by Cisco. This router includes a number of components which can be analyzed for EMC reasons during the design process, and which require a variety of simulation methods for a complete analysis.

PCB Rule-Checking and Simulation

One simple and widely used approach for identifying possible EMC problems is to apply design rules when laying out PCBs. These rules are based on years' worth of experience of "best practice" gained by EMC experts working in the field, and are intended to prevent engineers from designing boards that radiate too much energy or introduce too much noise into the signals. A few examples of such rules are:

- Critical Net Near Edge of Reference Plane – A limit on how near signal lines can be to the edge of the board or reference plane. Lines close to the edge can generate larger radiated emissions and couple to other components.
- Critical Differential Net Length Matching and Spacing – This ensures that pairs of lines carrying differential-

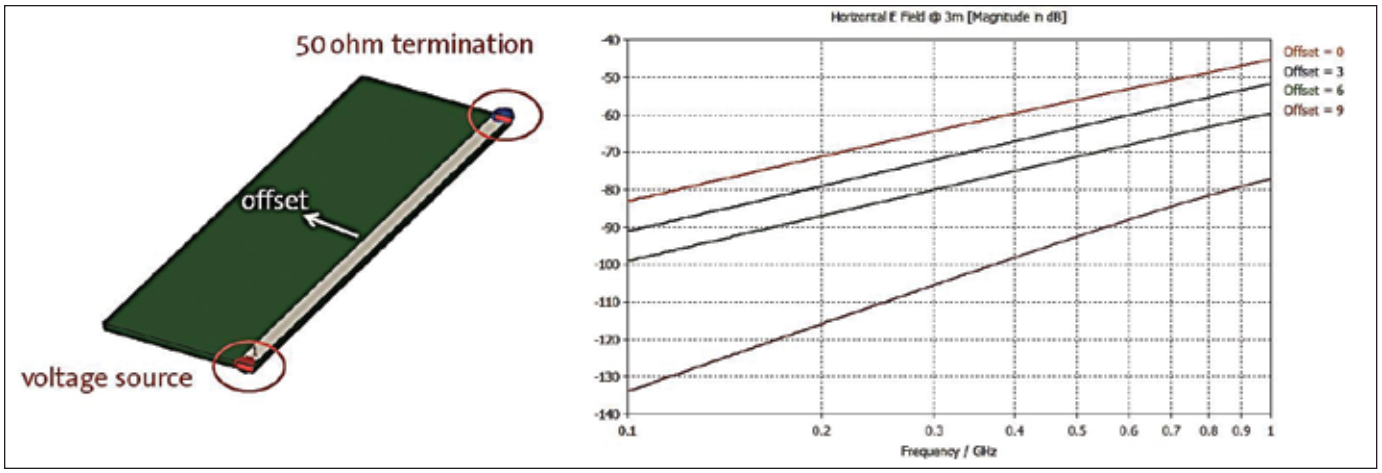

Figure 1 • Radiated fields around a microstrip.

mode signals have similar lengths. Too great a difference between the two causes common-mode noise, which leads to both EMC and signal integrity (SI) problems.

- Critical Net Near I/O Net – High-speed signals can couple into input and output nets, such as USB controller nets. As these nets leave the PCB and often run along long cables, they pose a significant risk of re-radiation.

To demonstrate the importance of careful net placement, a 5 cm long microstrip line was modeled on the edge of an FR4 substrate with a relative permittivity of 4.2, as shown in Figure 1. The line was terminated on one side by a 50 ohm resistor and fed by a broadband 1 volt source on the other side. The position of the line was parameterized: an offset of 0 mm corresponds to the line being located at the edge of the substrate, while at an offset of 9 mm the line is located in the center. A simulation was run using the time domain finite integration technique (FIT) solver in CST MICROWAVE STUDIO®, with horizontal electric field at a distance of 3 meter being recorded using a field probe. From the plot on the right hand side, we can clearly see how the radiated field depends on the frequency and the position of the microstrip. Moving the line from the center to the edge of the substrate increased the radiated electric field by more than 30 dB; potentially a huge increase in emissions.

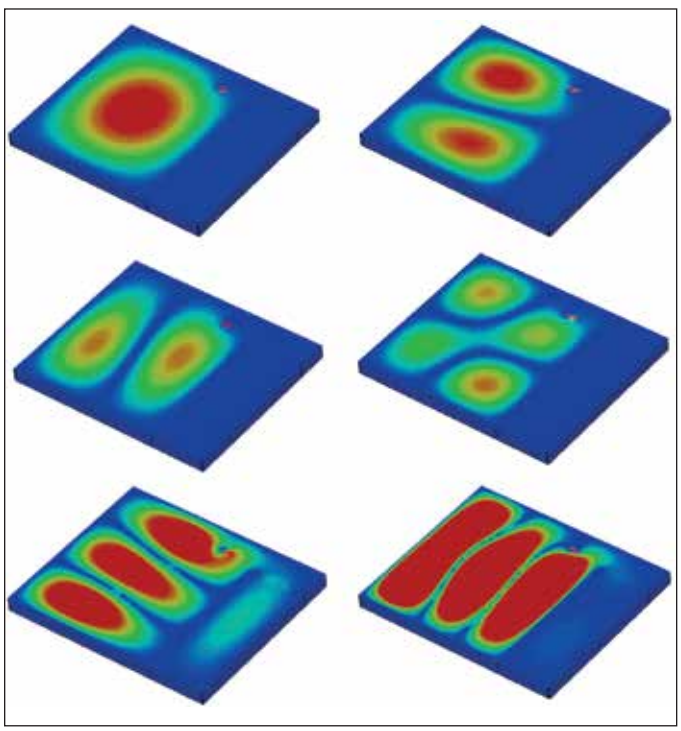

Figure 2 • Resonances for a source located in the corner of the enclosure.

Once a potential problem has been identified, the engineer needs to decide whether it is severe enough to warrant a redesign of the board. Full-wave simulation is a useful tool here – the design can be imported into a 3D electromagnetic simulation to examine the fields generated when in use. If the position of a component or trace can be parameterized, a parameter sweep can be used to investigate whether the benefits of, for example, moving a trace away from the edge of the board justify the extra design work.

Designing a complex multi-layer high-speed board to fulfill all of the design rules rigorously would be very difficult, as well as being poor use of time and effort. For many nets, rule violations will not always lead to EMC problems, and different types of device need different rule sets. Power electronics, for example, will not have the same EMC problems that a high-frequency RF device has.

The smartest way to apply design rules is to designate certain parts of the board, such as I/O nets, high-speed data lines and clock signals, as being especially critical. Rule-checking software such as CST

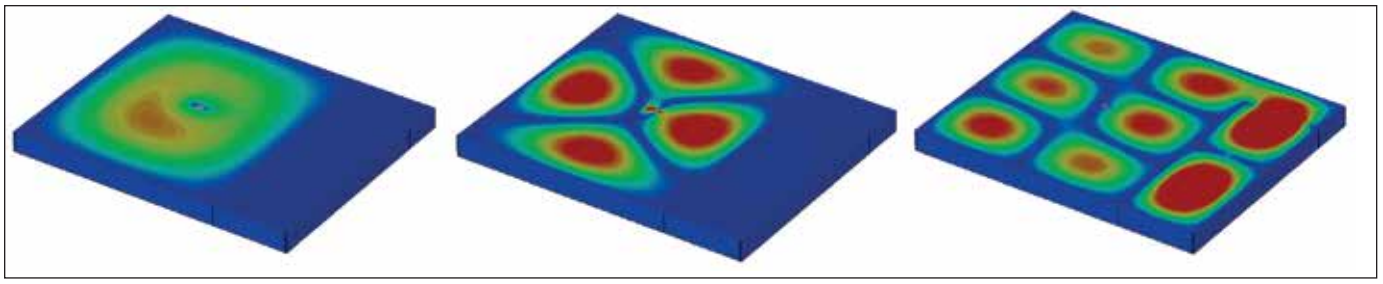

Figure 3 • Resonances for a source located in the center.

BOARDCHECK™ can then examine these areas against a set of design rules to highlight all violations, without the risk of human error.

In a real device, however, the PCBs do not simply sit in isolation. The environment around the board, such as the other components, cables and the enclosure itself, can give rise to further EMC problems.

For instance, many devices work in the range of hundreds of megahertz up to gigahertz. At these frequencies, the wavelength of the EM fields is comparable to the size of cables and the enclosure, and when fields couple to these they can produce resonances.

Because of their nature, resonances are slow to simulate with time domain methods – a high-Q resonance will keep ringing for a long time. Frequency domain simulation methods are a better fit for these sorts of problems. As a first step in testing the EMC properties of the router's housing, a very simple model is constructed, driven by a discrete port.

A broadband frequency simulation shows multiple resonant modes (Figure 2), each of which might contribute to the emissions of the device. If there is a noisy component which is radiating at a resonant frequency, it is often worth moving it to somewhere else on the board. As shown in Figure 3, moving the source from the corner of the enclosure to the edge produces very different resonances.

Once we have an idea about how the enclosure behaves, we can then model the device in greater detail. Due to their size and construction, heat-sinks are often a major source of EMC problems on PCBs – they are usually mounted over high-speed signal lines, and this means that currents couple into them and produce fields that are re-radiated.

Instead of using just a simple voltage source, we can use a realistic model of the heat-sink (Figure 4) and investigate what fields this produces. We can simply place the heat-sink model in the full router model, but then this mesh will extend throughout the simulation domain, slowing down calculation time.

For detailed models – for example, an integrated circuit or a multilayer PCB – it is more efficient to model the component separately using a hybrid approach with two different solver technologies. The detailed model is simulated using the time domain FIT method, suitable for components, and a nearfield monitor captures the field around it. This source is then imported into the router model (Figure 5), and used to drive a simulation

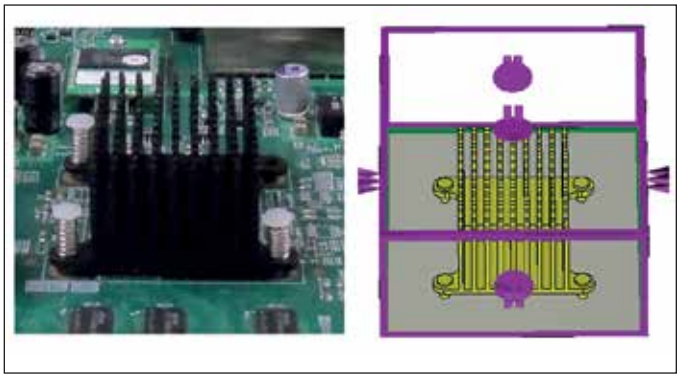

Figure 4 • The heat-sink and a 3D simulation model.

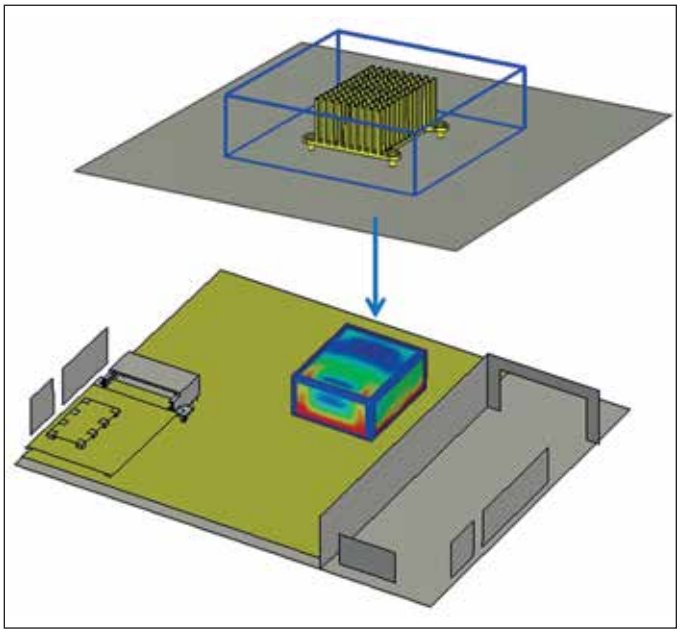

Figure 5 • A nearfield source replacing a detailed model.

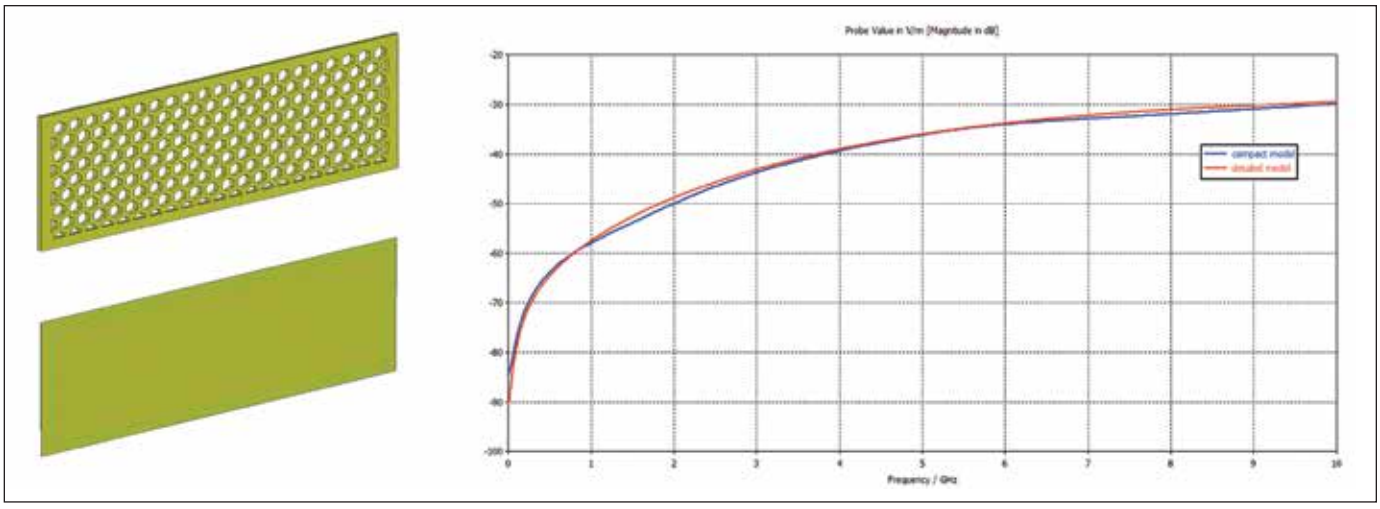

Figure 6 • Detailed vent (top), compact vent model (bottom), and a comparison of the two.

with the transmission line matrix (TLM) solver, which is well suited to enclosures.

With a detailed model, the engineer can try mitigation strategies such as adding grounding pins or changing the number of fins on the heat-sink. The dimensions of the model can even be parameterized; the System Assembly and Modeling (SAM) approach of CST STUDIO SUITE® can carry out a parameter sweep and cascade the changing nearfield into the full simulation – in this case, to calculate the interaction between the heat-sink and the radio frequency components in the bottom-left hand corner of the router. With SAM, a series of simulations can be carried out automatically simply by defining tasks in CST DESIGN STUDIO™, using monitors and ports to transfer data between different parts of the simulation.

Designing the Enclosure

Fields can leak through seams, vents and panels, and so it is very important to consider these in the calculation. However, the details of such features are usually very small, which makes them time-consuming to simulate. The simulation can be sped up by applying compact models. Compact models in the TLM solver replace these fine structures with an efficient equivalent representation which nevertheless interacts with fields the same way.

Figure 6 compares the detailed and compact model of a hexagonal vent, with hole side-length 1.74 mm and a depth of 1 mm. The compact model exhibits the same behavior as the detailed model; the field strength results are very similar across the entire frequency range. Not only do the compact models solve faster (for the example in Figure 6, simulation time was halved by compact

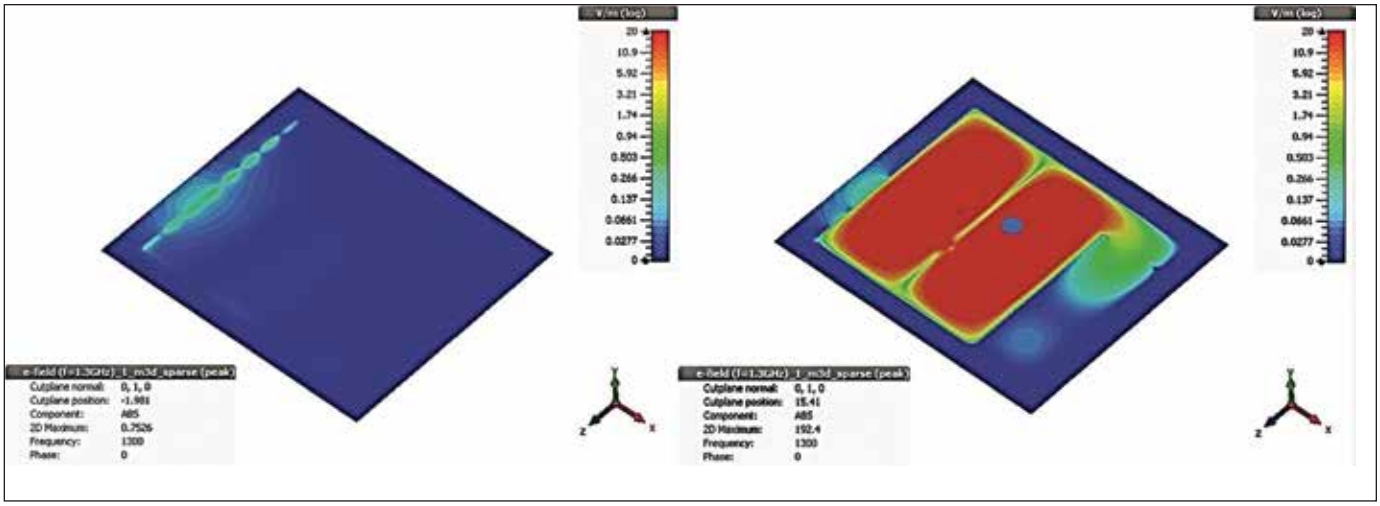

Figure 7 • Seam leakage (left) and vent leakage (right) at 1.3 GHz.

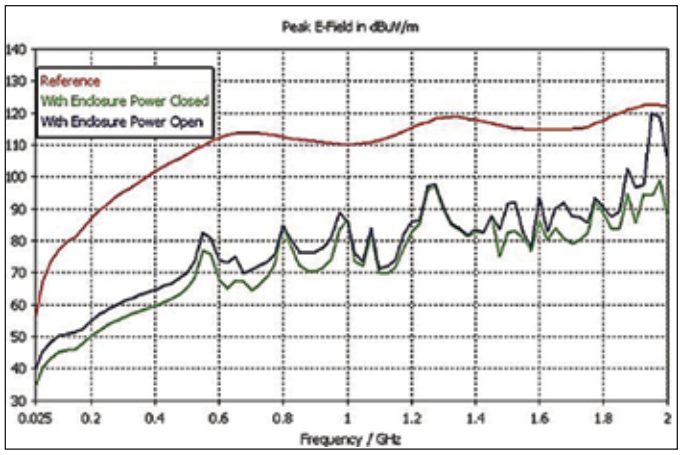

Figure 8 • Broadband results for the router, with the unenclosed PCB as a reference.

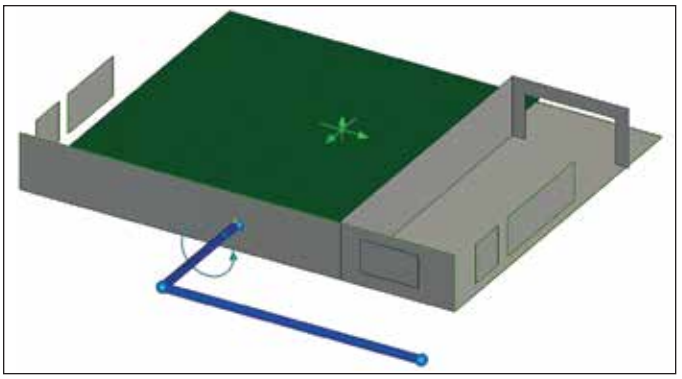

Figure 9 • A simplified model of the router, showing the cable (blue) entering the device.

models), they also require a less detailed mesh, which leads to even larger time-savings for electrically large models.

The simulation results for the complete device are shown in Figure 7 and Figure 8. Compact models were used for the cooling vents on the left and right sides of the device, and for the seams where panels of the case meet.

At 1.3 GHz, there is some leakage of fields through the enclosure – however, this is still several orders of magnitude lower than the fields seen around the unenclosed PCB. However, at around 1.95 GHz, there is a sharp rise in the E-field around the router, and the radiated emissions are almost as high as those if no enclosure at all was present. This corresponds to leakage through the power socket aperture – without this hole, there is a 20 dBuV/m difference in emissions.

Susceptibility

As well as keeping emissions low, engineers also have to ensure that external fields do not interfere with the device. One common cause of interference problems in devices is cabling. Long cables effectively act as antennas to external fields, channeling waves into the device.

However, traditional 3D simulation methods struggle with modeling cables, which can be several meters long but only a few millimeters wide, with an often complex internal structure. For these sorts of cables and cable harnesses, a hybrid cable simulation can be very efficient.

Cable simulation can be unidirectional or bidirectional, depending on which couplings are taken into account. In a unidirectional simulation, the solver calculates either the fields generated by currents flowing within the cable, or the currents induced in the cable by external fields – this is effectively the same approach used earlier to model the heat-sink separately from the PCB.

In a bidirectional simulation, however, the cable is simulated alongside the 3D model. This means that both effects are taken into account, so that, for example, fields can radiate from the cable, induce currents within the device enclosure, and then the re-radiated fields interact once more with the cable. Bidirectional simulation is not offered by all cable simulation tools, but it produces a more physically accurate simulation.

The wireless router in question includes a USB port, and we want to study how a USB cable could couple energy into the device. USB cables are hybrid cables, with one 5 V power wire, one ground wire and a twisted-pair set of signal wires. Although this would be difficult to build as a 3D model, we produce a hybrid model by defining the cable route and cross-section in CST CABLE STUDIO®. All the relevant properties of the cable can be adjusted, including the twist-rate of the twisted pair, the thickness and permittivity of the insulators and the material and design used for the shielding. In this case, we're using braided shielding, but a number of frequency-dependent shield models are available, and arbitrary shields can be simulated by importing transfer impedance measurements.

We define an USB cable entering the chassis, consisting of a long path of shielded cable outside of the enclosure and a short path of unshielded cable inside, illustrated in Figure 9. We then carry out two bidirectional simulations, varying the connection between the cable shield and the chassis. In one, the path between the shield and the chassis has a low resistance, representing a good connection, while in the other, there is a very high resistance between the two. A broadband plane wave is used to excite the structure, to model the

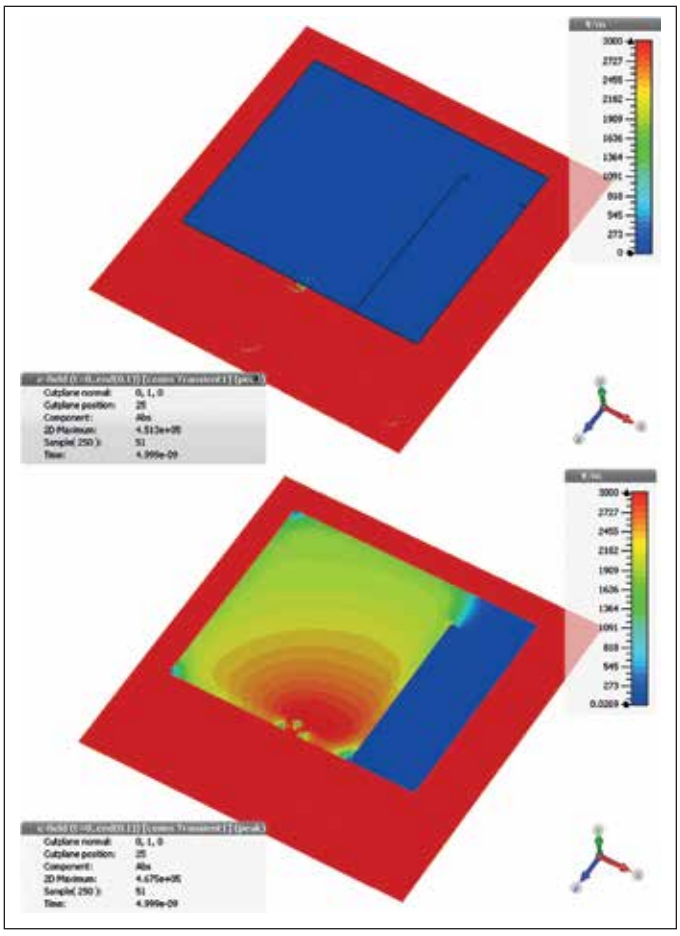

Figure 10 • E-fields within the device for (top) the connected chassis and (bottom) the disconnected chassis.

irradiation of the structure by a powerful external electromagnetic pulse (EMP). Again, probes are used to monitor the fields inside the enclosure.

As shown in Figure 10 and Figure 11, the connection between the shield and the chassis has a major effect on the susceptibility of the device to external radiation. With the cable shield well connected, the peak E-field measured was around 15 V/m. However, when the screen was disconnected, E-fields reached almost 3000 V/m.

From these simulations, we can conclude that the connection of the cable screen to the chassis is critical from a susceptibility point of view. During the design phase, care needs to be taken to make sure that this connection is well defined, and it is also important that this connection should not deteriorate during the lifetime of the device, as the reduced connectivity for example caused by aging effects can drastically increase the susceptibility of the device.

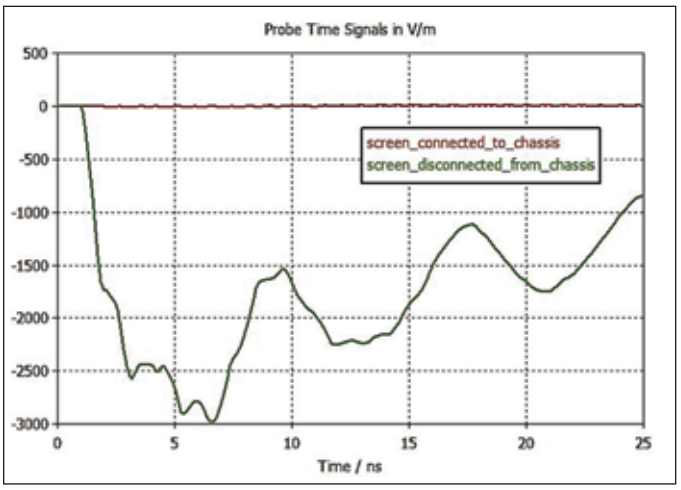

Figure 11 • E-field values in the center of the device.

Conclusion

With simulation, the engineer can investigate a wide range of EMC characteristics of a design long before going into the lab for measurement. From rule-checking at the early stages of layout, to full system simulation alongside traditional prototypes, simulation can be used at any stage of the product design workflow.

Components can be tested not just in isolation, but as part of a complex system – with SAM, different simulation techniques can be used on different parts of the system as appropriate. Additional specialized hybrid methods for modeling PCBs, cables and fine structures allow these often-complicated elements to be simulated in conjunction with the rest of the device.

This article has presented a simulation workflow for analyzing the EMC of a wireless router, and shown how, when problems are identified, simulation can also be used to help find a solution: alternative designs to be checked without the expense of constructing multiple prototypes.

About the Author:

Andreas Barchanski is the EMC Market Development Manager at CST (www.cst.com). He holds an M.Sc. degree in Physics and a PhD in Numerical Electromagnetics from the Technical University Darmstadt. He joined CST as an Application Engineer in 2007. Besides EMC, his main interest lies in the simulation of various electronic systems ranging from high-speed digital to power electronics.