Using Analyst™ to Quickly and Accurately Optimize a Chip-Module-Board Transition

By Dr. John Dunn

Optimizing the transition from a board-to-module-to-chip signal path.

3D electromagnetic (EM) simulators are commonly used to help design board-to-chip transitions. AWR now makes life easier for circuit designers with the introduction of Analyst™, the industry's first full featured, 3D EM finite element method (FEM) simulator integrated within the circuit design environment, without the need to launch a third party drawing and simulation tool.

The key advantage of Analyst over other available 3D simulators is its tight integration within Microwave Office® (MWO), AWR's circuit design and simulation environment. This paper highlights the unique features of Analyst by demonstrating the optimization of the transition from a board-to-module-to-chip signal path. The example shows how the ability to access Analyst from within in the MWO environment saves designers time and provides ready access to powerful layout and simulation tools that are not available in typical circuit design tools.

Analyst simplifies layout setup and drawing by offering preconfigured 3D parametric cells (Pcells) for the bond wires and ball grid arrays (BGAs). Hierarchy is supported in the EM layout, enabling easier reuse of designs. Tuning, optimization, and sensitivity and yield analysis can be quickly implemented through the use of parameterized layout, without having to leave the MWO environment. Since Analyst is optimized for RF designers with automatic simulation settings for typical technologies, users usually do not need to go into the simulation settings of the software. Designers can now concentrate on their design, easily using 3D EM simulation when needed, without having to spend time learning a complicated third product tool. Indeed, if they already use AXIEM®, AWR's planar EM simulation tool, they will find Analyst looks almost the same. The learning curve for making effective designs is therefore very short.

A Chip-Module-Board Transition

Figure 1 shows the board, module, and periphery of the chip being investigated. The signal goes from Port 1 on a trace on a PC board onto a module by means of a BGA, along a trace on top of the module, and over to Port 2 on the chip by means of a bond wire. The design goal is to have a return loss of less than -20 dB over the frequency range of interest, 10 to 20 GHz.

The simulation results for the layout using Analyst for the return loss of the initial design are shown in Figure 2. Clearly, the design goal of less than -20 dB is not being met.

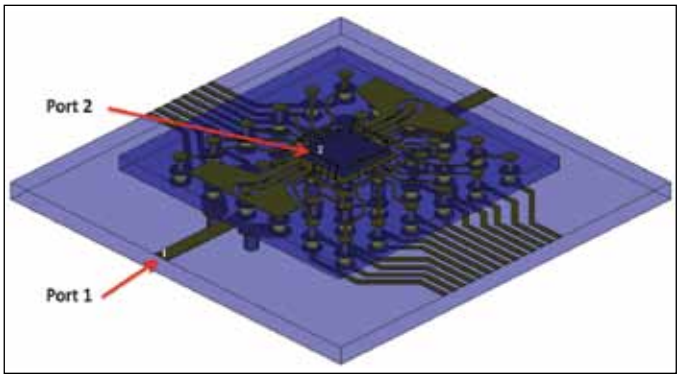


Figure 1 • The performance of the transition from Port 1 on the board to Port 2 on the chip is under investigation. The signal goes up the BGA ball, onto the module, and then onto the chip by means of a bond wire.

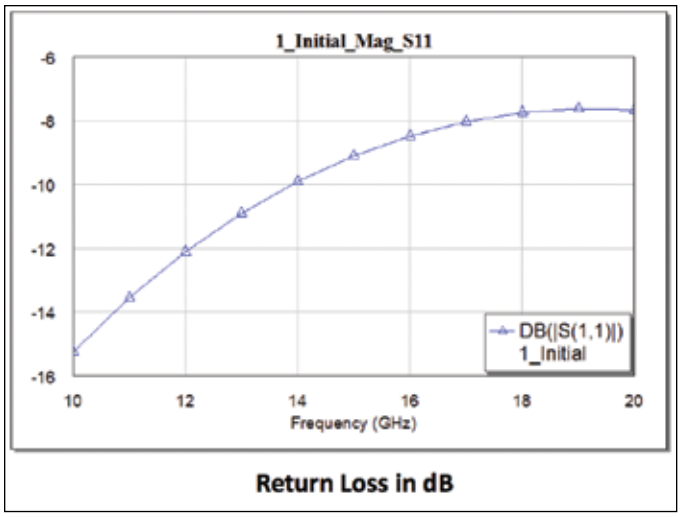


Figure 2 • The return loss in dB is shown from 10 to 20 GHz. The design goal of less than -20 dB is clearly not being met.

The problem can be fixed using a three-stage strategy. First, the specific area(s) causing the poor performance need to be identified. Second, the designer needs to understand why that area of the layout is electrically behaving the way it is. For example, there could be extra inductance or capacitance in that section of the layout. Third, the problem needs to be corrected by modifying the layout.

Analyst has a number of features that designers can take advantage of as the design is modified. Analyst has the ability to simulate only portions of the layout, thereby reducing problem size and increasing simulation flexibility. Simulation ports can be added where needed so that the problem area of the layout can be probed for better understanding. Because Analyst is part of the Microwave Office environment, these ports can easily be added where the designer suspects extra capacitance is needed. The Analyst results are then inserted into a schematic, capacitors are attached to the ports, and their values tuned and optimized. Finally, the layout is tweaked to give the desired extra capacitance or inductance. Again, only the portion of the layout of interest need be simulated. Analyst is designed to minimize the amount of setup time required for a simulation.

Let us now look at this design process in more detail. Starting with the launch area, the designer is focused on the return loss for Port 1. Only the part of the circuit close to the signal line running from Port 1 to Port 2 is relevant. Figure 3 shows the area of interest, in which the designer has drawn a new simulation boundary. The top half of the diagram shows the simulation boundary used. The bottom half of the figure shows the 3D view after initial meshing has occurred: the mesh in the air region above the board is not shown in the interests of clarity. (Note: viewing the mesh is not required of Analyst but is shown here for users' benefit given prior familiarity with 3D FEM EM point tools).

The first port appears on the edge of the boundary. Analyst treats this as a wave port, standard to all FEM simulators. Traditionally, the designer is required to go through the time-consuming step of setting up this type of port manually in a 3D EM tool In addition, the designer must to set up the number of modes analyzed and define their port impedance definitions. Because these concepts are not very familiar to the mainstream circuit designer, Analyst has been preconfigured for reasonable settings for the port for typical planar layouts, enabling users to focus on their design instead of worrying about tweaking the settings. In situations where the preconfigured settings are not optimal, the default settings can be changed.

The bond wire is attached to a pad on the chip. A second port is attached to the pad. Notice that it is interior to the boundary, unlike Port 1, and so Analyst automatically treats it as an internal port. In this type of port, a voltage is excited from the port to the port's ground. (The ground is specified with a mathematical "strap" from the

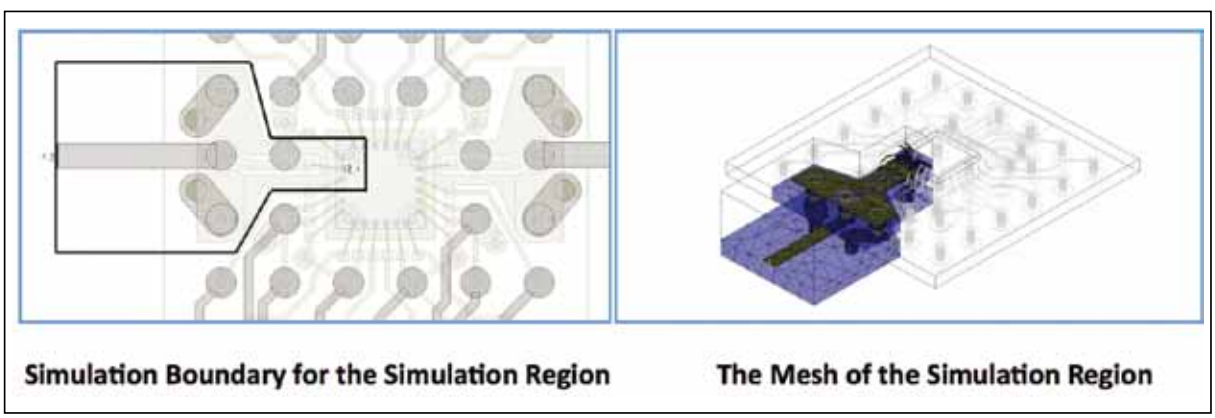


Figure 3 • A simulation boundary is used to reduce the size of the problem. Note that the mesh for the air region is not shown in the 3D view.

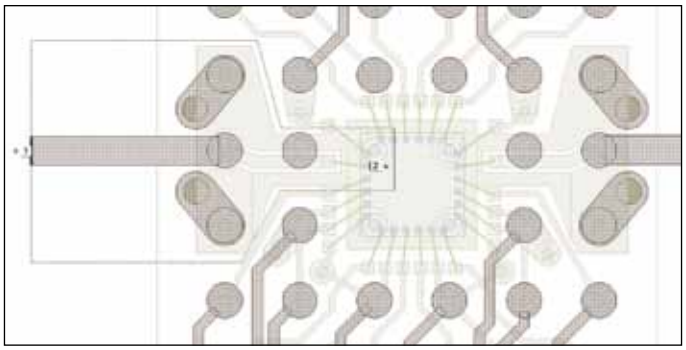


Figure 4 • A bond wire is drawn using a Pcell. The Pcell is shown as a symbol in a schematic, and has a 3D layout. No manual drawing is required.

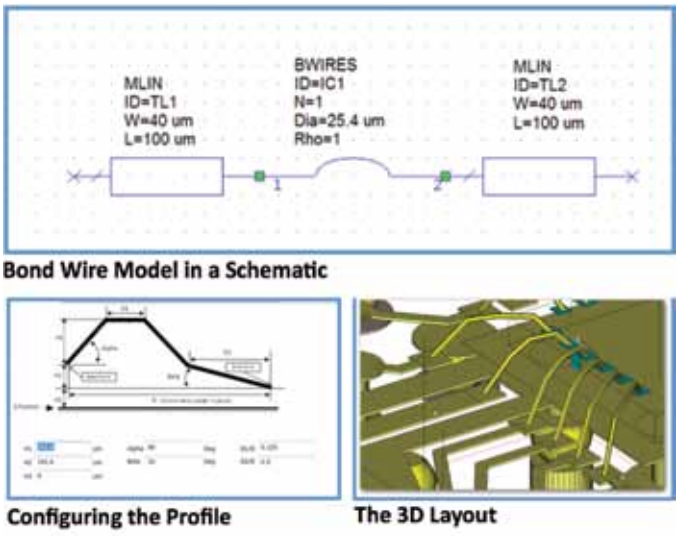


Figure 5 • The layout was constructed using hierarchy.

port to its ground. The strap can be set by the designer to go to the nearest ground plane above or below the port.) Later on, variations on this port will be shown, where the designer uses differential ports in which three ports act as a group to excite a coplanar circuit. The key point here is that it is not necessary for the designer to manually configure the port settings, a common source of error in EM simulation.

Layout of the Circuit and Hierarchy

A number of interesting features in the MWO environment were used to aid in drawing the circuit. First, the 3D bond wires and BGA balls were never drawn by hand. Rather, preconfigured Pcells were used. A Pcell is a model element that is controlled by parameters. For example, Figure 4 shows the Pcell used for the bond wires. The cell is placed in a schematic used for EM simulation. The figure shows it between two transmission lines.

It is easy to configure the profile of the bond wire using the Pcell properties menu, and place it in the EM layout. The 3D shape is automatically drawn, another feature highlighting how Analyst is optimized for ease-of-use for RF circuit design. Pcells are available for bond wires, tapered vias, bond straps, and BGA balls, to list the most commonly used elements.

The layout was drawn using hierarchy. There are three distinct levels of layout, as shown in Figure 5.

The chip level layout shows the chip pad locations. The module level layout uses the chip layout as a sub-cell. The final top-level layout uses the lower two levels of layout. There are a number of advantages to this approach. First, EM simulations can be carried out on various levels of the layout as the design progresses. For example, if a spiral inductor is simulated on its own, then the cells can be joined at a higher level to easily look at more than one spiral on the chip without any drawing, redrawing, or manual setup manipulations. Hierarchy makes it easy to organize the layout, and carry out smaller EM simulations as the design is being developed. Second, remember that there is the option of associating a layout with a schematic. With hierarchy, designers now have the flexibility of sub-circuits in schematics.

Improving the Transition

Next, the designer needs to figure out what the dominant source of reflection in the launch was. The next phase of the study is to isolate this source by systematically breaking the simulation region down further by adjusting the simulation boundary. The problem naturally breaks out into three regions: the line on the board up to the BGA balls; the transition from the board through the ball and vias to the signal line on top of the module; and transition from the module to the chip with a bond wire. Figure 6 shows the three regions that were used.

The designer was careful when specifying the boundary regions to make sure the enclosed structures were reasonably well isolated from the surrounding environment. An example of the issue is shown in Figure 7, which

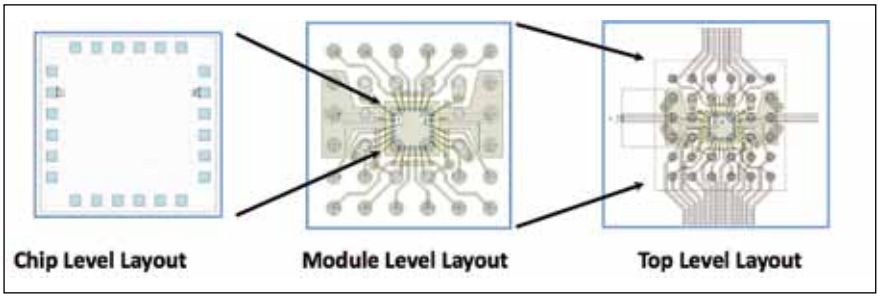


Figure 6 • The problem has been broken up into three different regions to determine the biggest contributors to the issue of reflection in the launch.

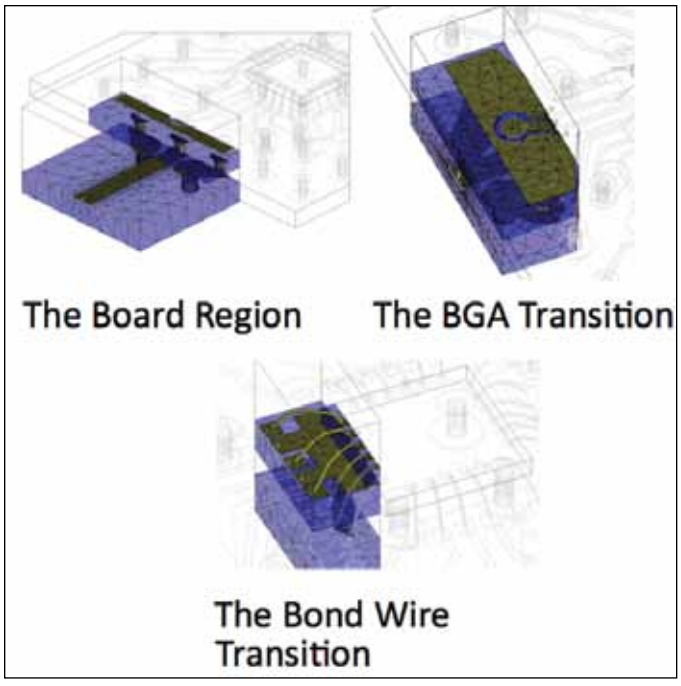


Figure 7. Detail of the second section. Notice the boundary is five-sided with different types of ports being used where needed.

provides the detailed layout for the BGA transition simulation.

The boundary was constructed with five sides in order to avoid coupling to other sections of the circuit. It depends on the technology being used, but typically a few substrate heights of distance are adequate for this type of problem. Analyst automatically sets the boundary to be an approximate open, where an impedance boundary condition mimics a perfect absorber to first approximation. Normally, this is the natural boundary condition to use, since the goal is to isolate the simulation region from other parts of the circuit. It is possible to override the default setting, but care is needed when choosing the boundary condition. For example, if a conducting boundary is chosen, it could actually short objects together in unintended ways.

The transition in Figure 7 also illustrates another interesting feature of Analyst. The location and type of ports used can be user-modified depending upon the circumstances. In Figure 7, Port 2 is a differential type of port. The current goes into the positive part of Port 2, and comes back on the neighboring ground returns, the ports of which are labeled with -2. The designer does need to make sure the ground for the ports is the same as the ground for the real layout. For example, in Figure 7 the differential port's grounds are the same as that of the module, and the return ground current is therefore the same as in real layout. The designer discovered that the second and third sections of Figure 6 needed the most improvement. The next step was to determine the specific causes of the poor performance. Extra ports were placed into the Analyst, and, once simulated, the results could then be placed into a schematic and the ports used to attach circuit elements. In this case, capacitors were added. This process is particularly easy in Microwave Office, because of the tight integration between the various parts of the software. The capacitor values can be tuned and optimized. To illustrate this procedure, Figure 8 shows that the designer added two more ports to Section 3 of the layout.

Ports 3 and 4 were inserted in the two most obvious trouble areas, near the bond wire and near the ball transition. Note that Port 4 is a differential port, which is the natural type of port to use in this situation, as it mimics the actual current flow in the real circuit. The current flows out of Port 4 and returns on the two ports labeled -4. The return current is coming back on the local ground of the port. The capacitor will be placed in the schematic from Port 4 to -4. Thus, the current return and local ground are all in agreement with the real layout. Port 3 is again a differential port, with the -3 part of the port attached to the local ground of the module.

The bottom half of Figure 8 shows the two capacitances added across Ports 3 and 4 in the schematic. Note that the capacitors are attached to ground symbols, which in this case means the local ground of the port, i.e., the negative port. The designer was surprised to find that the problem actually improved with negative capacitance at Port 4 near the BGA balls, i.e., inductance was required. Port 3, which is next to the bond wire, needed a positive capacitance.

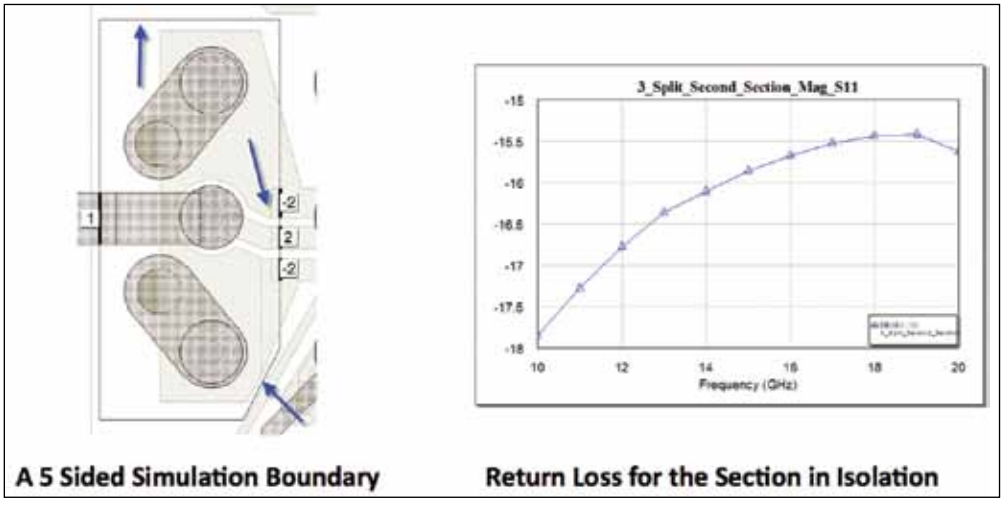
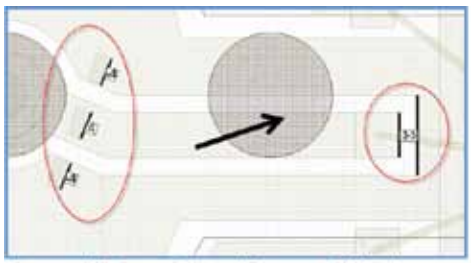
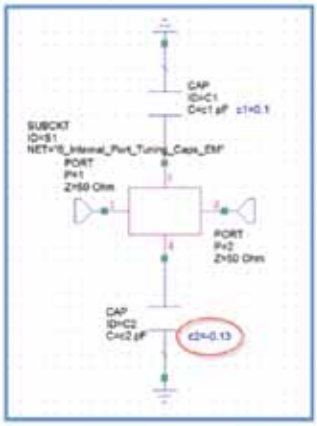


Figure 8 • Internal ports are added so that capacitance can be added and tuned on a schematic.

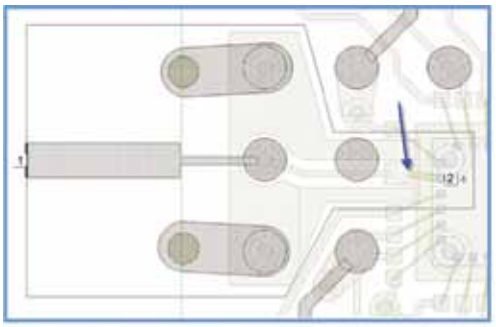


Internal Ports 3 and 4 are Added

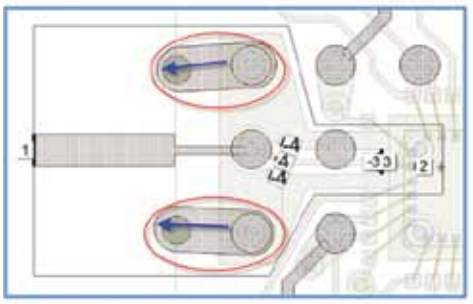


Capacitance is added in the schematic

Figure 9 • The bond wire region is modified by doubling the bond wires, and reducing the gap from the pad to the side grounds. The ground vias on the board are moved away from the ground balls for increased inductance.



Bond wire doubled and pad gap to ground decreased



Ground Vias on Board Moved Out

Figure 10 • The whole layout is simulated. The return loss meets the specification of being less than -20 dB over the desired frequency range.

To physically realize the extra capacitance near the bond wire, a variety of techniques were tried, including doubling the bond wires to reduce their inductance and narrowing the gaps between the line and the side grounds in the module. The extra inductance near the BGA balls was accomplished by adding extra loop length to the ground return on the board. The final solution is shown in Figure 9.

The ground vias on the board were moved away from the ground balls for increased inductance. The top diagram in the figure shows the bond wire has been doubled and shortened to reduce inductance. The gap between the bond wire pad and side grounds has been decreased to increase capacitance. The bottom figure shows the ground vias on the board being moved away from the ground balls to increase the loop inductance to compensate for the ball capacitance. The line on the module near the ball was also narrowed to increase inductance.

Finally, the entire structure was simulated for verification, as shown in Figure 10. The mesh is not shown in the air region for visual clarity. The return loss meets the desired specification, being less than -20dB over the frequency range of interest.

Conclusion

Within this design example, AWR's Analyst finite element 3D EM simulator was used to optimize the return loss for a board-to-module-to-chip transition. The novel features of Analyst were leveraged to speed up the study. Portions of the layout were simulated by redefining the simulation boundary and ports, without ever needing to manually redraw the structure. Pcells for the layout of the bond wires and BGA balls were used, so that these structures did not need to be manually drawn either. By adding extra internal ports, capacitance could be added to the parts of the transition quickly, and then the values could be tuned and optimized to determine where changes were needed. The preconfigured circuit simulation features in Analyst significantly reduced development time in this example: ports were automatically configured for optimal settings, 3D shapes were already drawn with Pcells, hierarchy of layout could be used, and simulation regions could easily be changed.

About the Author:

John Dunn is AWR Corp.'s electromagnetic technologist and is also in charge of training and university program development. His area of expertise is electromagnetic theory, simulation, and modeling. Dr. Dunn's past experience includes both the worlds of industry and academia. Prior to joining AWR, he served for four years as head of the interconnect modeling group at Tektronix, Beaverton, OR. Before entering the engineering industry, Dr. Dunn was a professor of electrical engineering at the University of Colorado, Boulder from 1986 to 2001, where he lead a research group in the areas of electromagnetic simulation and modeling. Dr. Dunn received his Ph.D. and M.S. degrees in applied physics from Harvard University, Cambridge, MA, and his B.A. in physics from Carleton College, Northfield, MN. He is a senior member of IEEE and has authored papers and presented at numerous conferences and symposia throughout the world.

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