# MMIC Frequency Doublers

By John E. Penn

Frequency multipliers can be useful for generating higher frequency sources from an existing lower frequency source.

**Abstract**

Several frequency doublers were designed using a 0.13 um GaAs Pseudomorphic High Electron Mobility Transistor (PHEMT) process from TriQuint Semiconductor. The design and fabrication of these circuits was performed as part of the Fall 2011 Johns Hopkins University Monolithic Microwave Integrated Circuit (MMIC) Design Course, taught by the author. The design approach is applicable to frequency multiplier MMICs that could be used for a variety of RF and Microwave systems.

Frequency multipliers can be useful for generating higher frequency sources from an existing lower frequency source. It can be simpler to take an existing Microwave communications system operating at one band and use multipliers to quickly up-convert the system for higher frequency operation. Whether mixing for up or down conversion, or directly up converting, a multiplier is one option for increasing the transmission or reception frequency.

Harmonics will be of concern with multipliers, so two of the three designs use a quarter wave stub to "short" out the fundamental input frequency, while optimizing the output load for the second harmonic. This approach could also be used for a harmonic tripler. Following is a discussion of the design and measured performance of these frequency doublers, a 10 GHz doubler, and an 8 GHz and 16 GHz doubler with harmonic stubs.

## Simple Frequency Doubler at 10 GHz

The first doubler design for 10 GHz to 20 GHz operation was quickly assembled using portions of other test circuits on the JHU 2011 MMIC Design Course quarter tile. For the input match, a simple four element high-pass, low-pass network was borrowed from a 5-11 GHz broadband medium power amplifier and re-tuned for a 10 GHz input center frequency. The output match was borrowed from a 20 GHz VCO design. Simulations of the doubler (Figure 1) show a strong second harmonic, but an even stronger undesired fundamental frequency. The fundamental could be filtered from the doubler output to accentuate the second harmonic. A plot of measured versus simulated s-parameters shows good agreement (Figure 2). Note that the spectrum plot seems to follow the S21 gain, with best operation around the 10 GHz design frequency. The DC bias can be optimized for best operation, and as expected, biasing lower than Class A towards Class B tends to enhance the second harmonic, particularly at lower input drive levels. Figure 3 shows the measured performance of the second harmonic versus input power level compared to simulations at 9, 10 and 11 GHz; showing reasonable agreement with the output, typically 2 dB lower than simulations. The input DC bias supply was -3V, which is divided through resistors to supply a gate bias that is closer to pinchoff (~-0.33V) and accentuates the second harmonic at lower drive levels. Figure 4 shows

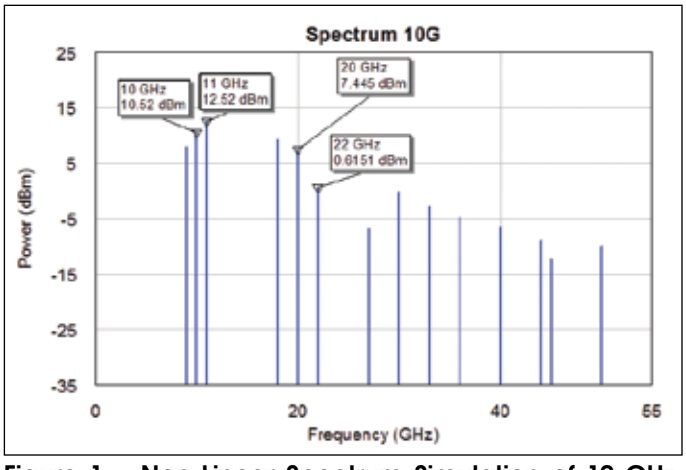



**Figure 1 • Non-Linear Spectrum Simulation of 10 GHz Doubler (Inputs: 9, 10, & 11 GHz).**

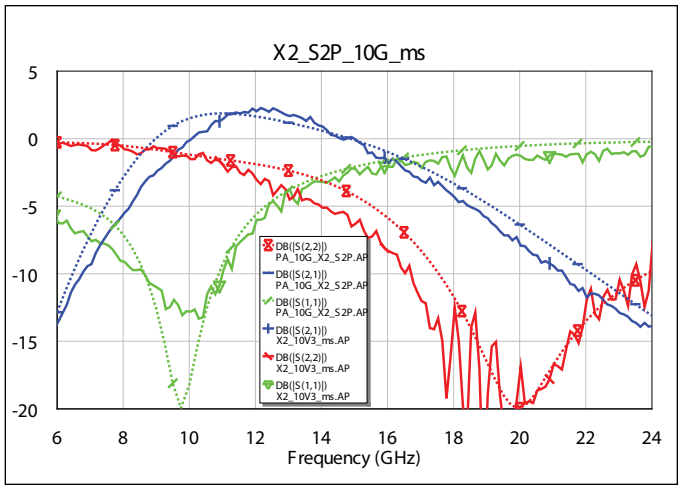



**Figure 2 • S-Parameters of 10 GHz Doubler (Measured-solid, Simulated-dotted).**

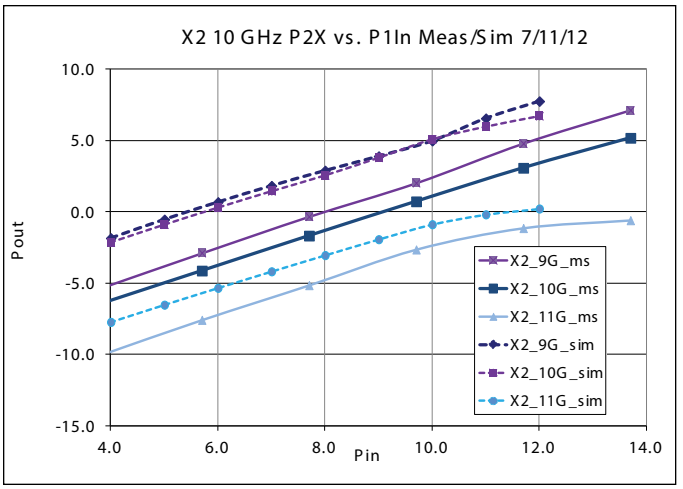



**Figure 3 • 2nd Harmonic Output Power vs. Input at 9, 10, and 11 GHz (Measured, Simulated).**

the same measurements at 9, 10 and 11 GHz with a -3V input DC supply versus 0V at 10 GHz ("X2_10G") which has less second harmonic at lower drive levels but nearly matches the -3V results at higher drive levels. Figure 5 shows the final layout of the 10 GHz frequency doubler.

### Frequency Doubler at 8 and 16 GHz with Fundamental Harmonic Stub Attenuator

For the next doubler designs, a harmonic stub was added to attenuate the fundamental input frequency. Additional filtering might be required to attenuate harmonics, but a simple one quarter wave open circuit stub on the output presents a short circuit at the fundamental, while presenting an open circuit at the desired second harmonic. Input matching circuits were designed for low return loss at the fundamental, while output matching circuits were designed for low return loss at the second harmonic. The harmonic stub doubler design for 8 GHz to 16 GHz operation, had an input conjugately matched to S11 of the PHEMT at 8 GHz, and an output match conjugately matched to S22 of the PHEMT at 16 GHz.

Simulations of the 8 to 16 GHz doubler (Figure 6) show a strong second harmonic, with an attenuated fundamental. Additional filtering on the output of the doubler could be added to further accentuate the second harmonic. Originally, the measured versus simulated s-parameters showed poor agreement (Figure 7). Once Sonnet EM software was used to simulate the actual layout, the discrepancy in the original simulation is due to the harmonic quarter wave stub. There must have been parasitic coupling in the layout that was not included in the original simulation. Adding the Sonnet Electromagnetic (EM) simulation of the stub alone matches well with the measured data, as does the full Sonnet layout simulation as shown in Figure 8. Figure 9 shows the actual layout and the Sonnet geometry. The Sonnet EM simulation correctly simulates the affect of parasitic coupling in the quarter wave meandered stub. It should be noted that the error in

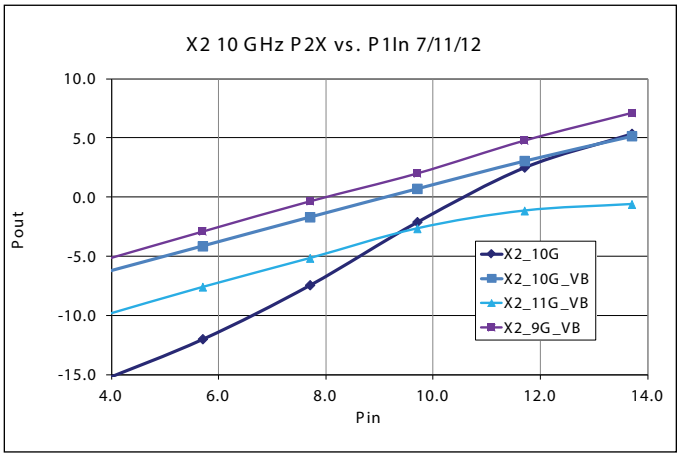



**Figure 4 • Second Harmonic Output Power vs. Input Power at 9, 10, and 11 GHz (0, -3V).**

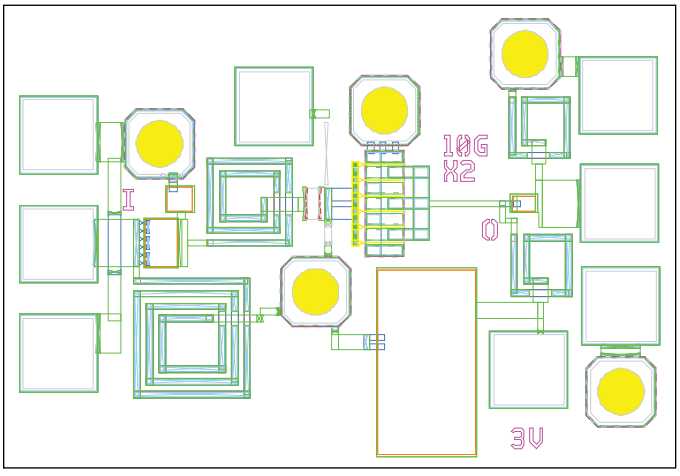



**Figure 5 • Layout Plot of 10 GHz Frequency Doubler (~0.8 x 0.6mm).**

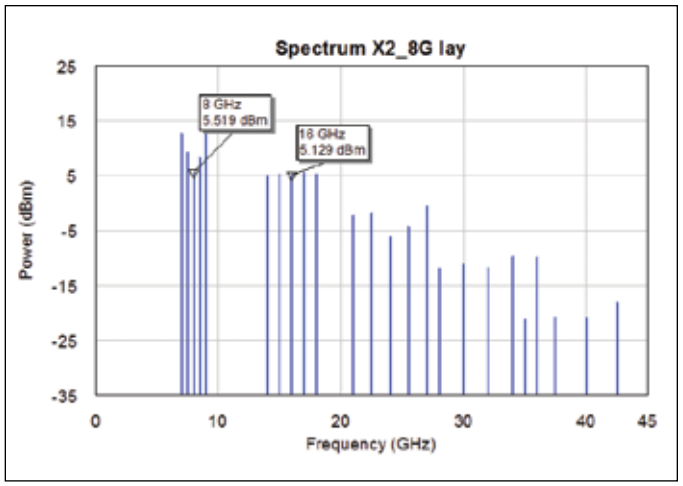



**Figure 6 • Non-Linear Spectrum Simulation of 8 GHz Doubler (Inputs: 7, 7.5, 8, 8.5, & 9 GHz).**

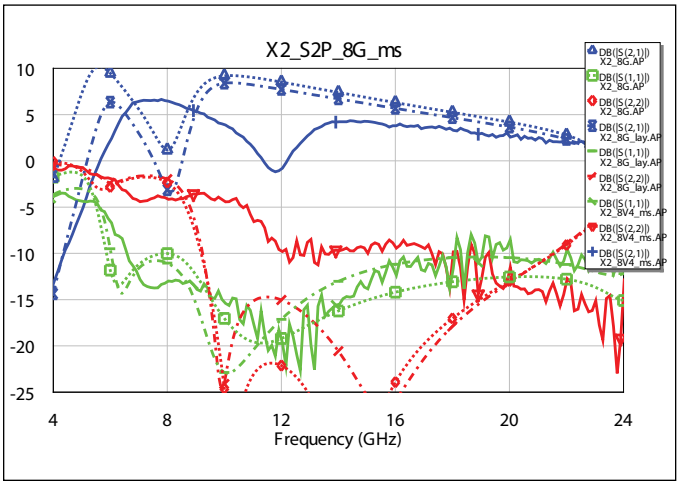



**Figure 7 • S-Parameters of 8 GHz Doubler (Measured-solid, Original Simulations-dotted).**

the harmonic stub simulation mostly affected the attenuation of the fundamental frequency, which shifted to a maximum attenuation at 12 GHz, rather than the desired 8 GHz, while retaining little effect on the second harmonic. Figure 10 shows the measured performance of the second harmonic versus input power level at 8, 11, 11.5, and 12 GHz; showing reasonable agreement with the output, though typically 2 dB less than simulations.

Likewise, a 16 GHz to 32 GHz doubler was designed with the same approach, with a meandered quarter wave stub approximately half as long as the 8 GHz stub previous. Unfortunately, the 16 GHz stub attenuation was also shifted up in frequency compared to the original simulations, but again, was correctly predicted with Sonnet EM. The EM simulation uses the physical layout, thus including any layout parasitics not modeled in the original linear simulations.

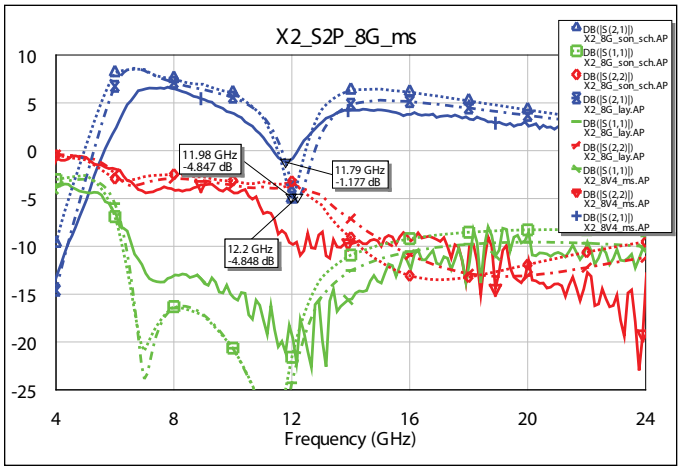



**Figure 8 • S-Parameters of 8 GHz Doubler with EM Simulation (Measured-solid, Full Sonnet-dot/dash, MWO+Sonnet Stub--dotted).**

Simulations of the 16 to 32 GHz doubler (Figure 11) show a strong second harmonic, with an attenuated fundamental leakage. Again, additional filtering after the doubler could be provided to further accentuate the second harmonic. Originally, the measured versus simulated s-parameters showed poor agreement (Figure 12). Sonnet software was used to simulate the actual layout, which matches well with the measured data as shown in Figure 13. Figure 14 shows the actual layout and the Sonnet EM plot which correctly simulates the affect of parasitic coupling in the quarter wave meandered stub. It should be noted that the error in the harmonic stub simulation affected the attenuation of the fundamental frequency which was shifted higher to around 21 GHz, from 16 GHz, but retained little effect on the second harmonic. Figure 15 shows the measured performance of the second harmonic versus input power level.

**Summary:**

These frequency doubler circuits were designed with a simple approach to illustrate a couple of concepts. First, the input match assumed a simple conjugate input match of the active device at the fundamental frequency (S11*), while the output match was designed for a conjugate output match of the active device at the second harmonic (S22*). A simple quarter wave microstrip open circuit stub was used to attenuate the fundamental helping to prevent leakage through to the output. While these simple frequency doubler MMIC circuits were used to illustrate a first cut doubler design, they also illustrate the efficacy of the non-linear and linear models, as well as, illustrating the occasional necessity for an EM simulator, such as Sonnet, to accurately predict the actual layout parasitics. These designs could be optimized further with additional non-linear simulations and/or measurements. If the chance arises, the circuits may be re-fabricated with the harmonic

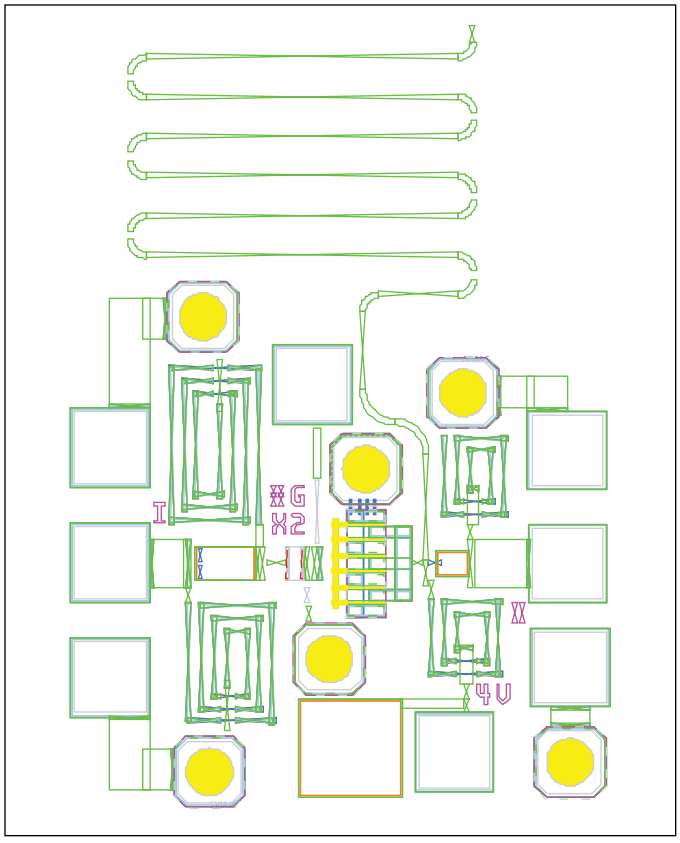
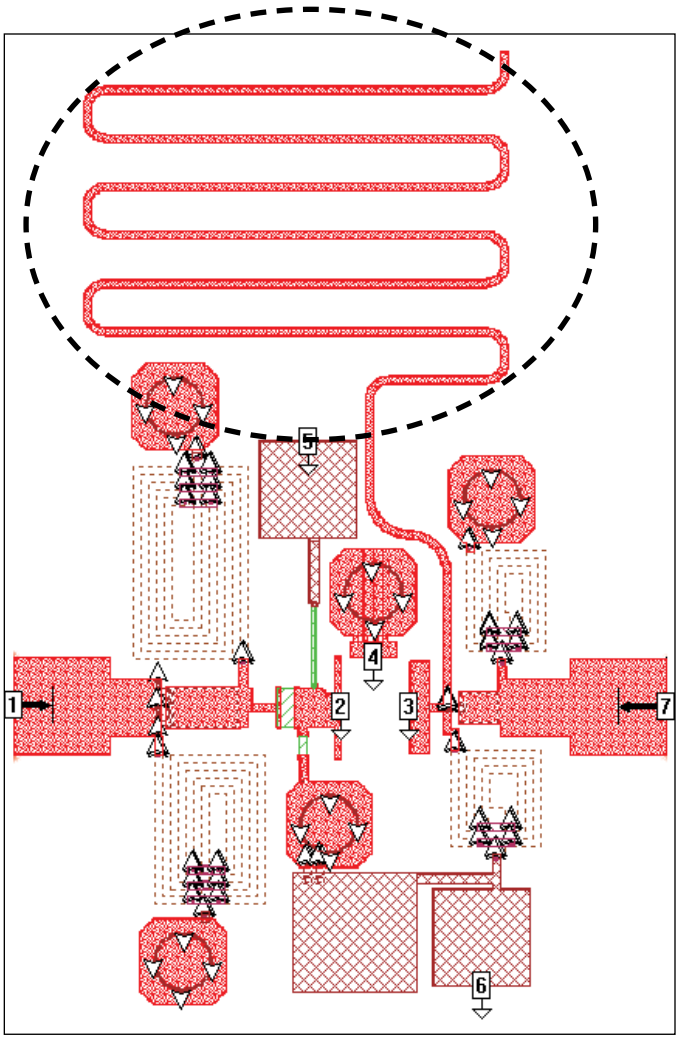


Figure 9 • Layout and Sonnet EM Plot of 8 GHz Frequency Doubler (~0.65x1.0mm).



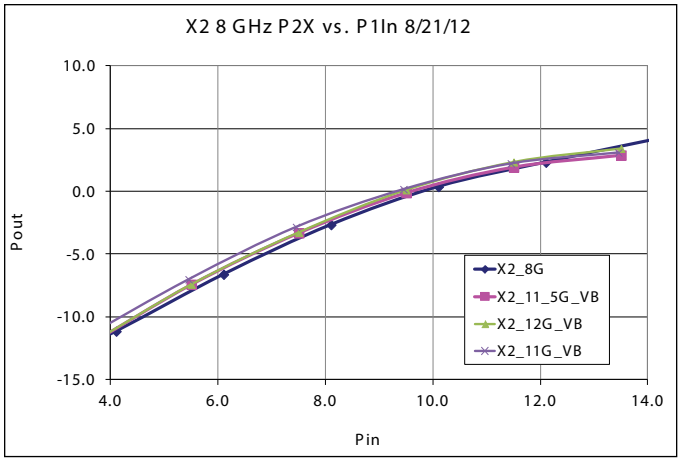




Figure 10 • 8 GHz Doubler 2nd Harmonic Output vs. Input Power at 8, 11, 11.5, and 12 GHz.

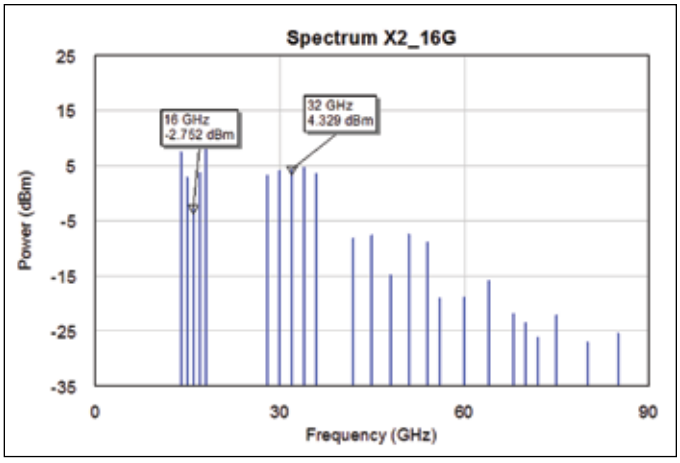



Figure 11: Non-Linear Spectrum Simulation of 16 GHz Doubler (Inputs: 15-17 GHz).

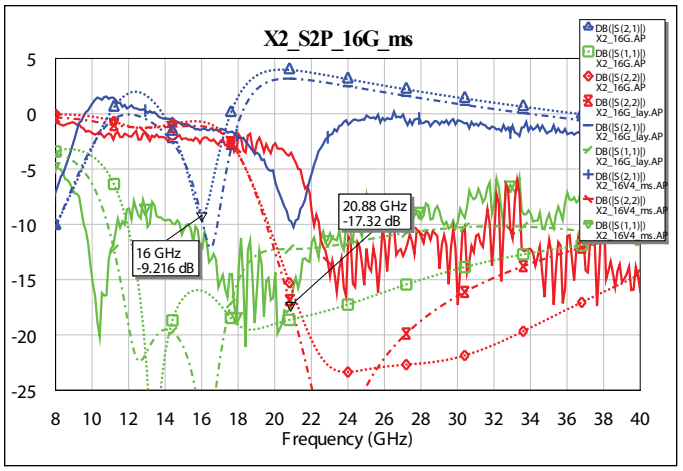



**Figure 12 • S-Parameters of 16 GHz Doubler (Measured-solid, Original Simulations-dotted).**

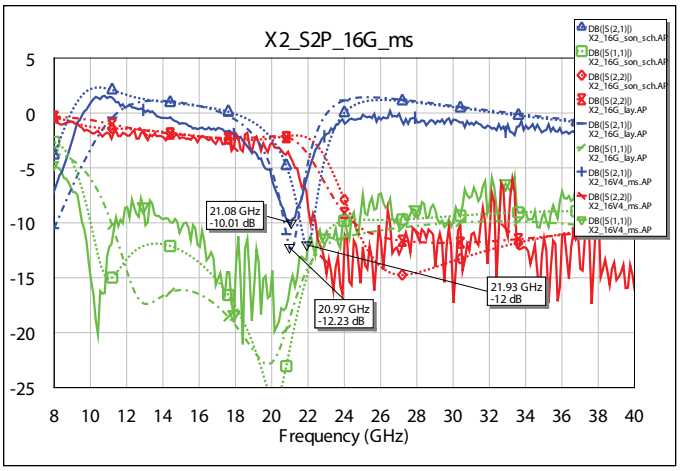



**Figure 13 • S-Parameters of 16 GHz Doubler with EM Simulation (Measured-solid, Full Sonnet-dot/dash, MWO+Sonnet Stub--dotted).**

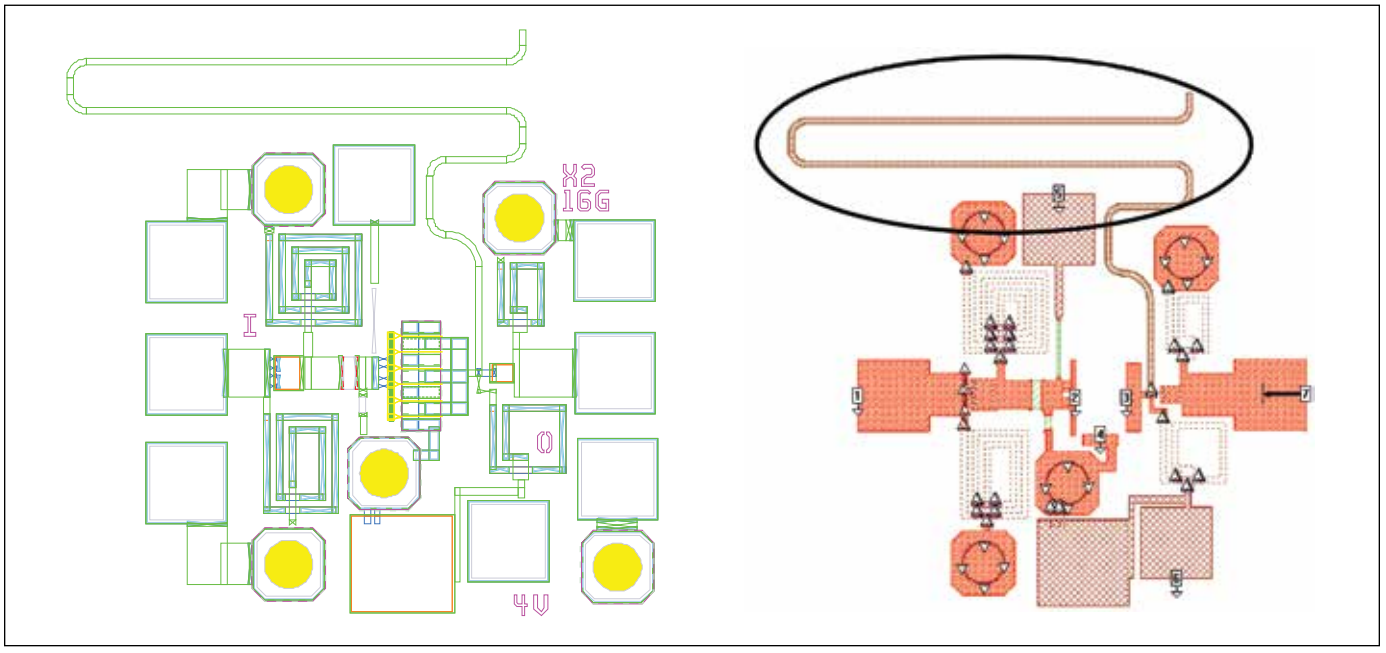



**Figure 14 • Layout and Sonnet EM Plot of 16 GHz Frequency Doubler (~0.7x0.8mm).**

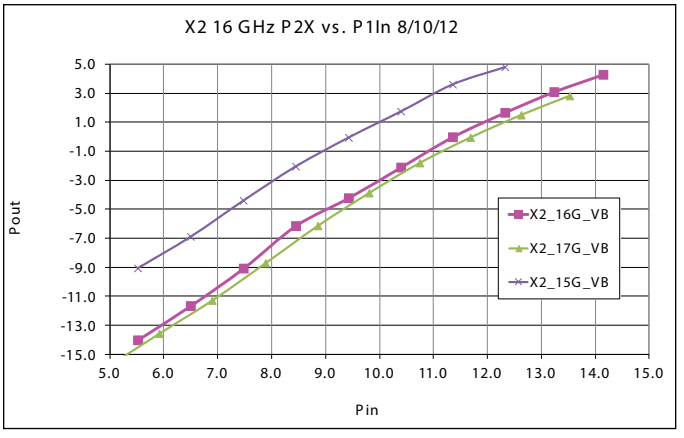



**Figure 15 • 16 GHz Doubler 2nd Harmonic Output vs. Input Power at 15, 16, and 17 GHz.**

stubs adjusted to account for the parasitic coupling in the layout which was correctly simulated in the EM simulation.

**About the Author:**

John Penn has been an adjunct professor in the Johns Hopkins University Engineering for Professionals (EP) program since the first JHU MMIC Design Course was offered in 1989. Previously, he was a full time engineer at the Applied Physics Laboratory for 26 years before joining the Army Research Laboratory in 2008. He currently serves as the Team Lead for RFIC Design in the RF Electronics Branch.